

## Component Failure Analysis - Hermetic Packaging

Recently ACI Technologies was asked to perform failure analysis on a hermetically sealed transistor for potential electrostatic discharge (ESD) or electrostatic overstress (EOS).

ACI was asked to determine if the field-failed transistor was damaged by ESD or EOS. In order to properly assess the failure, additional samples were requested.

- New transistors: “stock” transistors which are still sealed in original manufacturer packaging.
- Production passed transistor: tested and passed by the customer as a good transistor.
- Production-failed transistor: tested and failed by the customer as a bad transistor.
- Field-failed transistor: tested and passed by the customer and used in the production build, but now no longer functions after some usage in the field.

Slight variations between the bad and the good transistor could be an indicator of the failure mechanism.

Before delidding, non-destructive testing by x-ray inspection was performed to provide a baseline for the as-received device (Figure 1). This will be used later to determine if any damage resulted from the delidding process.

The delidding procedure was performed with a pair of sharp, heated razors. This carefully melted away the top casing of the hermetically sealed transistor to physically remove the lid from the device. Clearance from the top of the wire bonds must be considered to avoid removing too much or too little of the packaging. Often times, x-ray inspection would be used to gauge the clearance distance from the top of the hermetic packaging. Afterwards, an optical microscope is used to examine the die and wire traces for any damage from the delidding process and to help determine the failure mechanism (Figure 2).

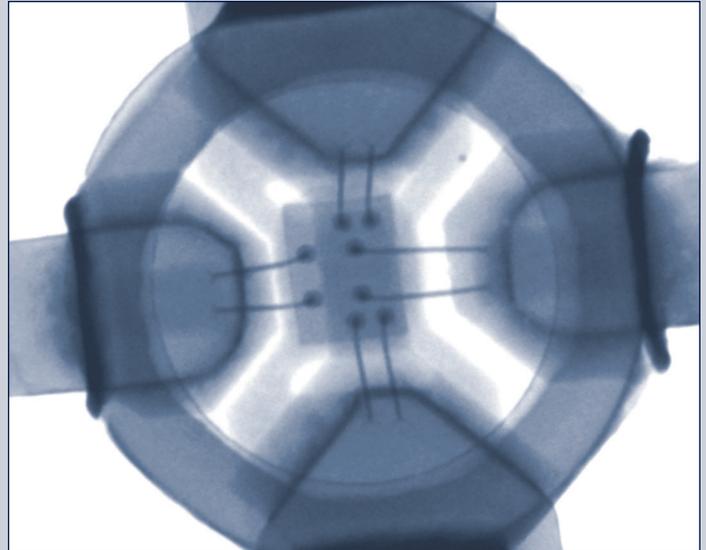


Figure 1: X-ray image of field-failed transistor prior to delidding.

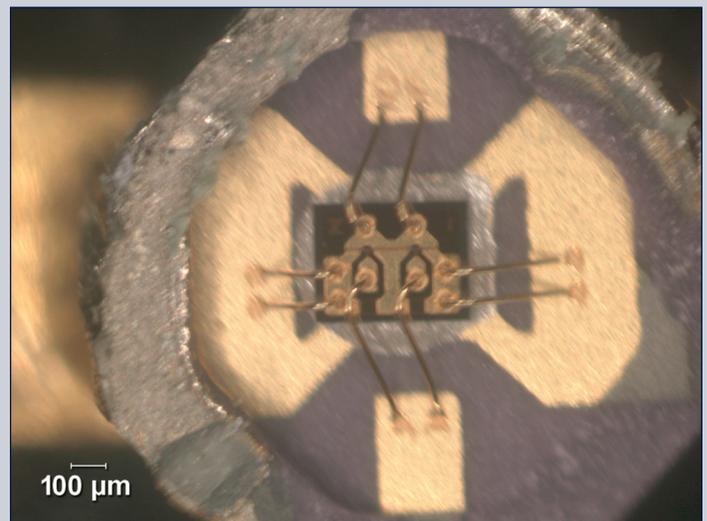


Figure 2: Optical image of field-failed transistor.

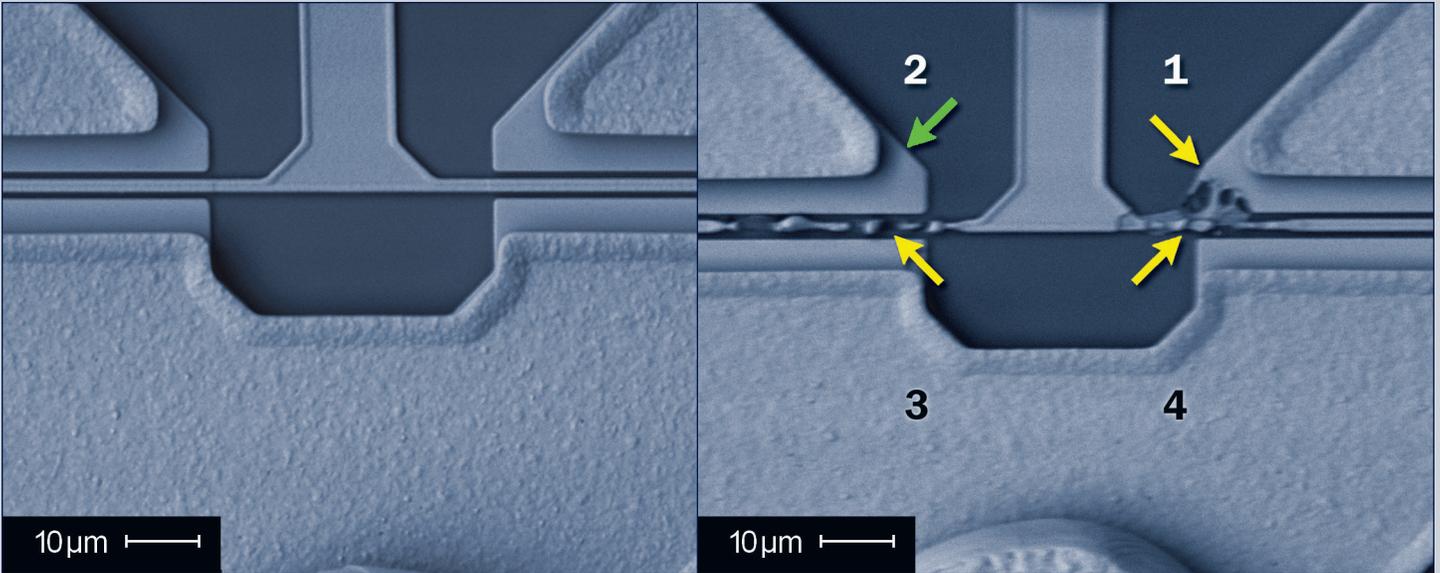


Figure 3: Shown on the left is a SEM image of good transistor. To the right is a SEM image showing EOS damage (indicated by yellow arrows).

Figure 3 shows that higher magnification with a scanning electron microscope (SEM) is necessary for a closer examination of die, wire bonds, and traces. Melted traces were clearly observed at the higher magnification which typically indicated EOS damage. The large current caused by the electrical overstress was high enough to melt pad #1 and traces #3 and #4.

Delidding was critical for identifying the failure mechanism since it allowed internal observation with no obstructions. For very small devices like this transistor, SEM is necessary when features like wire bonds and traces are difficult to examine under optical microscopy.

For the production-failed transistors, no obvious signs (post-delidding) of ESD or EOS damage were observed on the die, wire bonds, or traces by SEM or optical microscopy. ACI recommended that superconducting

quantum interference device (SQUID) analysis be performed to isolate potential ESD damage. SQUID has the capability of mapping the entire die area for high densities of charging by electromagnetic field strength intensity.

For assistance with electrostatic overstress, electrostatic discharge, or other failure analysis of components and board assemblies, contact ACI by calling 610.362.1320, emailing [helpline@aciusa.org](mailto:helpline@aciusa.org) or visiting the website at [www.aciusa.org](http://www.aciusa.org).

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