

Advanced Packaging Technology

A major goal of the development of advanced packaging technology is to reduce the size, weight, and power consumption of electronics components using state-of-the-art commercial technologies.

One of the novel concepts involves the use of all three spatial dimensions when designing and producing new systems. In the past, electronic structures tended to be two dimensional in nature. Generally speaking, individually packaged integrated circuit (IC) dies were interconnected on printed circuit boards. Techniques such as die and package stacking naturally contribute to a reduction of the spatial footprint of any given electronic system design. Several examples of the stacking concept are shown in Figures 1 and 2.

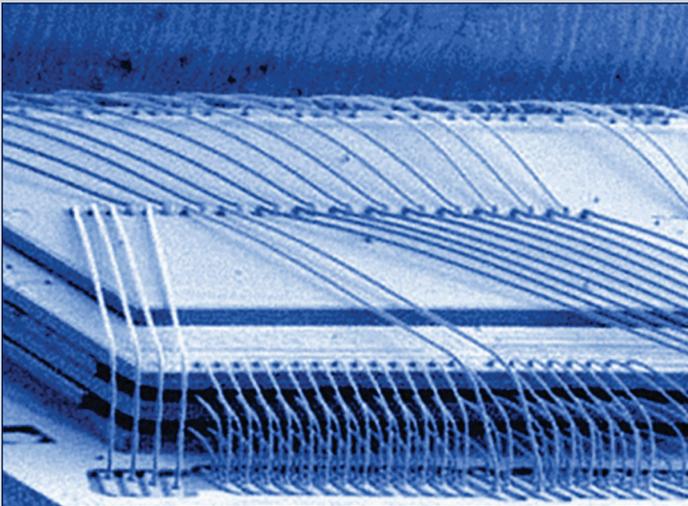


Figure 1: Wire bonded die stack.

In many cases, die stacking results in a structure that requires the die interconnection wire bonds to be physically crossed. Under these circumstances, electrical shorting of the routing interconnections between stacked dies can become a problem. A solution to this problem is the introduction of an interposer into the stack. The interposer is a higher circuit density adapter that reroutes the connections of a die to allow wire bonding to another die or package without the need to cross the connections. An example of an interposer is shown in Figure 3.

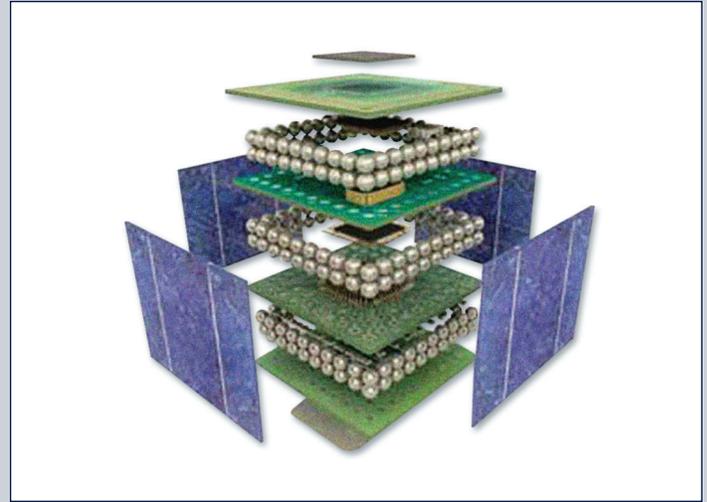


Figure 2: Stacked package.

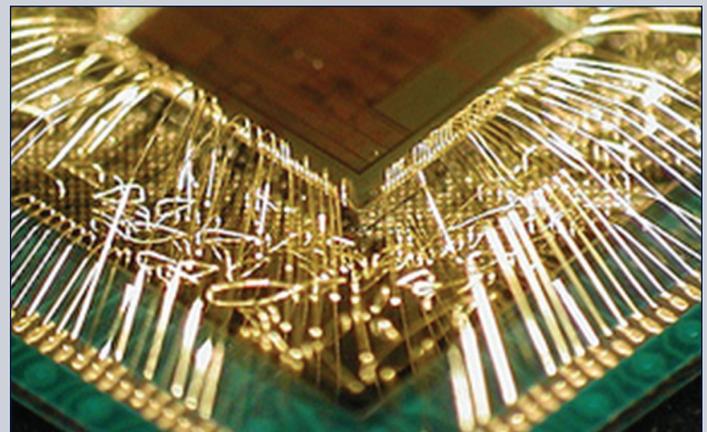


Figure 3: Wire bonded interposer.

Another method of providing high density interconnection is referred to as flip chip. Instead of wire bonds connecting the input/output (I/O) pads on the IC to a lead frame or another die, each I/O pad has a “bump” made of solder, conductive epoxy, or even a “stud bump” which is made from the ball from a standard wire ball bond. The chip is then flipped over so that its active surface is face-down toward the substrate circuit board and connected to the circuit using the metal

or conductive epoxy. The short (usually only a few thousandths of an inch, or “mils”) interconnection of the bump has substantially lower inductance and capacitance than the long (10-100s of mils) bond wires of the conventional wire bonded and glob-topped packaging.

In addition to the lower inductance and capacitance at radio frequencies, and the real estate savings due to the elimination of long wires, another major advantage is the “area array” of I/O connections available in the flip chip method (Figure 4). Only “peripheral” I/O pads (pads at the perimeter of the chip) can be wire bonded. However, I/O pads can be designed onto the chip anywhere on the surface for flip chip attachment. This gives flip chip a great geometrical (real estate) advantage over wire bonding in the number of I/O connections that can be placed on a chip, which results in smaller chips. A lower cost can also be realized for designs that are limited to the number of wire bonds they can have by edge length.

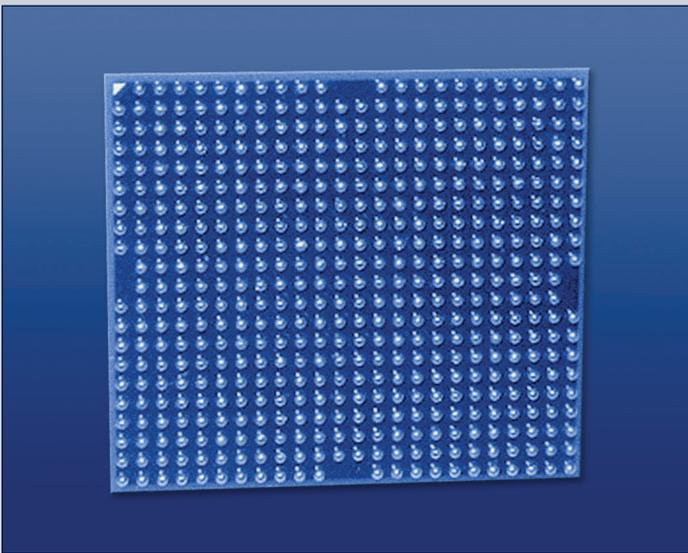


Figure 4: Flip chip ball grid array.

Advanced packaging technology will incorporate a mixture of the previously mentioned packaging technologies to produce a new generation of electronics modules. This will enable the incorporation of new capabilities into a wide variety of electronic systems.

For more information on advanced packaging technology, please contact the Helpline at 610.362.1320, via email to helpline@aciusa.org or visit the website at www.aciusa.org.

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