Nexlogic - Design-For-Test Considerations For PCB Design

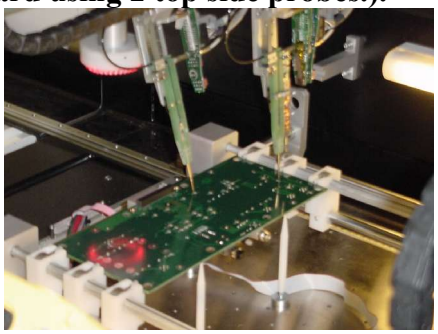
Deck: Effective DFT for PCB designs demands a number of key considerations. Overlooking any of them may result in costly rework.

Byline: Zulki Khan, president and founder, Nexlogic Technologies, Inc., 2075 Zanker Road, San Jose, CA 95131 www.nexlogic.com, zk@nexlogic.com, (408)436-8150 ext. 102

Contact: Dan Garza
DGPR
dlgarza@dgpr-inc.com

The perennial question in electronics design and manufacture is: "How do I design a printed circuit board (PCB) so that it can be properly tested?" To achieve this objective, there are a number of design-for-test (DFT) considerations and techniques. Some are major, others, minor. However, the total contributes to a highly effective PCB design so that testing procedures applied to a given design result in high 90 percent plus test coverage.

Initially, the PCB design engineer should lay out all test points on one side of the board. It's considerably faster and inexpensive to test a board when the accessing probes are available on one side. There can be multi-side probes on some select flying probe testers, but they pose greater cost since they incur more time to generate the test programming (See Fig # 1 below where Flying Probe testing is performed on a circuit board using 2 top side probes.).



Sometimes, both the top and bottom probes may not be able to be run at the same time. Hence, it is highly recommended that all test points be laid out on the same side of the board.

Another consideration is maintaining minimum test point distance from one test point to another there should be minimum distance of 100 ml., accounting for about 2.54 millimeters so that probes can perform their job properly. Test points designed too close to each other presents the possibility they will interfere with one another and cause the test not to be performed effectively, thus reducing the test coverage area.

Test point distribution is important factor, as well. A high density of test points or clusters should be avoided. Test points should be uniformly distributed throughout the board, making it easier to test with multiple probes and not having to rely on a specific area for all the probes to concentrate on.

Moreover, there should be a free zone or a safe zone designated as a *keep out* area. This real estate is designed for components that are tall in size. If component height interferes with test methodology, then a safe zone or keep out area should be designed at the layout stage, where there are no test pads. When components are too high, probes may not be able to access those pads; therefore, it is imperative that a safe zone for these high components is designated in the PCB design.

While doing the layout and when feasible, it is a good idea to consider using standard commercial electronic modules, which are available for testing. However, if there are redundant modules, are they being laid out so that they can be tested independently? Put another way, if there's a fault in one module and not in the second, third and fourth, each module should be available for independent testing. It is important here that there is accessibility to each address and data and bus line.

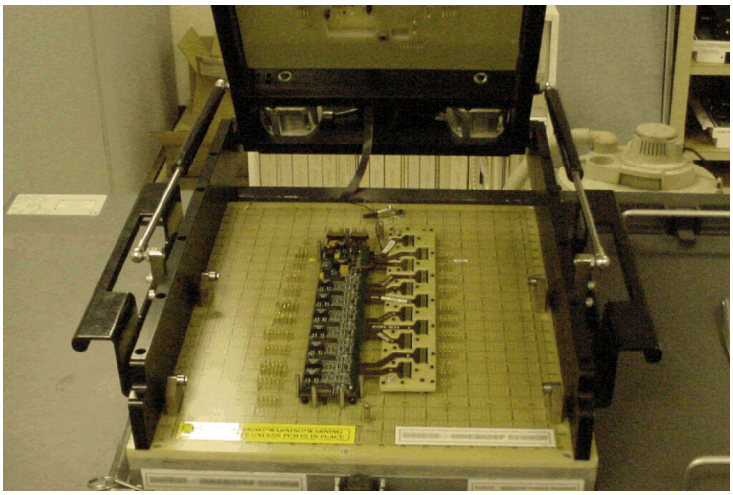
The PCB designer must determine whether or not system level feedback loops are de-controllable. Also, while the board is being tested, are all system and subsystem specs made available, to the test technician for the debugging purposes? Also, test probe nodes should have access to at least one test node. Every separate node should have one test point and maybe multiple points.

The amount of total load current must be considered. Power and ground nodes should be independently accessible and test targets should be evenly distributed, especially for high-speed designs. Target test pad is 25 ml. smallest, while optimal test point size is 40 ml., so although 25 mil. is acceptable, but nothing smaller than that should be used as pad size for a test point. Boundary scan can be used to reduce test development time, plus it solves the node access issues at the same time.

Multiple boards in a panel form could pose a limiting factor for a tester. This problem usually occurs as a DFM issue under fabrication process. If a small board is being tested and there are 15 to 20 boards in a panel, for example, it is important to keep in mind tester's physical limitations, so as to how big of a panel size can be tested on a tester, when all the test probes could comfortably reach all the test points in the panel. Also, if too many boards are placed in a panel, they may considerably slow down the tester. Hence, there should be an optimal balance between number of boards on a panel versus the speed of the tester.

There should also be at least two mounting holes, which could be used as datum points across from each other. Three would be good but at least two are absolutely necessary. Test points should not be covered by solder resist or ink or any other kind of non-conductive material because the probes need clear access to those test points.

When implementing fixture changes, in case of ICT (In circuit testing), they must be kept to an absolute minimum. The ICT fixture, costs the most amount of money, in some cases from $25K to even $50K (See Fig # 2 below where an ICT Fixture is shown with a circuit board mounted on it on a HP 3070 tester).



It is prudent not to make many fixture changes, even if there are changes made in the design, fixture changes should be kept to a bare minimum, to avoid extreme costs that are associated with the fixture changes. The same test fixture can be used for small changes (10% or less), but for the bigger changes, the fixture needs to be redesigned, thus costing huge sums of money.

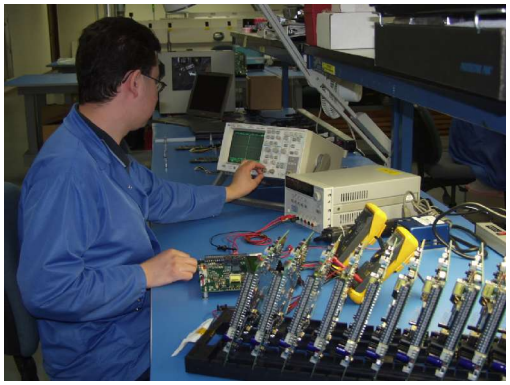
In conclusion, other DFT considerations may be regarded minor, but in reality play a major role in the overall requirements for effective DFT. One general guideline for DFT is making sure that all vias are left unmasked. Vias don't need to tenting because accessibility of the net through vias must be available if test points are not available or not designed in. Also, SMT pads should be designed slightly larger if very fine pitch SMT components are involved to give better access contact points to the test nodes. One must keep in mind board's real estate as well as other DFM considerations, for example, ample access by the testing probes especially when flying probe testing is conducted.

Access to service signals through connectors is another key DFT consideration. If a microprocessor is being designed, it should have disabling capability features, especially if the design calls for device programming. In this case, it is important to disable the functionality before programming the device.

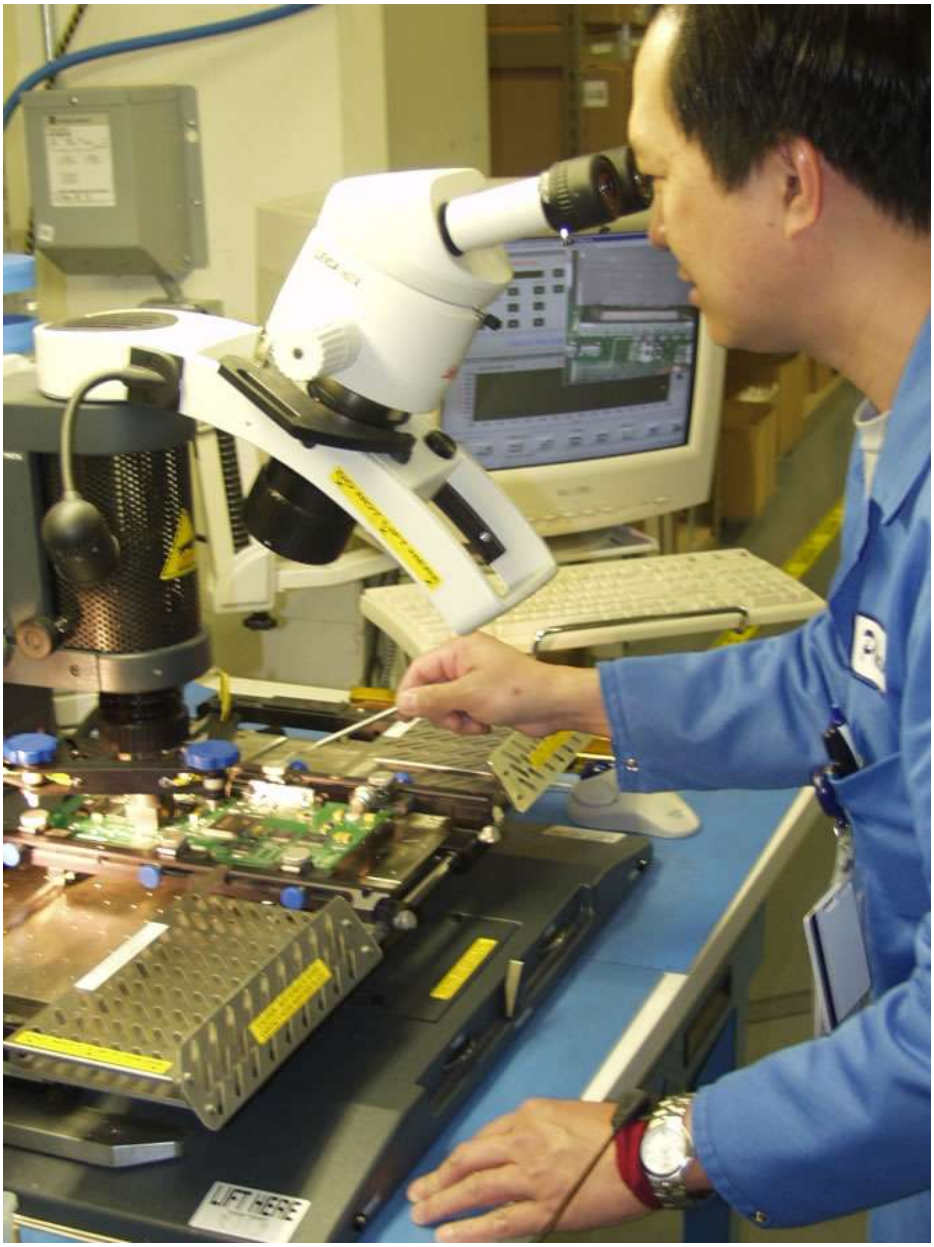
Manufacturing tolerances must also be made part of a DFT design to avoid the tombstoning effect. Accurate geometry design for components at the layout

stage is critical to avoid problems at test, such as enough accessibility on the pad for the test probes, if the pad size that are designed are small in size.

Last, but not least are documentation accuracy and CAD software. Are all testing procedures available and are repeatable with high level of confidence (See Fig # 3 below where in the test lab, functional testing is being performed by a test engineer)



Are all ECOs documented? Is the testing procedure repeatable? A *golden* board should be made available for testing before a given batch is started. This provides the test engineer a reference point, if necessary during the test procedures. Plus, the more precise CAD tools used for DFT such as generating a netlist from a design database verses gerber generated netlist. The more accurate the testing results would be, the less time would be required to debug the board(See Fig # 4 below).



More comprehensive test procedure is written and called out for, more accurate the test results would be. Also more test coverage is detailed in the test procedure, less debug time would be required by the test engineer to test and debug the board.

##########