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Boundary Scan Skews Test Coverage Tradeoffs in your Favor

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Introduction

The complexity and programmability of modern embedded boards means that knowledge built up during debugging and testing must be regarded as Intellectual Property (IP) and therefore preserved. But many of the processes and tools used today do not provide a means to preserve or pass on this IP, and thereby forego valuable opportunities to save time and improve quality during subsequent stages of product development.

Boundary scan testing creates a test infrastructure that is inherently suited to preserving and re-using test knowledge throughout the product lifecycle. It provides a convenient means for original equipment manufacturers, design houses, test specialists and electronic manufacturing services (EMS) providers to maximize the value of this test IP, which is every bit as valuable as design IP as it can be reused, enhanced, and extended, to add value throughout the product lifecycle.

Preserve Test Knowledge as IP

Test engineering often happens at least twice in a product's lifetime. The first time is during prototyping, as development engineers create their own tests as part of the design and debugging phase. However, many of the tools and techniques used in development laboratories do not provide an intuitive or standardized way to record the tests or the results. As a result, this board-level test IP, built up during development, is mostly wasted as production test engineers are effectively forced to carry out a second test engineering project for the same product.

XJTAG's Boundary Scan - a Natural Test IP Framework

Embedding a boundary scan chain on the board to interconnect the test ports of JTAG-compliant components creates the foundation for product teams to create valuable IP by recording test knowledge. The XJTAG system combines the BSDL files for the components on the board with the board netlist and a test script written by the engineer that describes how the device is to be tested. The XJTAG scripts (see example) are written in an intuitive high level language, which is easily readable by electronic designers and software engineers.

The use of a high level language abstracts engineers from the intricacies of the boundary scan data stream. This supports fast test development, eliminates human error, and facilitates development of sophisticated test routines that require minimal physical access to the board.

Device-Centric Scripts Promote Re-Use

The device-centric nature of XJTAG tests means that a script for a particular device can be stored and re-used at a later date when the same component is designed into a subsequent product. In this way, XJTAG achieves a device-centric approach to boundary scan testing that facilitates re-use of test knowledge acquired throughout the product lifecycle. Hence, engineers using this technique are effectively creating test IP that can be used again and again to reduce development costs and turnaround time for a multitude of board and product designs.

The script-based nature of the test allows easy integration with other production test techniques such as ICT, flying probe or functional testing. This provides additional freedom for test engineers to create hybrid test strategies that take advantage of all the physical and electrical characteristics of the board, and thereby achieve very high levels of test coverage.

Conclusion

Great power is gained from the seamless flow of test information from one department to the next, continuously growing and being reused. The key to exploiting this power is to understand the value of test knowledge as precious IP, and to take steps to preserve it.

The JTAG test structure provides a standard platform which can be utilised throughout a given product’s complete lifecycle. Furthermore, focusing test compilation at the device level, rather than the board level, maximises the value of re-use by allowing proven test scripts to be incorporated directly in subsequent projects.