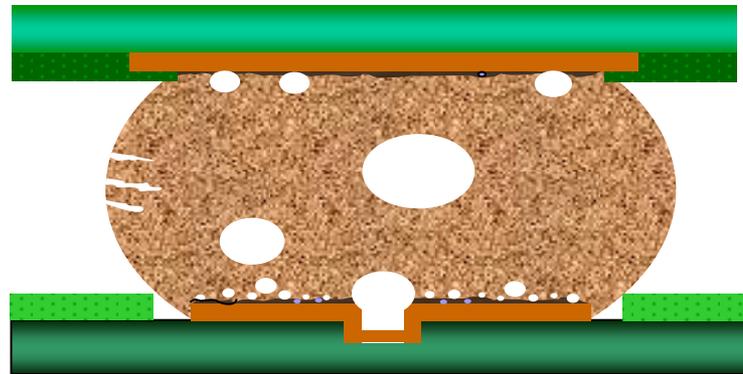


VOIDS IN SOLDER JOINTS



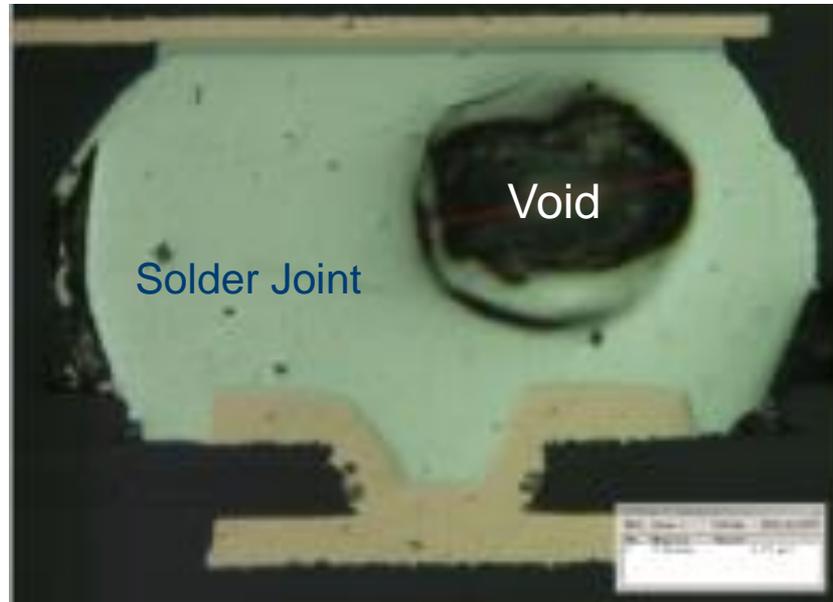
Raiyo Aspandiar
Intel Corporation
raiyo.f.Aspandiar@intel.com

Contents

- **Introduction to Solder Voids**
- **Various Types of Voids**
 - **Description**
 - **Detection**
 - **Root Causes**
 - **Ways of mitigating**
- **Summary**

What is a Solder Joint Void?

Typical BGA Solder Joint with a large Void



- **A void is an absence of solder within a solder joint**
- **A void typically contains nothing but air**
- **Some voids contain flux residues or cured resins when epoxy fluxes or resin containing pastes are used**

Why do we care about Voids?

- **Some types of Voids deleteriously impact Solder Joint Reliability**
- **Voids reduce the thermal conductivity of the solder joints**
- **Voids can cause solder bridges**
- **Voids can cause solder transfer between neighboring solder joints during the reflow soldering process**
- **In small solder joints, voids can significantly reduce their current carrying capacity**

Types of Voids

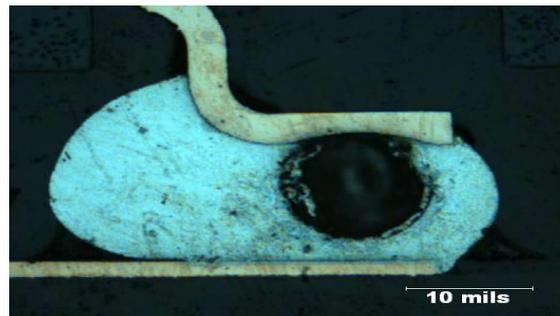
- **Macro Voids**
- **Planar Microvoids**
- **Shrinkage Voids**
- **Micro-Via Voids**
- **IMC Microvoids**
- **Pinhole Microvoids**

MACRO-VOIDS

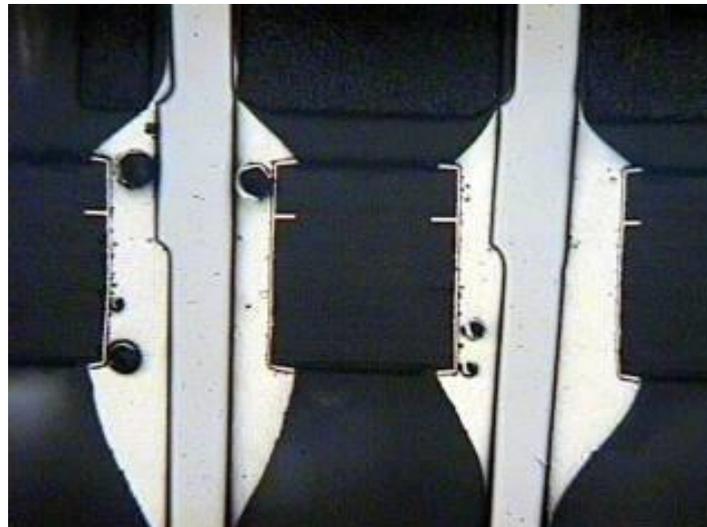
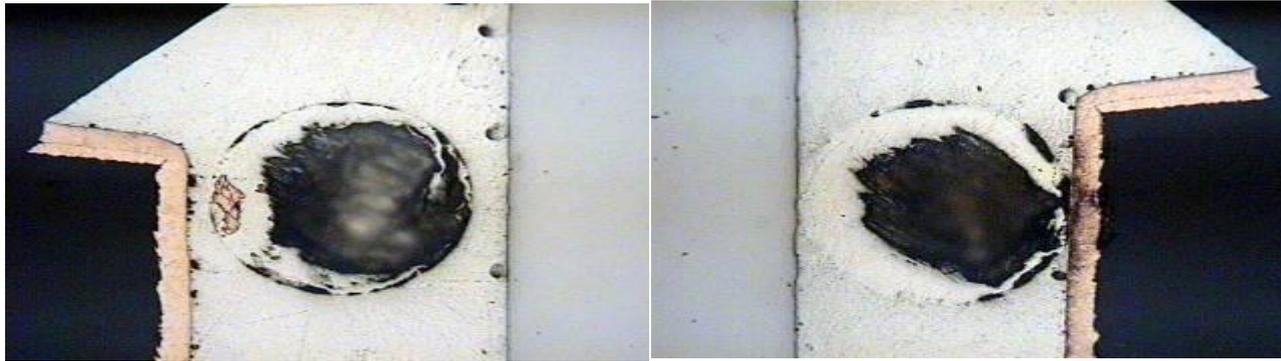
Description - Macrovoids

- **Voids generated by the evolution of volatile ingredients of fluxes and solder pastes**
 - **Insufficient time to escape**
- **100 to 300 μm (4 to 12 mils) in diameter**
- **Found anywhere in the solder joint**
 - **Not Just at Land to solder interfaces**
- **NOT unique to SnAgCu (LF) solder joints**
 - **Eutectic SnPb**
 - **SnBiX**
- **Also called “Process” voids**
- **Generally, when SMT process engineers talk about voids in solder joints these are the type of voids that are being referred to**

Examples of Macrovoids in BGA Solder Joints



Examples of Macrovoids in Through Hole Solder Joints

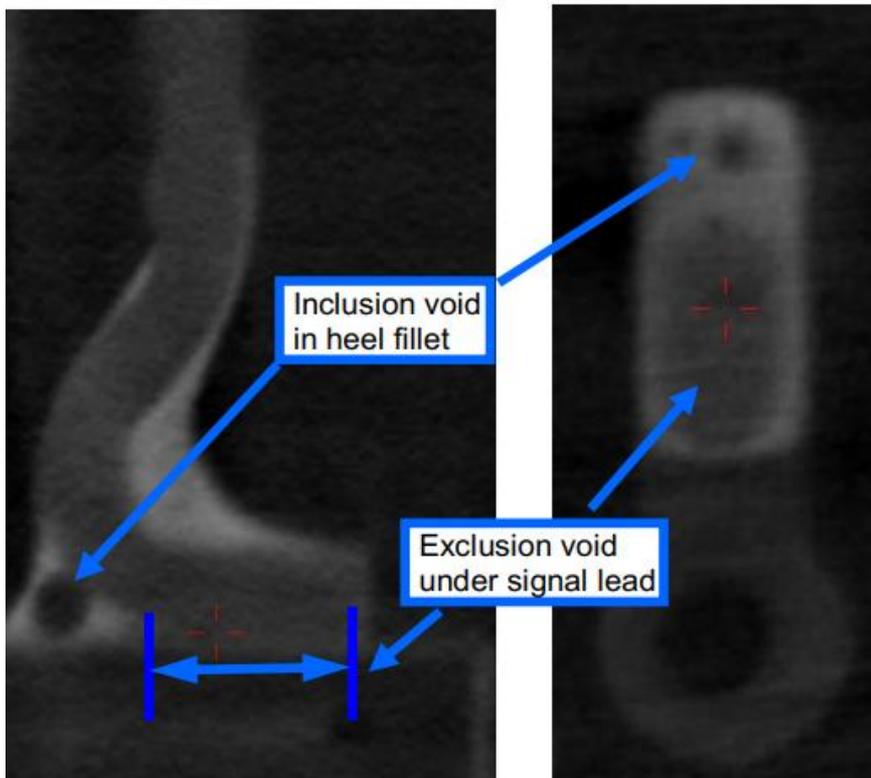


Causes of Macro Voids

- **Trapped gases within the solder joint which have insufficient time to escape during the reflow process when the solder is molten**
- **Source of these gases**
 - ***Chemical Ingredients of fluxes and solder pastes that evolve during the SMT reflow process when the temperature of the materials is raised above their boiling point***
 - ***Absorbed moisture in the board laminate and lands that evolves above 100C***
 - ***Water vapor resulting from the reduction of Oxides on the surfaces of solder particles in the paste and solder balls as well as on the board lands;***
 - ✓ **These oxides are reduced by the action of the organic acids in the flux**

Inclusion vs Exclusion Macro Voids

-- Typically for Gull Wing Solder Joints --



Images and Exclusion Voids concept from T.L. Lewis, C.O. Ndiaye and J.R. Wilcox, "Inclusion Voiding in Gull Wing Solder Joints", APEX EXPO Proceeding, 2012

Type	Shape(s)	Causes
Inclusion	Spherical, elliptical, Cigar-shaped	Trapped gases
Exclusion	Irregular shapes	Squeeze out of solder paste, hot tearing, ductile rupture

✓ **Exclusion Macro Voids have causes different from typical macro voids**

Areas Critical to Macro Void Generation

- **Solder Paste**
- **Reflow Soldering Process**
- **Printed Circuit Board**
- **Component**
- **Other**

✓ **Control of Critical Parameters in these areas is essential to minimize Macro Voids**

Parameters Critical to Macro Void Generation

➤ Solder Paste

□ Solvent

- ✓ *Amount, Boiling Point, Volatility determine the amount of macro voids generated*
- ✓ *most solvents in the solder paste should evolve at temperatures below the solder alloy melting point to minimize macro-voids*

□ Volume printed on Land

- ✓ *Larger paste printed volume will result in more macro-voids due to more volume of solvents being present*

□ Solder Powder characteristics

- ✓ *More oxidized powder results in increased macro voids*

□ Flux

- ✓ *Higher activity and amount will result in faster, complete reduction of solder oxides which will enable macro voids formed by this reduction reaction more time to escape from the solder joint*

Parameters Critical to Macro Void Generation

(continued)

➤ Reflow Process

□ Profile

✓ Peak Reflow Temperature

- *Higher Temperature lowers solder surface tension and allows more `mobility` for macro voids which can lead to their escape from the solder joint*

✓ Time Above Liquidus

- *Longer liquidus time increases probability for escape of macro voids from the solder joint*

✓ Flux Activation Time (also called soak time)

- *Most of volatile chemical compounds in the solder paste are evolved during this period; hence the flux activation time needs to be sufficient for this evolution to happen*

Parameters Critical to Macro Void Generation

(continued)

➤ Reflow Process

□ Reflow Atmosphere

- ✓ Atmospheres with lower oxygen content produce less amount of oxidation of the solder surfaces during the reflow soldering process
- ✓ Less oxides will result in less macro voids since
 - a. *reduction of oxides creates water vapor which is one source of macro voids*
 - b. *lack of an oxide crust on the other surface of the balls when molten; this oxide crust can prevent voids from escaping from the molten ball during reflow soldering*

Parameters Critical to Macro Void Generation

(continued)

➤ PCB and Component

□ Surface Finish

- ✓ Co-deposited volatile organic compounds from surface finish plating operations will result in more macro voids

□ Land Size and Design (soldermask defined / metal defined)

□ Oxide Content of Solderable Surface

- ✓ Higher oxide content, typically copper oxides, will result in more macro voids

□ Contamination

- ✓ Contamination can increase amount of macro voids by
 - presenting a non-solderable surface on the lands which may keep macro voids attached to the lands and*
 - by generating volatile gases at soldering temperatures if the contamination decomposes*

Parameters Critical to Macro Void Generation

(continued)

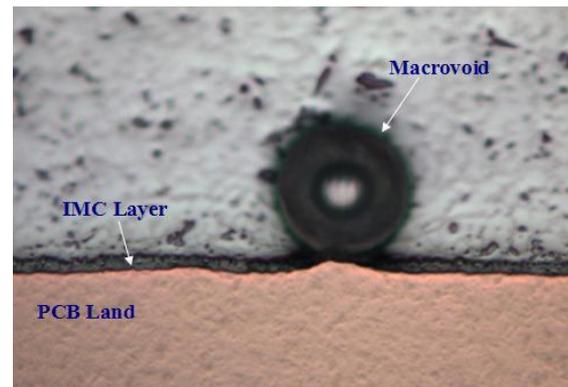
➤ General

❑ Ambient temperature and humidity conditions

- ✓ Excessive temperature and humidity causes oxidation of the solder paste particles and BGA balls
- ✓ Excessive oxidation on solder paste particles and BGA balls leads to excessive macro-voids when these oxides are reduced by the flux during reflow soldering

❑ Contamination during board assembly processes

- ✓ This leads to non-wettable patches on the PCB lands
- ✓ Macro voids form at those patches and get stuck at the board interface



PLANAR MICRO-VOIDS

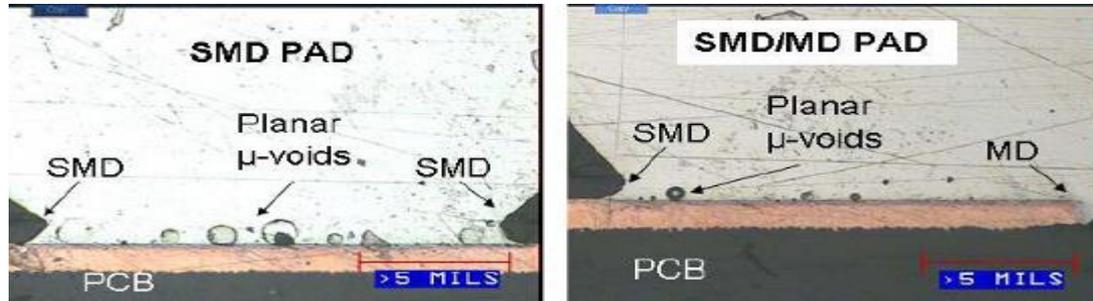
Description of Planar Micro Voids

- **Planar Microvoids are smaller than 1-2 mils in diameter**
- **Planar Microvoids are located in one plane at the Land-to-solder interface above the Intermetallic compound**
- **Planar Microvoids are a risk for reliability failures of BGA and other solder joints**

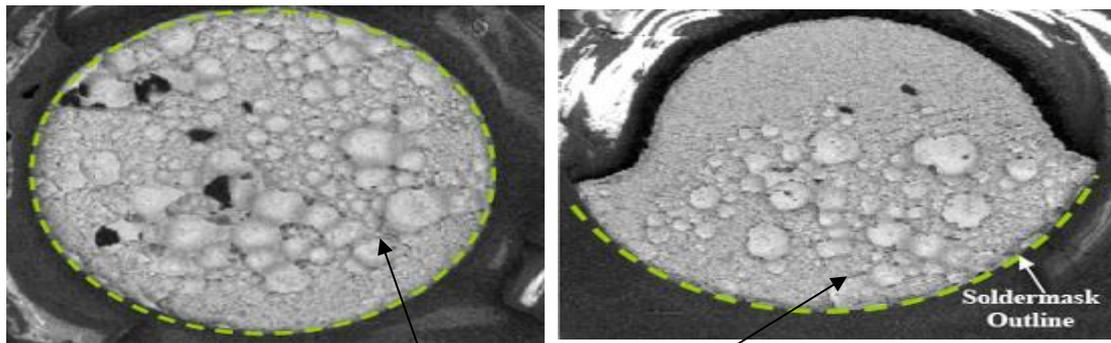


Detection of Micro Voids

- Cross-sectional Analysis



- Pull off solder joint from land



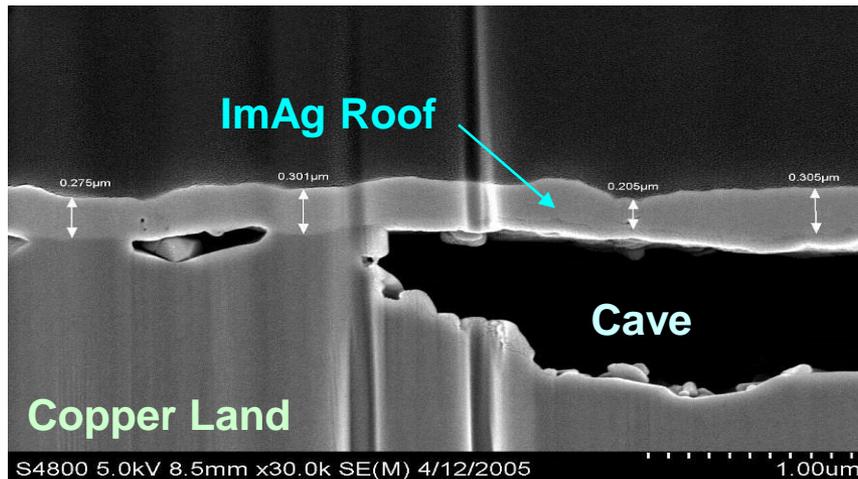
Micro voids

Characteristics of Planar Microvoids

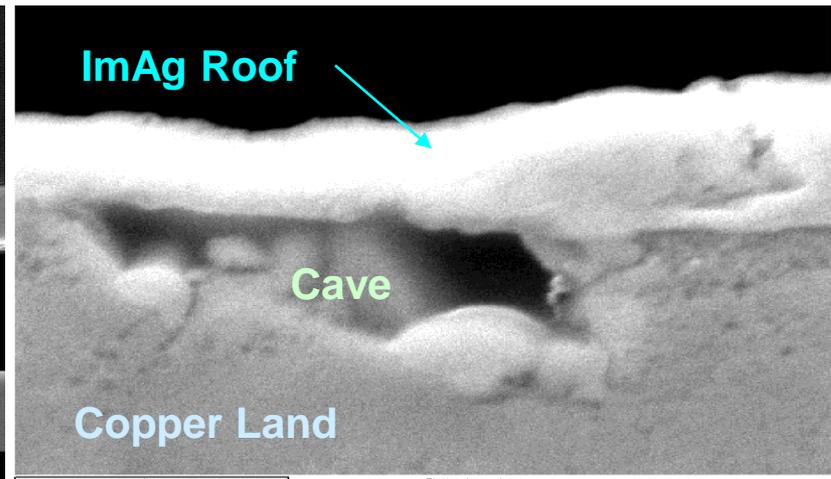
- Always occur at the land-to-solder joint Interface (PCB Land)
- Observed predominantly on ImAg surface finishes but also reported with other surface finishes (OSP, ENIG) in the industry
- Appear to be a PCB batch related phenomena
- More prevalent on soldermask defined lands (SMD)
 - *But also formed on metal defined lands (MD)*
- Does NOT cause yield loss
- But CAN be a reliability risk

Root Cause of Planar Microvoids

- Caves in the Copper of the PCB Lands under ImAg Surface Finish Plating on as-received PCBs



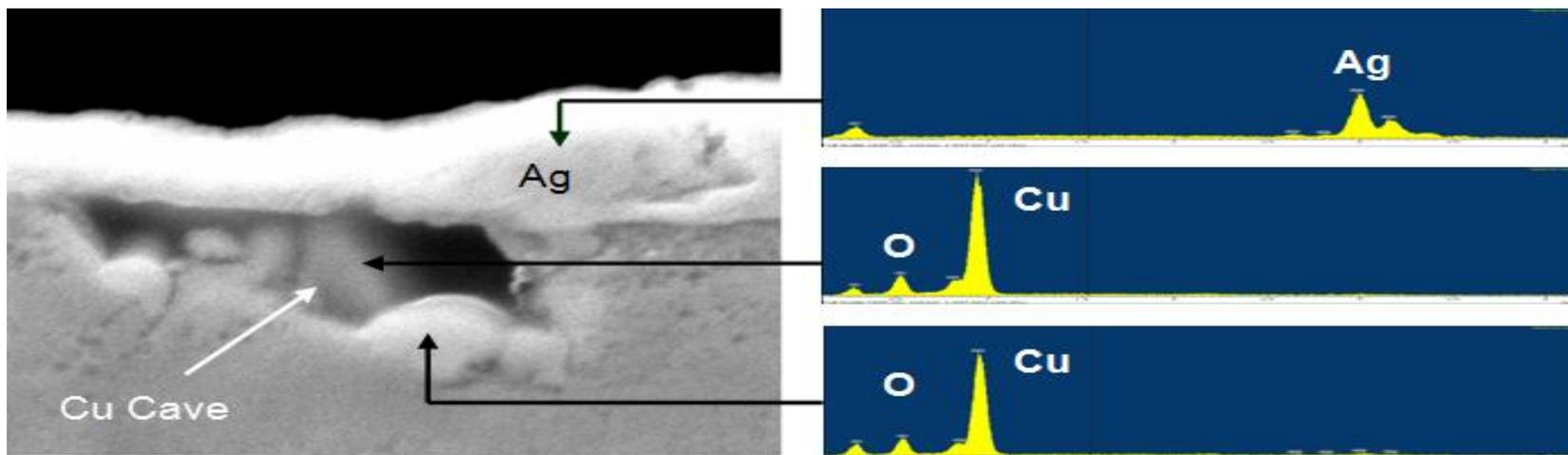
**SEM Photo of XS after FIB
(Focused Ion Beam)**



**SEM Photo of XS without FIB
(Conventional Mechanical Polish)**

- ✓ Strong correlation within a PCB lot between Caves in as-received bare boards that exhibited caves and boards that exhibited Planar microvoids after SMT assembly

PCB Cu Caves' Contents



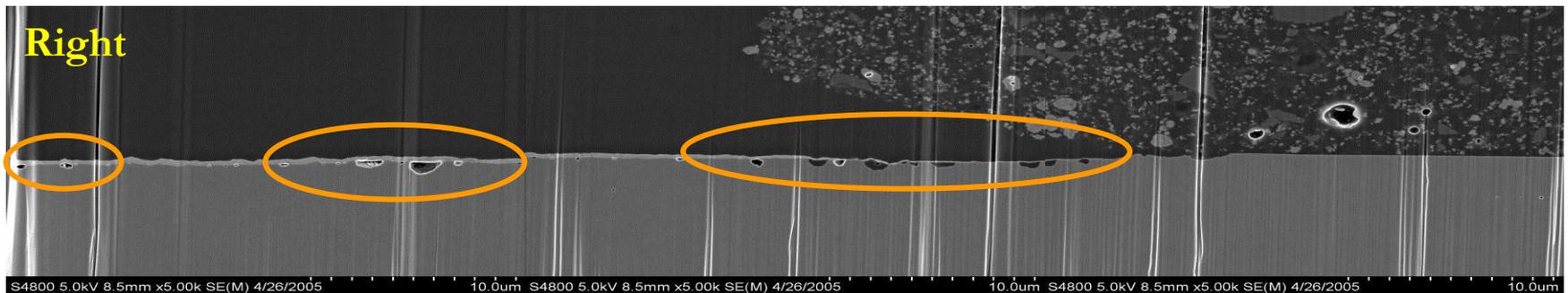
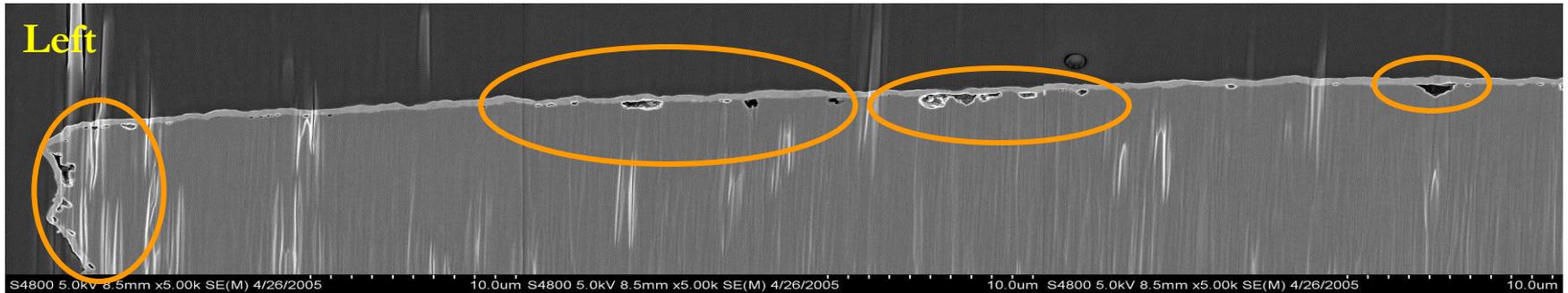
As- received PCB SEM XS View

EDS Spectra

- **Oxygen(O) was detected within the PCB Cu Caves on the walls and floor under a "roof" of ImAg Plating.**

More Micrographs Illustrating Presence of Caves under ImAg plating

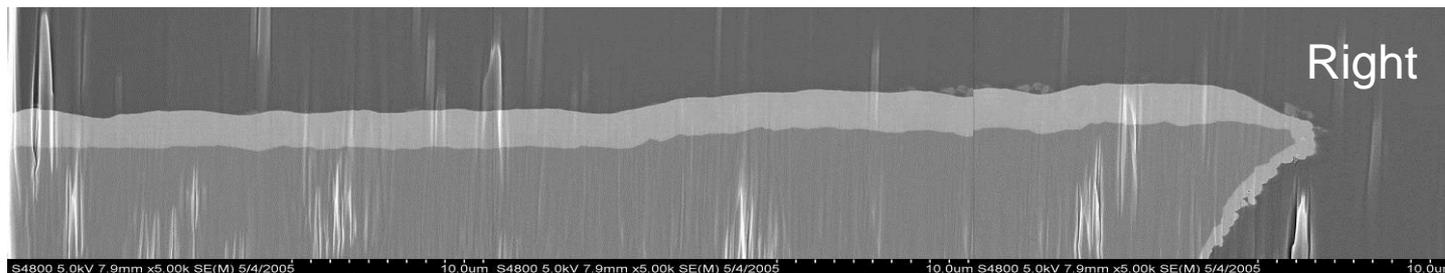
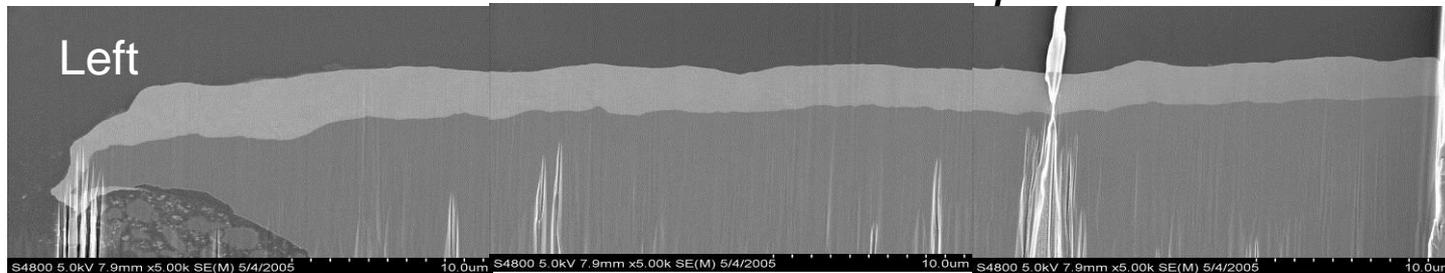
-- From the same BGA Land --



✓ **Many Caves Observed**

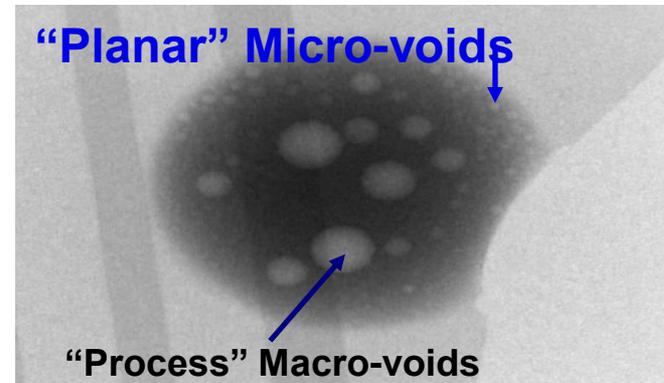
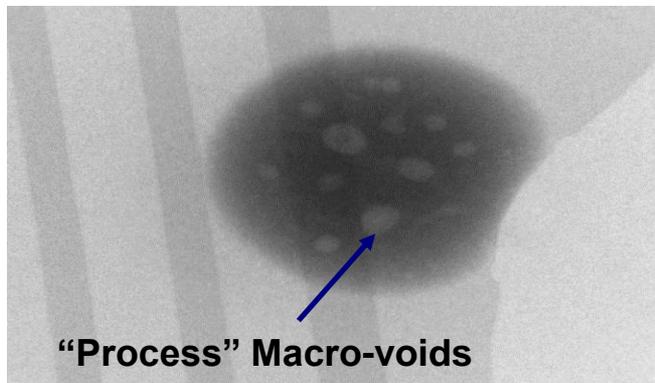
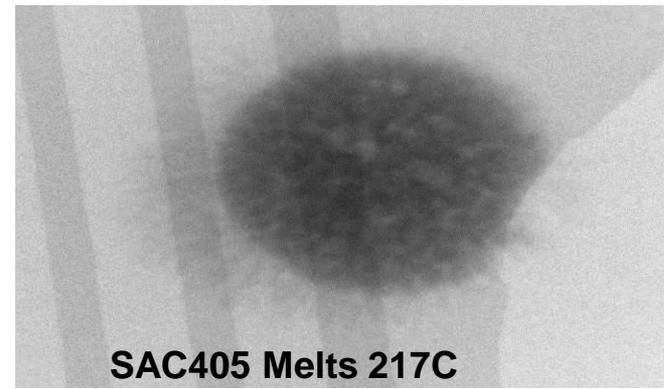
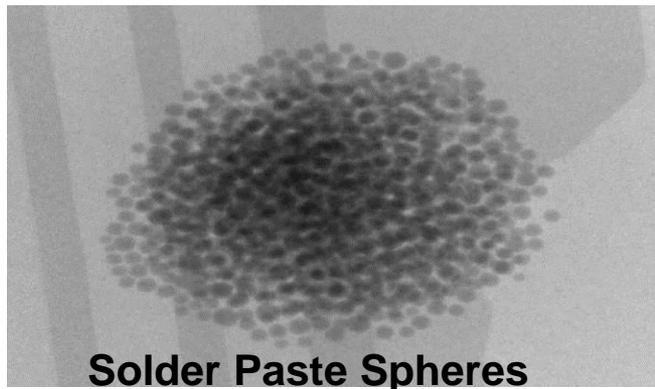
Micrographs showing Absence of Caves under ImAg plating

*From the same BGA Land,
but different board lot from one in previous slide*



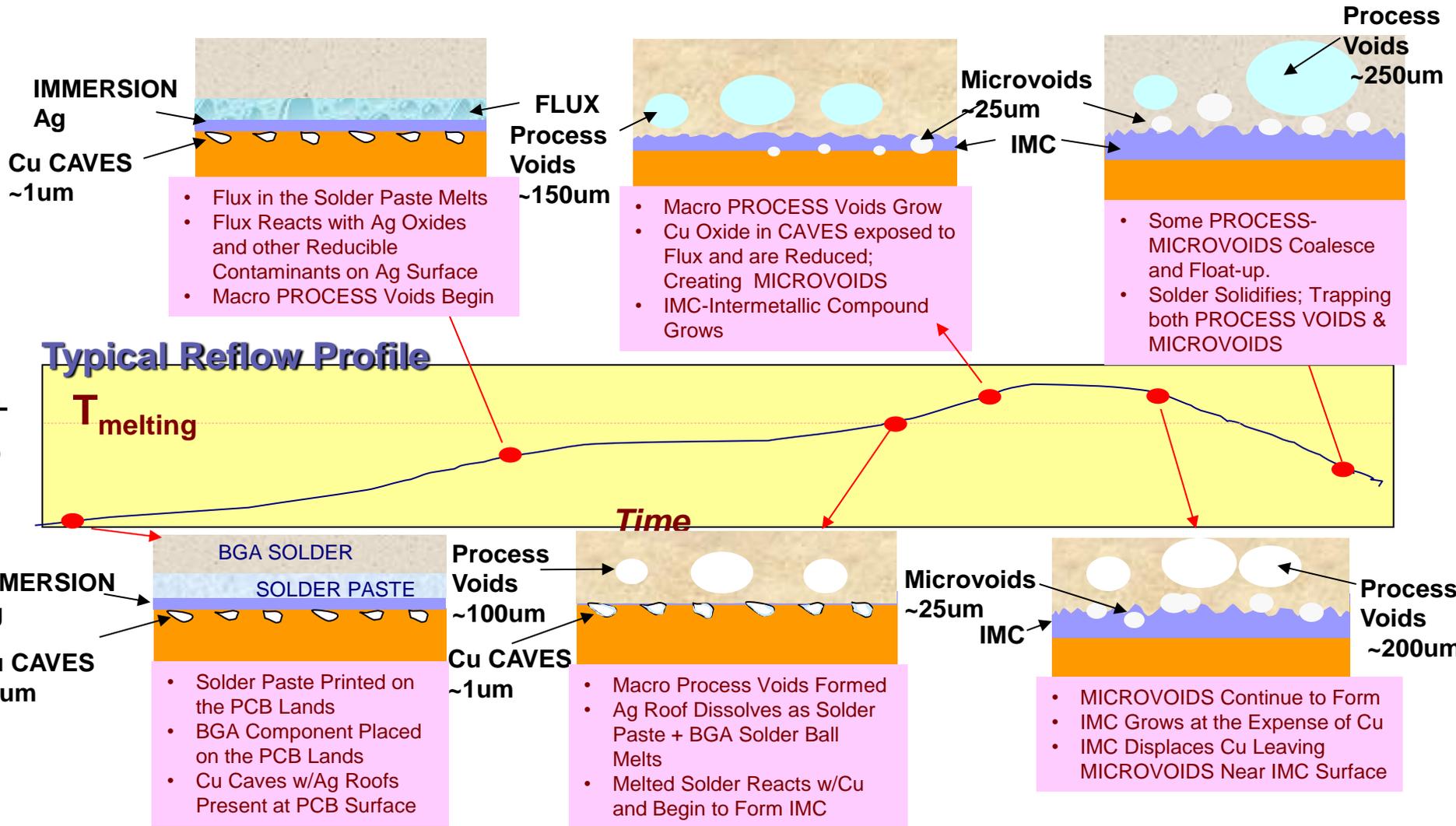
✓ **No Caves Observed**

IN-SITU THERMAL X-RAY IMAGING

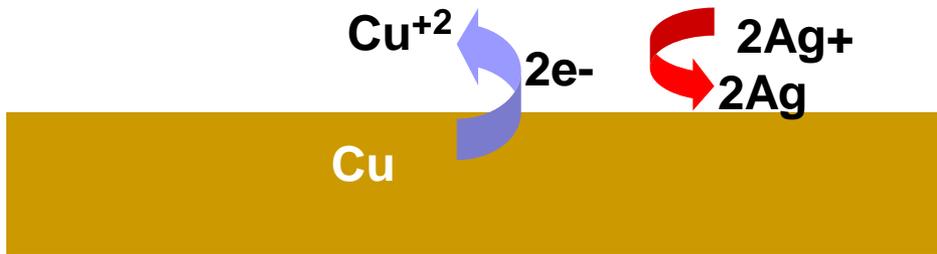


➤ Planar Micro-voids form ~10 s after Process Macro-voids form

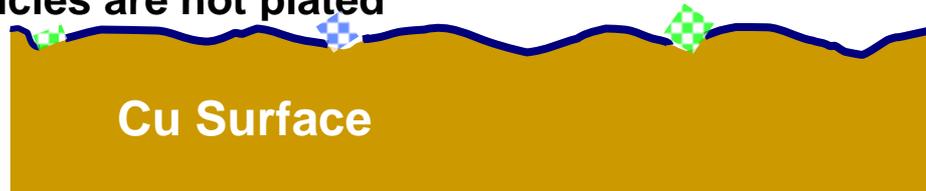
CAVES TO MICROVOIDS FORMATION MECHANISM



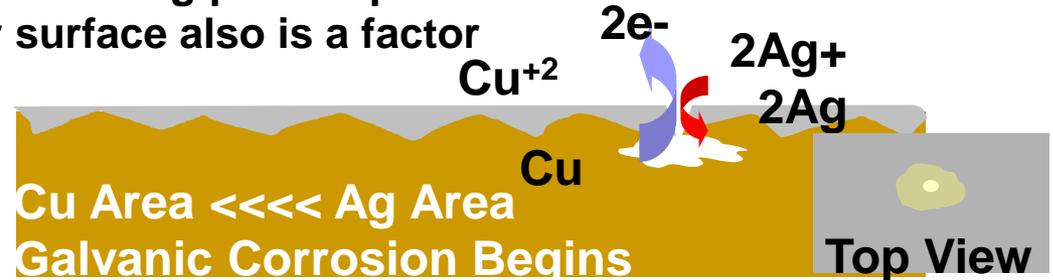
A Hypothesis for Cave Formation -- Galvanic Corrosion --



When ImAg plating starts, areas with SM residue or particles are not plated

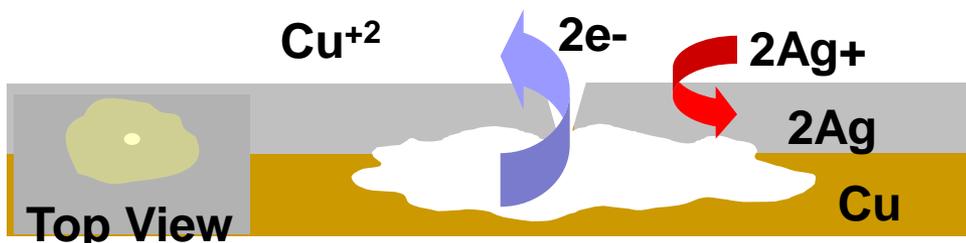


Ag deposits around SM or particle Ag pore or pinhole forms; roughness of copper surface also is a factor

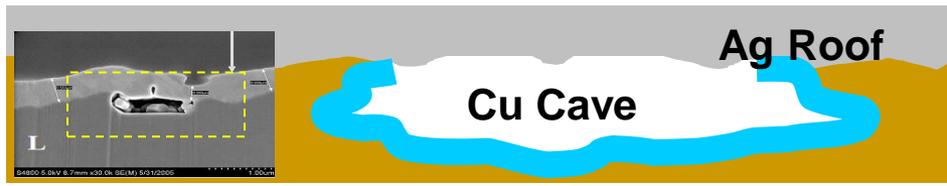


Cave under ImAg

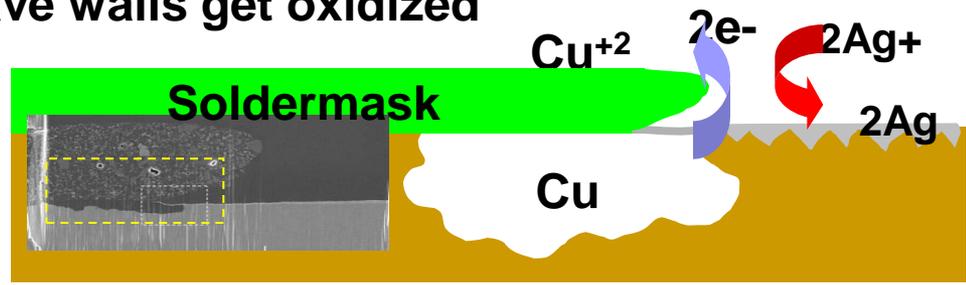
A Hypothesis for Cave Formation -- Galvanic Corrosion --



Top View
Ag deposition & Ag build-up continues



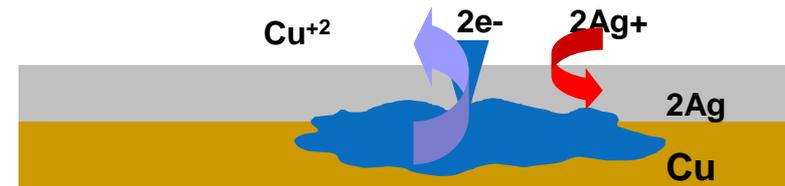
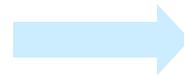
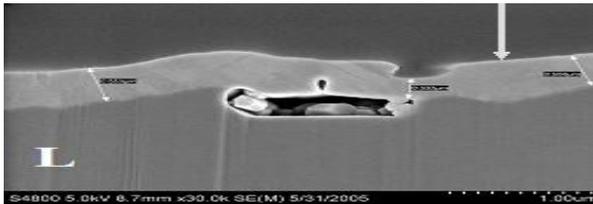
After 1mAg, Cu cave walls get oxidized



Soldermask edge-crevice effect

Mitigating Planar Microvoids

- ✓ Copper Caves result from Excessive Galvanic Corrosion



- ✓ Excessive Galvanic Corrosion results from a complex interaction of

- PCB Cu surface condition,
- PCB geometric design

- ✓ Hence,

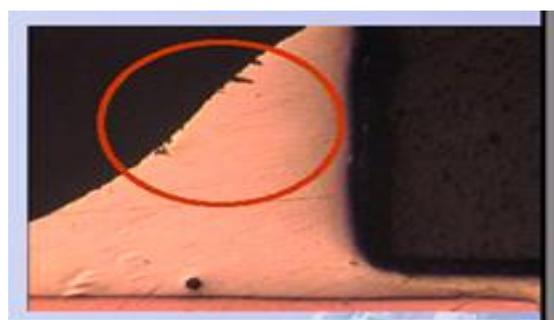
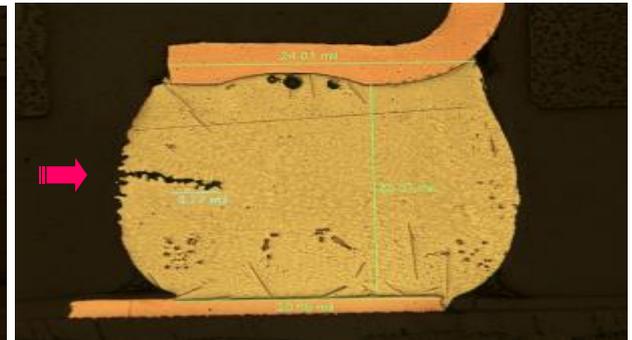
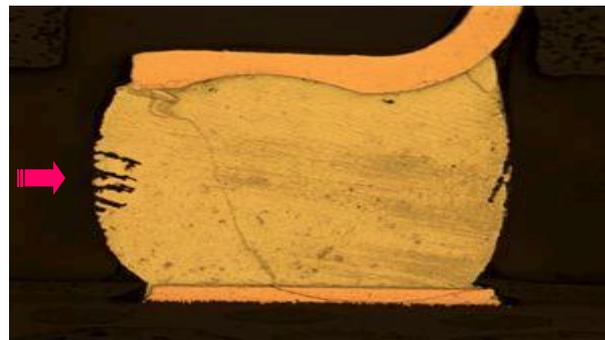
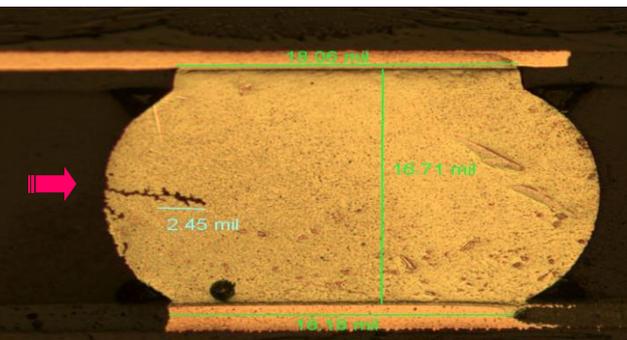
- Proper Micro-etch and Plating Chemistry by the Chemistry Supplier, and
- Strict Control of the Critical to Function Variables during the Plating Process at PCB Fabricator

are necessary to lower Risk of Planar Microvoids formation during SMT Assembly

SHRINKAGE VOIDS

Description of Shrinkage Voids

- Elongated, voids with rough, `dendritic` edges emanating from the surface of the solder joints
- These are seen not just in BGA solder joints, but also in Through Hole Solder Joints and chip component solder joints



Shrink Hole Void Characteristics

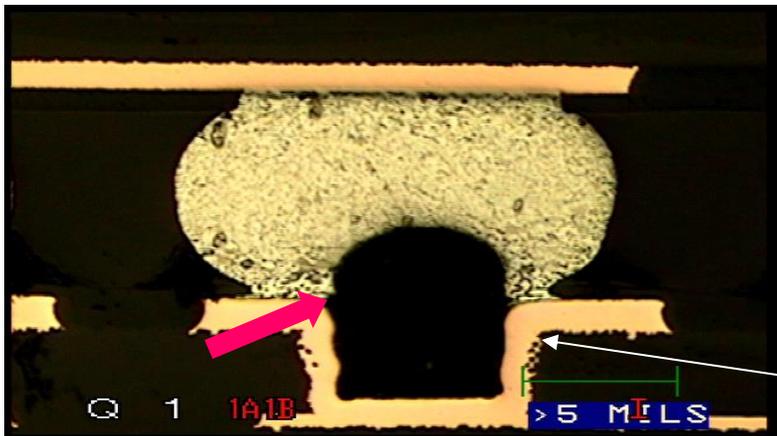
- Industry consensus is that solidification sequence of SAC solders causes shrink holes
- Slow Cooling of solder joints causes excessive shrinkage of the final eutectic solder phase just before solidification
- Disturbance to the solder joint while it is solidifying will increase amount and size of shrinkage voids
- Do not impact reliability
- Is not a `Crack` and does not continue to grow under thermo-mechanical stresses
- Also called `sink holes` and `hot tears`

✓ **Shrink Hole Voids are natural for SnAgCu solders, can be minimized**

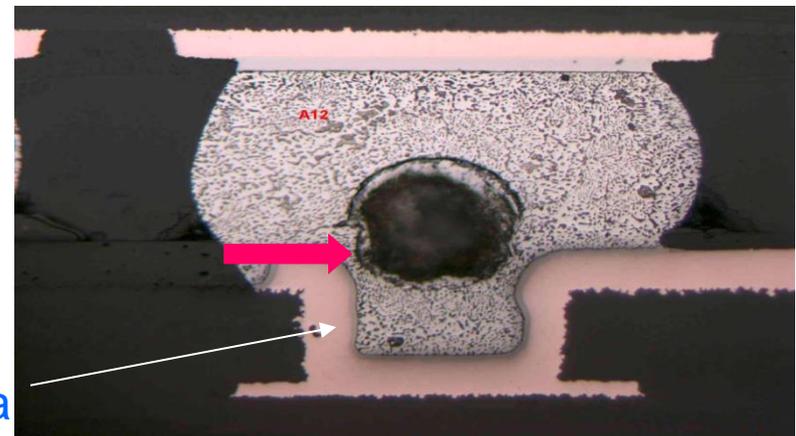
MICRO-VIA VOIDS

Micro-Via Voids

- Voids generated due to the presence of a microvia in the BGA land



MicroVia



- Molten solder has not wet the inside copper walls of the microvia

- Molten solder has wet the inside copper walls of the microvia but left a void above it

Diagrammatic Representation of Void Formation due to Microvias in BGA Lands

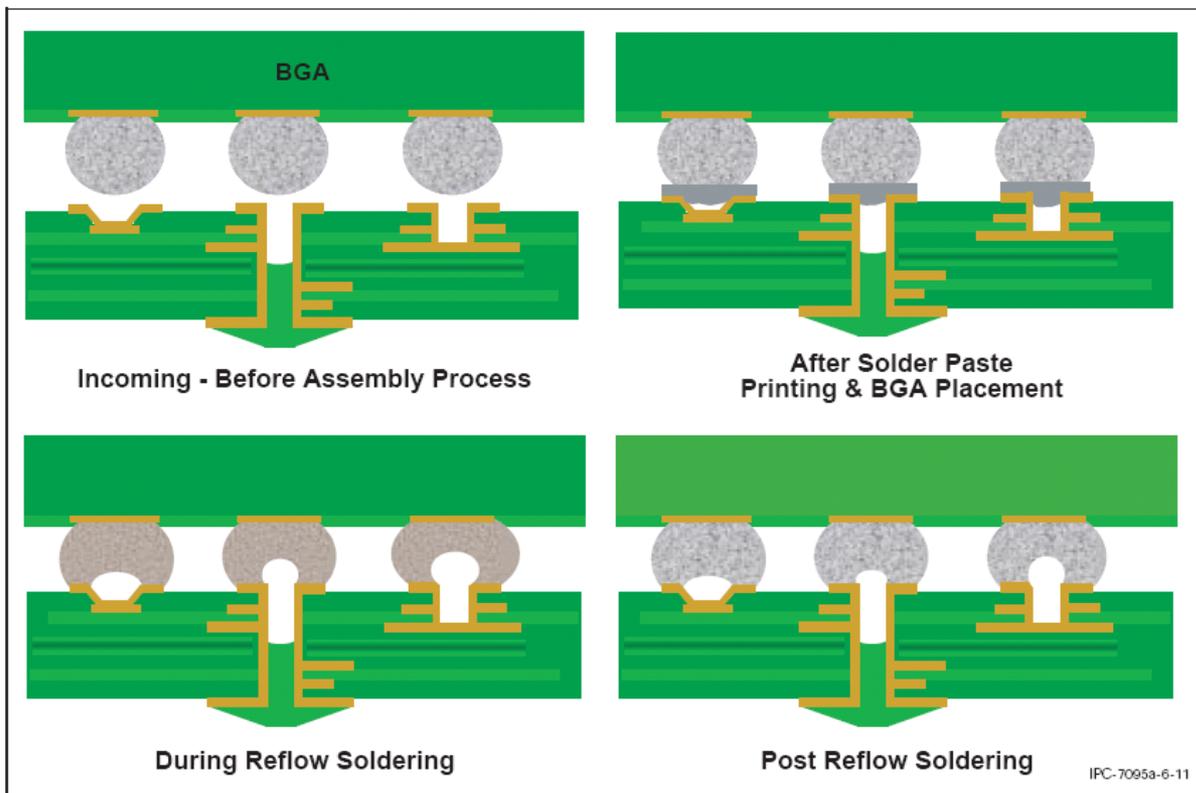


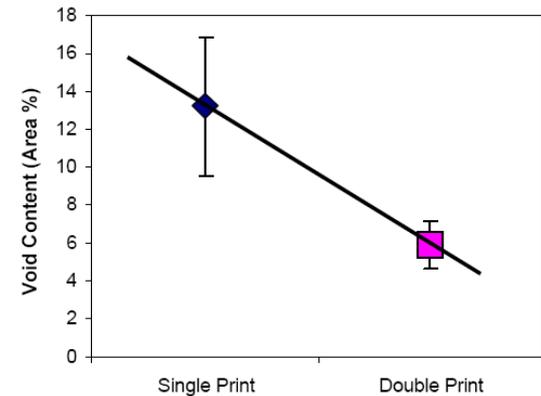
Figure 6-11 Via-In-Pad Process Descriptions

- ✓ Gases are evolved in the microvia during reflow soldering
 - *air from within microvia*
 - *Water vapor from solder oxide reduction reaction*
 - *Other volatile compounds from the solder paste*
 - *Organic chemicals in the microvia plating or from improper cleaning after plating*
- ✓ These gases are entrapped within the microvia since they have no easy pathway for escaping from the solder joint

Effect of Materials and Process Parameters on Micro-Via Voids

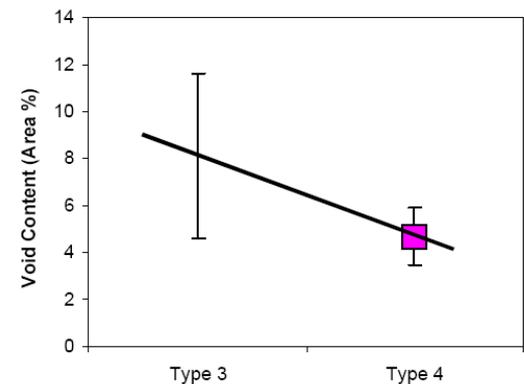
□ Printing Passes...Single vs Double

- ✓ Double Printing reduces voids by better filling of the micro-via



□ Solder Particle size of Solder Paste...Type 3 vs Type 4

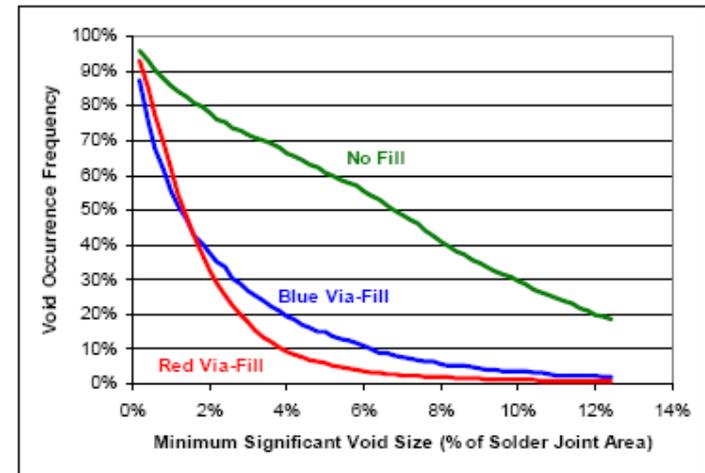
- ✓ Type 4 powder size (smaller) is better since it enables better filling of the via hole during printing



Source: *Voiding of Lead-Free Soldering at Microvia*, Dr. Ning-Cheng Lee, et.al., Indium Corporation of America

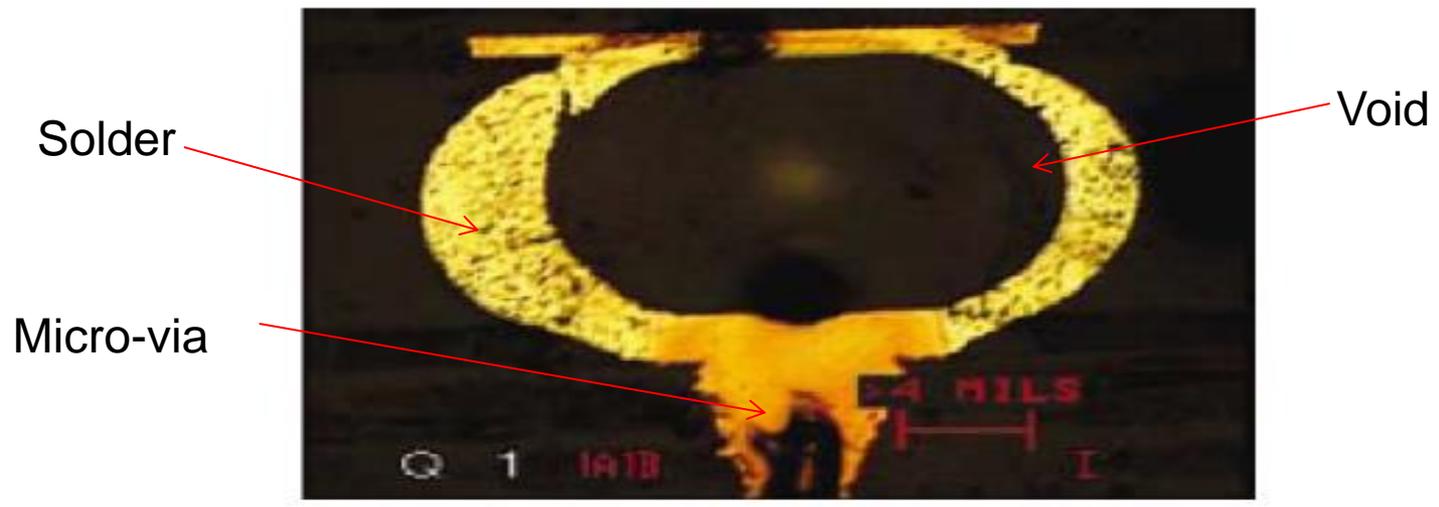
Effect of Materials and Process Parameters on Micro-Via Voids

- ❑ Plating Micro-Vias partially or fully with copper during PCB fabrication process
 - ✓ Pocket for air or gas entrapment is reduced or eliminated
 - ✓ Type of plating chemistry (red vs blue) is important



Source: *The Effect Of Via-in-pad Via-fill On Solder Joint Void Formation*, Adam Singer et al., Cookson Electronics

Solder Joint Failure due to Huge Micro-via Void



✓ Improper Plating resulted in severe out gassing from Micro-via to cause the huge void

Recommendations for Mitigating Micro-Via Voids

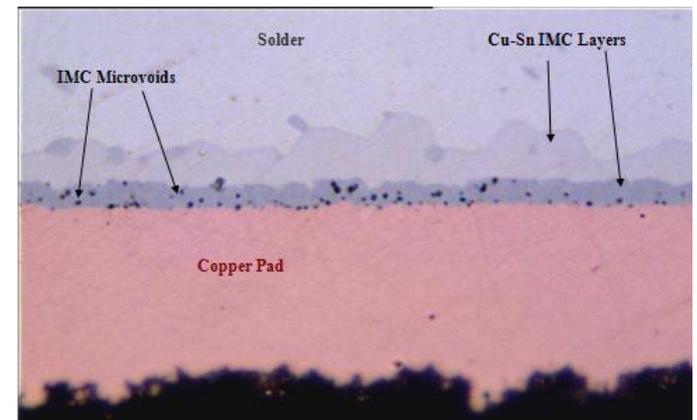
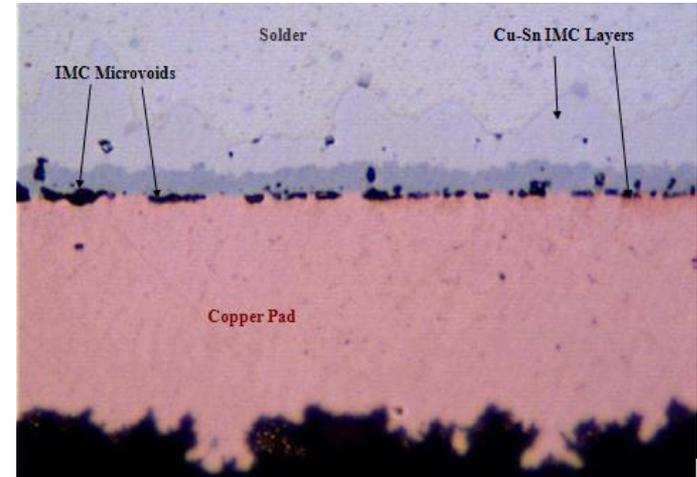
- **When microvias are incorporated into the design of Product boards, the recommendation is**
 - **Quantify micro-via voids' number and size by X-ray Analysis or X-section**
 - **If risk on Solder Joint reliability is high, explore ways to reduce by following techniques**
 - ❖ **Double printing**
 - ❖ **Increasing microvia diameter**
 - ❖ **Plating microvias shut**

IMC

MICRO-VOIDS

Description of IMC Microvoids

- **Sub-micron size voids**
- **Located either at the interface between the IMC and copper land or within the IMC**
- **Formed after samples have been exposed to elevated temperatures (>100C) for extended period of time (>48 hours)**
 - *High temperature aging*
 - *Temperature Cycling*
- **Independent of surface finish on the lands**
- **Observed for SAC solder joints and eutectic SnPb solder joints**
- **Observed on 10-15% of board lots**
- **Absent on high purity electrodeposited copper foils**



Source of Photos: D.W. Henderson, et al., "What the Electronics Industry Missed for 80 Years ... Interfacial Void Formation in Solder Joints with Cu Pad Structures during Thermal Aging", Presentation at TMS 2006 Lead Free Workshop, San Antonio, TX, March 2006

✓ **IMC Microvoids are a Reliability Risk**

Root Cause of IMC Microvoids

- **A few Hypothesis Proposed and rejected**
 - *Kirkendall Voids, due to difference in diffusion rates of the copper and tin atoms within the IMCs*
 - *Vacancy coalescence due to super saturation*
 - *Gas formation from the additives used in copper plating, as these additives are uncovered when the IMC is formed*
 - *Presence of Nickel or Bismuth at the solder-copper land interface or within the solder*

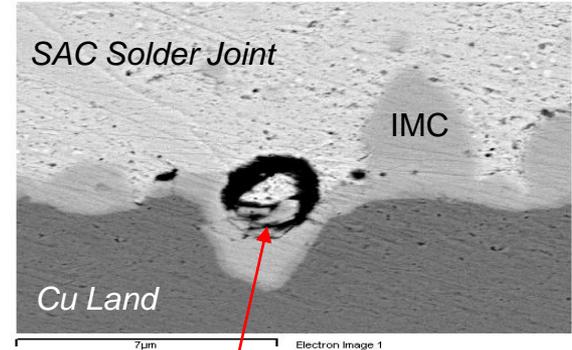
- ✓ **Prevailing Hypothesis in Industry: Organic impurities incorporated in the Cu during electroplating (proposed by Borgesen & Yin)**

✓ **Proper Copper Plating Process Chemistries and Process Control during PCB fabrication are necessary to avoid formation of IMC Microvoids**

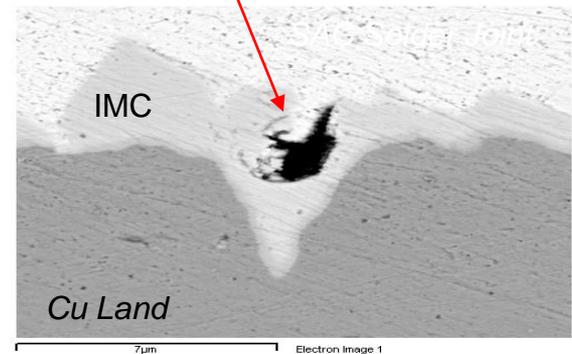
PINHOLE VOIDS

Pinhole Microvoids Characteristics

- **Size:**
 - 1 to 3 microns in diameter
- **Location:**
 - within the IMC
 - between IMC and the PCB Cu land
 - sometimes just above the IMC in the solder
- **Solder Metallurgy**
 - Independent of solder Metallurgy
 - Seen in both eutectic SnPb and SAC solder joints

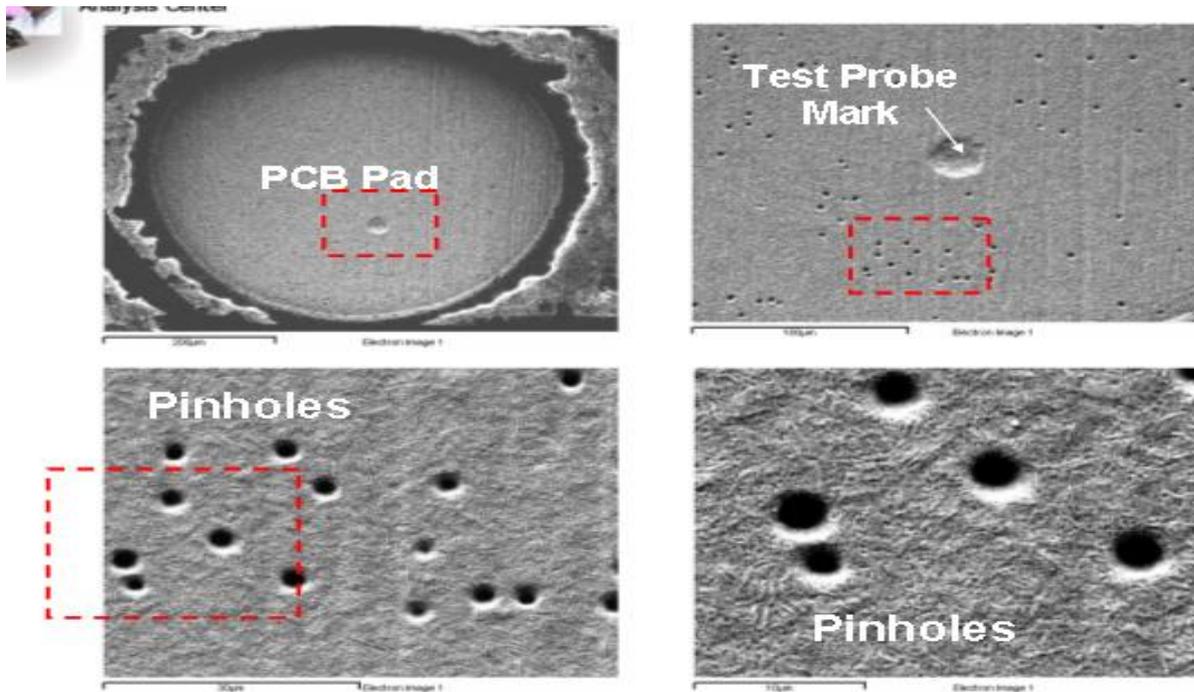


Pinhole Microvoids



Pinholes in PCB Lands

- Appearance of Pinholes in SMT lands on incoming PCBs

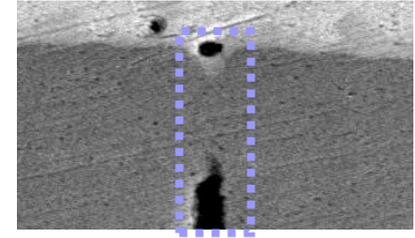
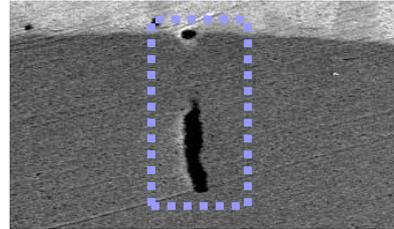


✓ Need high powered Optical Microscope to clearly seen these Pinholes

Root Cause of Pinhole Microvoids

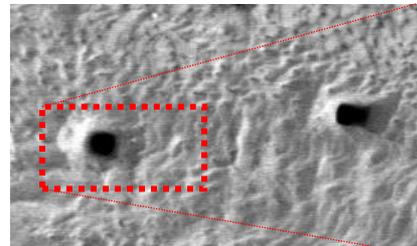
(continued)

- Pinholes were associated with crevasses in the copper land as seen in Cross-sections of Assembled PCBs

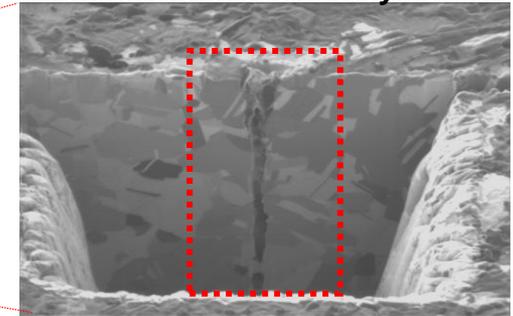


- Further material Analysis using Focused Ion Beam (FIB) milling indicated direct connection between pin holes and deep crevasses on un-assembled PCBs

Pinholes in Bare Board PCB



After FIB milling in middle of Pin Hole & Picture taken by 45° Tilt

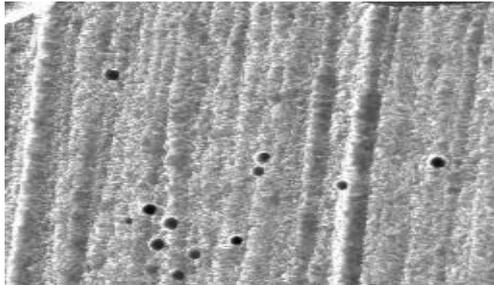


✓ Entrapped air and Process chemicals evolve from the pin holes during reflow soldering to cause the Pinhole Microvoids in and around the IMC

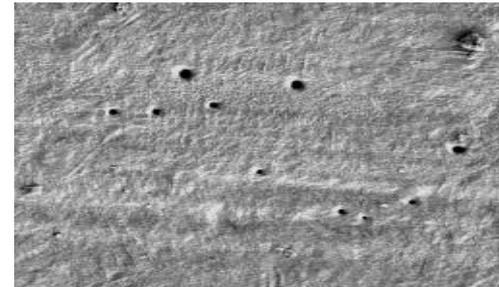
What caused these Pinholes?

- **Pinholes are NOT unique to any particular surface finish**
 - Seen on OSP and ImAg surface finish lands

Pinholes in OSP Coated PCB land



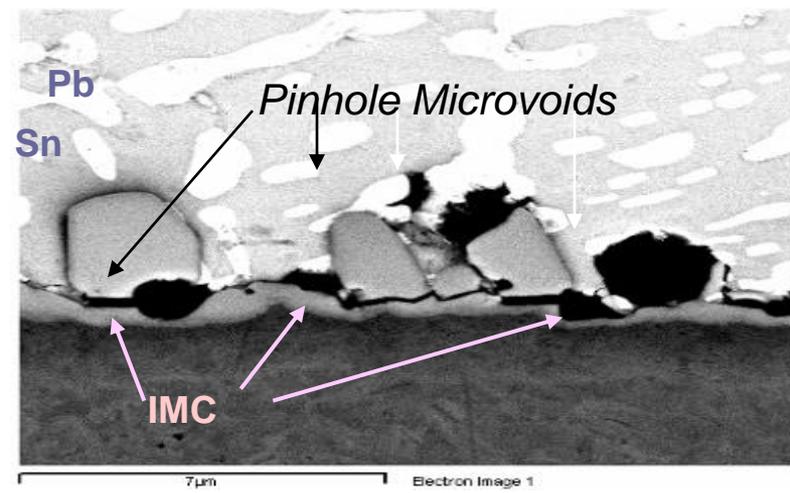
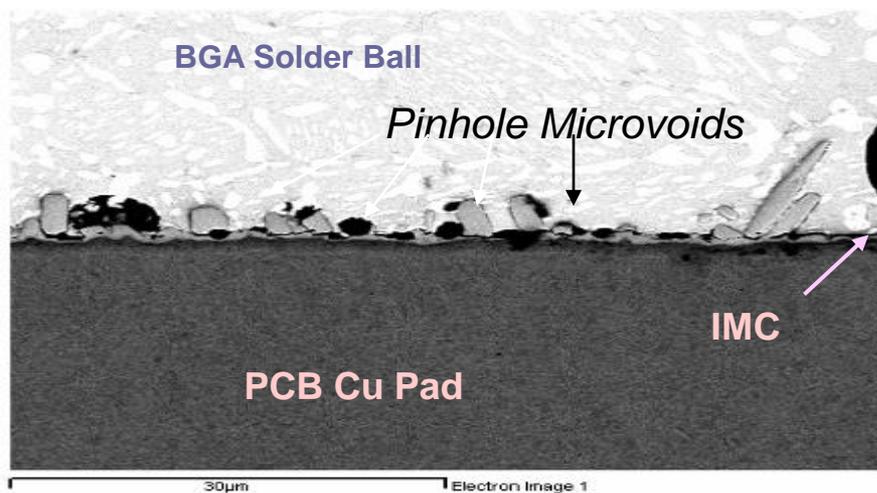
Pinholes in ImAg Plated PCB land



- **Primary Cause of Pin holes is Excursion in the Copper Plating Process during PCB fabrication**
 - *Deep Crevasses in the land are clear evidence of this*

✓ **Proper Copper Plating Process Chemistries and Process Control during PCB fabrication are necessary to avoid formation of Pinhole Microvoids**

Reliability Risks of Pinhole Voids

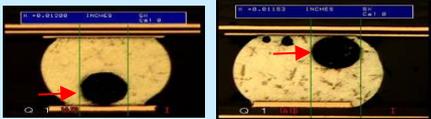
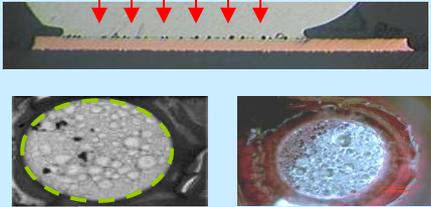
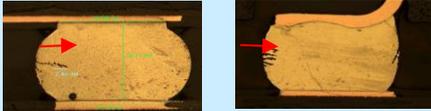
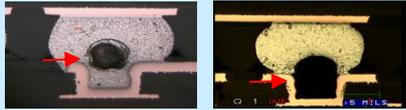
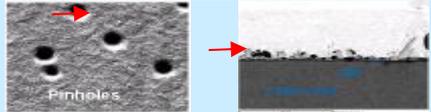
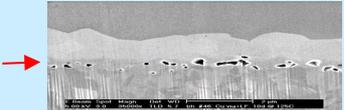


- Pin Hole Voids are located within or just above IMC layer
- This is the region in this solder joint where cracks propagate when boards subjected to thermo-mechanical and mechanical stresses

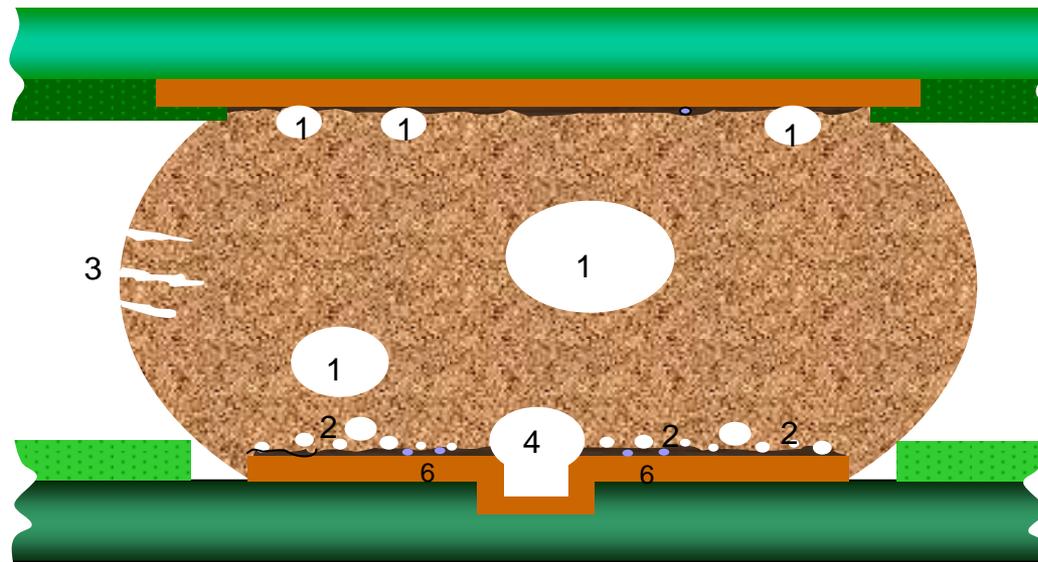
✓ Pinhole Voids are a Reliability Risk

Summary

-- Types of Voids in Solder Joints --

Type of Voids	Description	Photos
Macro Voids	Voids generated by the evolution of volatile ingredients of the fluxes within the solder paste; typically 4 to 12 mils (100 to 300 μm) in diameter, these are usually found anywhere in the solder joint; IPC's 30% max area spec requirement is targeted toward process voids; Sometimes referred to as "Process" voids. Includes Inclusion and Exclusion voids.	
Planar Micro Voids	Voids smaller than 1 mil (25 μm) in diameter, generally found at the solder to land interfaces in one plane; though recent occurrence on Immersion Silver surface finish has been highlighted these voids are also seen on ENIG and OSP surface finishes; cause is believed to be due to anomalies in the surface finish application process but root cause has not been unequivocally determined. Also called "champagne" voids	
Shrinkage Voids	Though not technically voids, these are linear cracks, with rough, `dendritic` edges emanating from the surface of the solder joints; caused by the solidification sequence of SAC solders and hence, unique to LF solder joints; also called sink holes and hot tears	
Micro-Via Voids	4 mil (100 μm) and more in diameter caused by microvias in lands; these voids are excluded from 25% by area IPC spec; NOT unique to LF solder joints	
Pinhole Microvoids	Micron sized voids located in the copper of PCB lands but also visible through the surface finish; Generated by excursions in the copper plating process at the board suppliers	
IMC Microvoids	Sub-micron voids located between the IMC and the Copper Land; Growth occurs at High Temperatures; Caused by Difference in Inter-diffusion rate between Cu and Sn. Also Known as Kirkendall Voids.	

Location of Voids in BGA Solder Joints after Reflow Soldering



- 1: Macrovoids
- 2: Planar Microvoids
- 3: Shrinkage Voids
- 4: Micro-Via Voids
- 5: IMC Microvoids
- 6: Pinhole Voids

Cu-IMC-Solder Interface after High Temp Aging



Sources For Root Causes of Various Types of Voids In Solder Joints

Types of Voids	Component Terminations / Balls	Solder Metallurgy	Solder Paste	SMT Reflow Soldering Process	PCB Land Design	PCB Fabrication materials /processes	Other
Process Voids	✓		✓	✓	✓	✓	Environmental Conditions on Mfg Floor
Planar Microvoids						✓	
Shrinkage Voids		✓		✓			Physical Disturbance to Solder Joints during solidification
Microvia Voids			✓	✓	✓	✓	
Pin hole Voids						✓	
IMC Microvoids						✓	Aging of Board assemblies

Parting Quotes for Voids Impact

- **What you see may not hurt you, what you do not see will hurt you**
 - Macro Voids observed in X-ray Images may not cause any significant reliability impact, but microvoids which cannot be seen in X-ray images will deleteriously impact reliability
- **Size may not matter**
 - Large voids away from the solder joint to land interfaces do not impair the solder joint strength reliability; small voids at the interfaces are can be `zipped` through once a crack starts
- **Location, Location, Location**
 - Location of voids within the solder joint is as much if not more important than void size

Questions

