

Via Fill and Through Hole Plating Process with Enhanced TH Microdistribution

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Abstract

The increased demand for electronic devices in recent years has led to an extensive research in the field to meet the requirements of the industry. Electrolytic copper has been an important technology in the fabrication of PCBs and semiconductors. Aqueous sulfuric acid baths are explored for filling or building up with copper structures like blind micro vias (BMV), trenches, through holes (TH), and pillar bumps. As circuit miniaturization continues, developing a process that simultaneously fills vias and plates TH with various sizes and aspect ratios, while minimizing the surface copper thickness is critical. Filling BMV and plating TH at the same time, presents great difficulties for the PCB manufactures. The conventional copper plating processes that provide good via fill and leveling of the deposit tend to worsen the throwing power (TP) of the electroplating bath. TP is defined as the ratio of the deposit copper thickness in the center of the through hole to its thickness at the surface.

In this paper an optimization of recently developed innovative, one step acid copper plating technology for filling vias with a minimal surface thickness and plating through holes is presented. The direct current (DC) process is studied in a wide variety of conditions to collect information on its capabilities. The plating conditions allowing improved micro-distribution for the plated TH are discussed. Boards with various thicknesses and TH aspect ratios are included in this study. The responses included TP min., TP knee, via dimple and cavity formation. A strong interaction between brightener and leveler concentrations was found. The results obtained allow for enhancing through hole micro-distribution while filling a wide range of BMV sizes. The process is designed for a variety of equipment applications with insoluble anodes, including vertical continuous plating equipment. In addition, a modified formula for soluble anodes applications is described.

Filling of through via holes in core layers of HDI and IC substrates in a one-step DC process is also demonstrated. Through vias filled with <5 microns or zero dimple and no voids or defects are shown. Mechanical properties, tensile strength => 42,000 psi, elongation > 20% as well as the thermal resistance of copper deposits met and exceeded the IPC standards thus satisfying the need of a highly reliable copper electroplating process.

Key words: Copper electroplating, PCB metallization, TH plating, via fill.

Introduction

Electroplating copper solutions are used in many industrial applications, such as anticorrosion and decorative coatings, and in the electronics industry for manufacturing of electronic devices. Aqueous sulfuric acid copper baths are particularly useful for the fabrication of printed circuit boards (PCB) and semiconductors. Copper, having better electrical conductivity than any metal except silver, is the metal of choice since copper metallization allows for smaller features application. Interconnect features are features such as blind micro vias (BMV), trenches, and through holes that are formed in a dielectric substrate. They are metallized, preferably with copper, to render the interconnect electrically conductive. During circuit fabrication, copper is electroplated over selected portions of the surface of the printed circuit board, into blind vias and trenches and onto the walls of through holes passing between the surfaces of the circuit board base material. The walls of the through holes are metallized to provide conductivity between the circuit layers of the printed circuit board. The conductive deposits should be of a uniform plating thickness. Vias and trenches provide conductive connections between circuit board inner layers. For semiconductor fabrication, copper is electrodeposited over a surface of a wafer with various features such as vias and trenches. Copper filled vias and trenches ensure a good conductivity between the semiconductor

device layers. Thus, in many printed circuit board and semiconductor fabrication processes, electroplating has been adopted by industry as the primary deposition means for copper metallization. [1-2].

The trend of portability combined with increased functionality of electronic devices has driven the miniaturization of PCBs. Smaller device sizes and increased circuit density require decreasing the dimensions of interconnect features and increasing their density. The conventional multilayer PCBs with through-hole interconnects are not always the optimal solution. Sequential build up technologies, which utilize blind vias have been developed for high density interconnects. Maximizing of via filling, while minimizing the surface copper thickness and deposit thickness variation presents difficulties for the manufacturers, especially when the PCBs contain both through holes and BMVs. It is mostly desirable to obtain a good throwing power in electrodeposition processes. Particularly in the through hole plating of PCBs, a uniform distribution of deposited copper is demanded including inside the holes on hole walls. In general, copper plating processes that provide good via fill and better leveling of the deposit across the substrate surface tend to worsen the throwing power of the electroplating bath. In the fabrication of reliable PCBs, via filling and plating through holes (PTH) with various aspect ratios at the same time, in the same electrolyte is highly challenging for the manufacturers.

The purpose of this work was to optimize a recently developed innovative copper process for simultaneously filling vias and plating through holes (TH) with a minimal surface thickness. The process was evaluated in a wide variety of conditions to collect information on its capabilities. The effect of inorganic components and organic additives concentrations and the influence of the plating parameters on the plating process performance in terms of throwing power and via filling were determined. A series of copper electroplating solutions were evaluated. THs with various diameters / aspect ratios in boards up to 1.6mm thick were measured.

Insoluble and soluble anodes applications were considered. Filling of through via holes in core layers of HDI and IC substrates in a one-step DC process was also studied. Panel plating as well as pattern plating for vertical plating applications including vertical continuous plating (VCP) equipment were included in the experiments. The mechanical properties of plated copper deposits, Tensile Stress and Elongation were measured. The thermal characteristics were evaluated.

Acid Copper Plating Process

A typical copper plating solution contains copper sulfate, sulfuric acid, chloride ions, and organic additives that control the deposition process and the quality of the plated coatings [3-8]. Solutions that provide good via filling and leveling of the copper deposits usually are characterized with low polarization and presence of leveling agents. High copper, low acid base electrolytes (VMS) are used. The brighteners are adsorbed at low current density areas of the cathode surface, accelerating the process, while the levelers are adsorbed at the most negatively charged areas thus slowing the deposition rate there. On the other hand, high throwing power is achieved in low copper, high acid baths. The throwing power of an electroplating bath depends on solution conductivity, electrodeposition kinetics (the slope of the polarization curve, the higher the better TP min), cell geometry, and temperature.

The innovative plating process is an advanced, direct current acid copper system offering simultaneously via filling and through hole plating [9]. The plating is uniform over the cathode surface and no TH thin knee or “slope” is observed around the THs. Key features include filling BMV up to 5mils x 4mils with a low dimple size, any layer build up applications, as shown in Figure 1. Figure 2 shows a typical plating in the bath at 20 ASF. Surface copper thickness is 18 – 20 microns and the surface appearance is bright. The process is compatible with direct metallization or Electroless copper. The low organic (TOC) system has extremely long life and it is easily maintained, all organic additives are CVS analyzable.

Process Optimization

The capabilities of the innovative plating copper process for VF and THP were studied as a wide range of plating conditions were tested. Factors included were: organic additive concentrations, inorganic components concentrations, and plating parameters. Large ranges of the additive concentrations were tested:

Wetter: 5 – 15 ml/L, Brightener 0.5 – 4.5 ml/L and Leveler 5 - 25 ml/L.

Current density applied were 10, 20 and 30 ASF.

Optimization was performed in terms of enhancing TH Microdistribution, including for thicker panels, up to 1.6 mm (TH aspect ratios up to 6.4:1), via filling (minimal dimple size, void free filling), while keeping a low surface copper thickness. TH micro-distribution is given as throwing power min and TH corner plating is characterized by TP knee [9].

$TP_{min} = \text{Ave. Cu thickness in the through hole center} / \text{Ave. Cu surface thickness} \%$

$TP_{knee} = \text{Ave. Cu thickness at through hole corners} / \text{Ave. Cu surface thickness} \%$

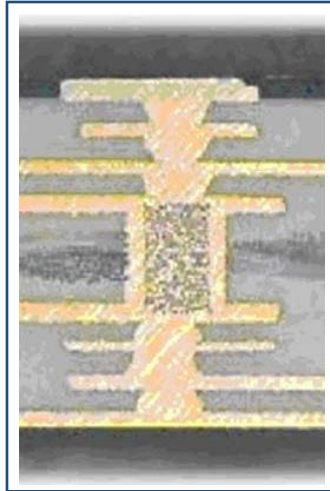


Figure 1 – Any Layer Build

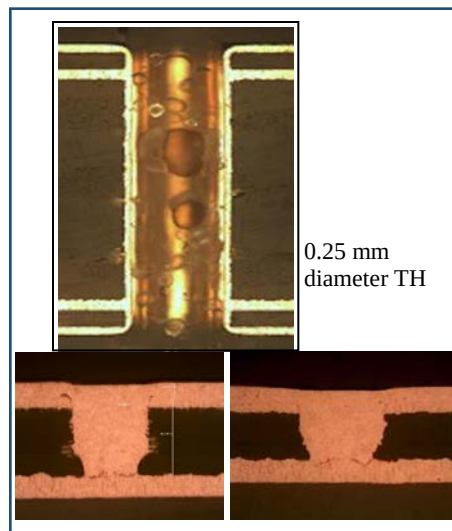


Figure 2 – Plating THs, 0.8mm thick panel and filling vias; 20 ASF, 60 minutes

Tests were completed in 8.5 liter cell, Figure 3 and 200 liter pilot tanks. Insoluble anodes were used. They allow for higher applicable current densities, easy maintenance and a uniform copper surface distribution. Each bath was made up, dummy plated for 2 Ah/L, analyzed, adjusted to correct additive levels, and then the test panel was plated. Each test panel went through a pre-clean cycle of 2 min acid cleaner, 2 min rinse, 2 min 10% sulfuric acid before the plating in the Process A bath.

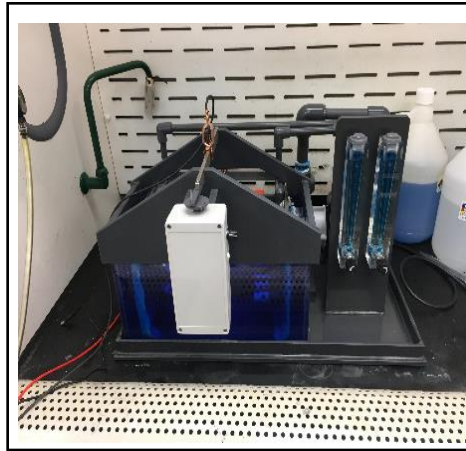


Figure 3 – Plating cell, 8.5 liters, “knife” agitation, eductor spray

Results and Discussion

Through Hole Plating: Concentration levels effect and CD influence on Throwing power.

Results shown are for a basic electrolyte (VMS) containing 250 g/L $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$, 50 g/L sulfuric acid and 45 – 50pp Cl⁻. Increase in brightener resulted in an increase in throw power. Wetter and leveler did not show a clear trend. When increasing current density, the throw power decreased in all cases. The tests showed that there was a strong interaction between the brightener and leveler concentrations in the electroplating bath.

Examples are given in Figures 4 and 5, TP min as a function of organic additive concentrations and CD.

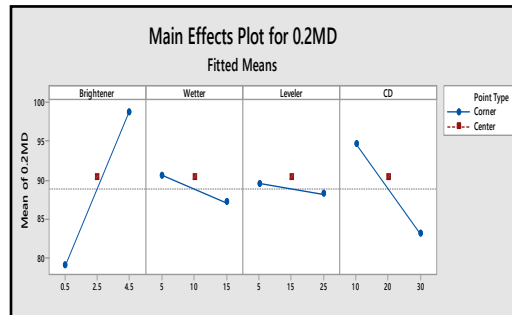


Figure 4 - Main Effect Plot, 0.20 mm diameter TH in 0.8mm thick panel

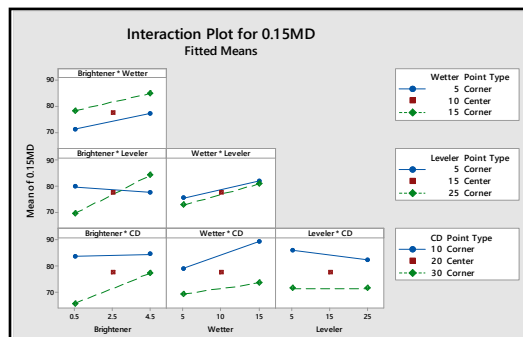


Figure 5 - Interaction Plot for 0.15 mm diameter TH in 0.8 mm panel, Aspect Ratio = 5.3

Via Fill: Concentration levels effect and CD influence on via dimple.

It was established that an increase in brightener concentration lead to an increase in dimple size. Wetter showed minimal effect on dimple depth. Leveler results are inconclusive, although in most of the cases increasing the leveler concentration

affected via filling, usually increasing via dimple. Increase in current density showed an increase of dimple size for 3x3 vias and a decrease in dimple size for larger size vias, Figures 6, Figure 7, and Figure 8.



Figure 6 - Main Effect Plot, 3x3 (75 μ m X 75 μ m) Via dimple as a function of Brightener, Wetter, Leveler and CD

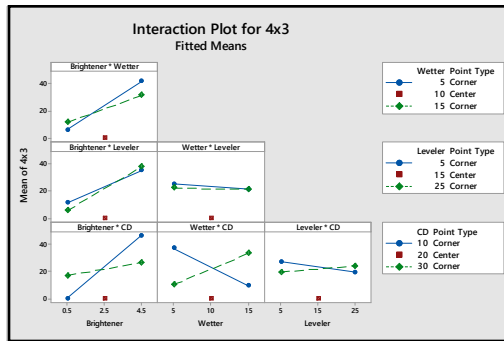


Figure 7. Interaction Plot for 4x3 (100 μ m x 75 μ m) vias

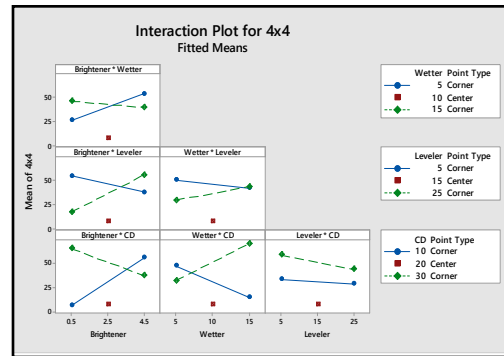


Figure 8. Interaction Plot for 4x4 (100 μ m x 100 μ m) vias

High concentration of the organic additives and 10 ASF showed the best plating results. The optimization model could minimize and maximize throwing power and via dimple size. Enhanced TH microdistribution was achieved under optimal conditions for maximum throwing power: high brightener and leveler concentrations, low CD, 10ASF. 30 ASF caused cavities in 3x3 and 4x4 vias in some cases. Experiments were designed to be run under the conditions of the minimum and maximum dimple size and minimum and maximum throwing power:

- Max dimple (no voids inside the vias) - 4.5ml/L Brightener, 5.0ml/L Wetter, 25.0ml/L Leveler, 10 ASF
- Max throw power - 4.5ml/L Brightener, 15.0ml/L Wetter, 25.0ml/L Leveler, 10 ASF
- Min dimple (no voids inside the vias) - 2.5ml/L Brightener, 10.0ml/L Wetter, 15.0ml/L Leveler, 20 ASF
- Min throw power - 0.5ml/L Brightener, 5.0ml/L Wetter, 25.0ml/L Leveler, 30 ASF

The minimum dimple condition shows a large improvement from maximum dimple conditions; large differentiation. Maximum throw power % showed improvement from the minimum condition, but not considerable; small differentiation, Figure 9.

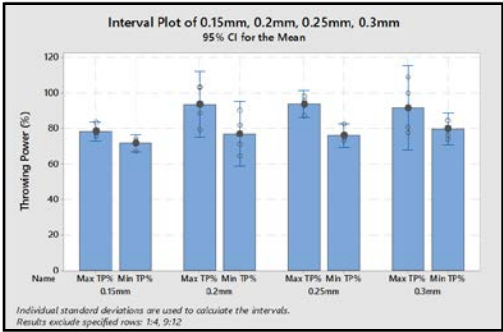


Figure 9 - Throwing power Interval Plot of various sizes THs at min TP% and max TP% conditions

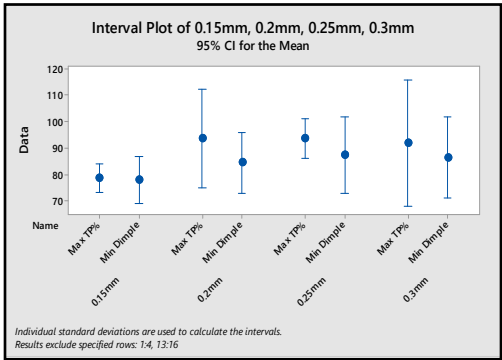


Figure 10 - Throwing power Interval Plot of various sizes THs at optimum conditions

Comparing maximum throw power and minimum dimple conditions (2 ideal conditions) resulted in a better tradeoff by targeting minimal dimple. Throwing power varies much less between the maximum TP condition and minimum dimple condition, Figure 10, than dimple size between the two conditions, Figure 11. The throwing power was reduced slightly when run at optimized dimple conditions (minimum dimple). If dimple size and throwing power are critical, the best compromise is to run under optimized dimple conditions.

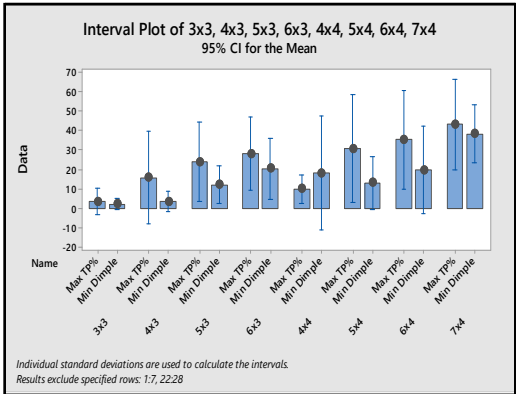


Figure 11 – Via dimple Interval Plot of various sizes vias at optimum conditions

Throwing power and knee thickness increases as the TH aspect ratio decreases /diameter increases, as shown for the 0.8 mm thick panel in Figure 12.

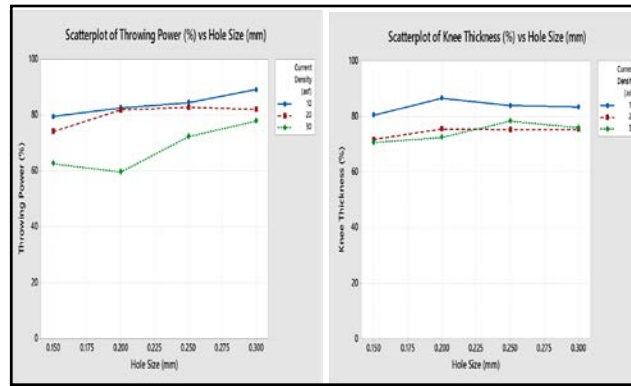


Figure 12 – TP_{min} and TP_{knee} as a function of hole diameter

The industry specification for a throwing power $\Rightarrow$ 75% and knee thickness $\Rightarrow$ 75%, could be achieved under proper plating conditions for all sizes THs (0.15, 0.20, 0.25, and 0.30 mm), Aspect Ratios of up to 5:1 in 0.8mm or thinner (0.4mm) panels. However the throwing power for thicker panels (1.2 - 1.6 mm) was measured to be below 75%. It usually was about 55% – 59% for 0.25 mm holes in 1.6 mm panels, AR = 6.4.

Basic copper electrolyte (VMS) in Terms of Enhanced Throwing Power

In an effort to improve the throwing power for thicker boards, the inorganic component concentrations in the bath were varied, reducing copper ions concentration and increasing sulfuric acid amount in the bath. Results from plating in a bath with 200 g/L $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ and 100 g/L sulfuric acid are shown in Figure 13: TP_{min} = 78%, TP_{knee} = 86.6% for 0.25mm TH in 1.6mm panel; Aspect Ratio = 6.4:1.

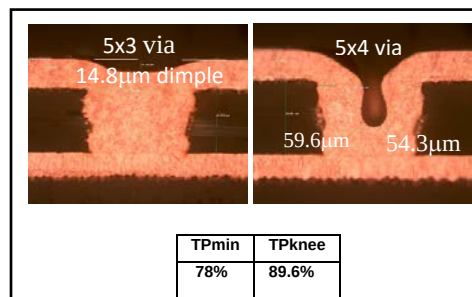


Figure 13 – Plating with reduced copper ion concentration; 0.25mm diameter TH in 1.6mm thick panel

The throwing power was considerably enhanced, TP_{min} = 78% for AR=6.4:1. The small vias, 3mil deep are filled up with a dimple $< 15 \mu\text{m}$. However the via filling of 4mil deep vias was adversely affected, as shown in the cross section images, Figure 13. Still the thickness of copper plating on 5x4 via bottom was $> 150\%$ of the surface copper thickness, that in many cases met the industry requirements. More work was done to improve further the via fill, keeping very good throwing power for thicker panels. Tests with different wetter species were run, leading to good results by using a higher MW organic compound. TP_{min} of about 76-78% and good via fill for 3mil as well as for 4mil deep vias were achieved, when plating in the Process A bath, with basic electrolyte (VMS): 180 - 200 g/L $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$, sulfuric acid = 80 - 100 g/L, Cl = 45 – 50 ppm. The thickness variation across the cathode surface was improved.

Soluble Anode Application

In many cases, soluble anodes are the preferred choice, especially if copper replenishment presents difficulties. The described process was modified for applications with copper phosphorous anodes. Tests were performed in a large-scale pilot tank. Figure 14 shows the process sequence and the plating tank. Eductor spray and / or air agitation were used, sparger pipes per side were 8; with 20 nozzles on each pipe.

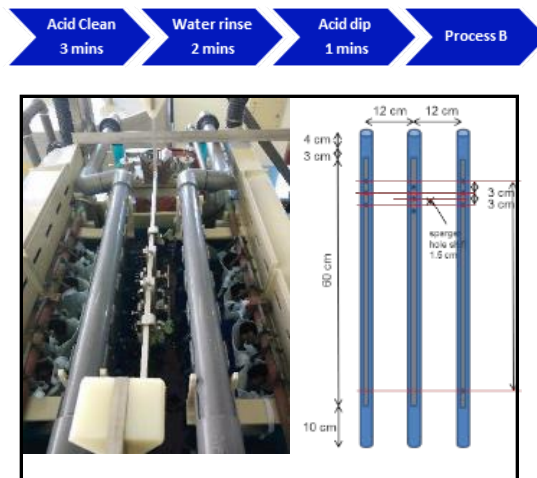


Figure 14 – Process sequence; 650 L tank; soluble anodes; air agitation and side impingement / eductor flow

Excellent via fill and TH Plating were achieved, as shown in Figure 15 using the Process B. The plating conditions were: 16 ASF, 60 minutes, eductor flow 100 LPM/side. The surface copper thickness was 18 – 22 μm , $\text{TP}_{\text{min}} = 93\%$, $\text{TP}_{\text{knee}} = 86.7\%$ for 0.15 mm TH in 0.8 mm panel, AR=5.3.

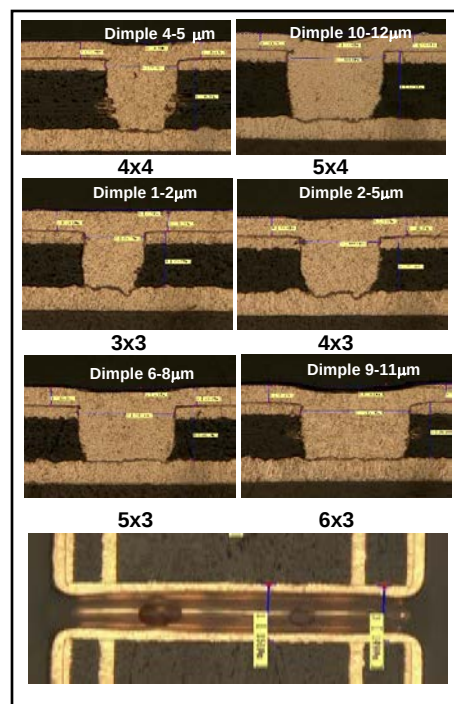


Figure 15 – Plating with soluble anodes

High flow volume setting, 0.8L/nozzle per minute was recommended to achieve good via fill without void defects for high aspect ratio blind vias. Plating of larger vias, 4 x 4.5 mils and 5 x 5.5 mils, is demonstrated in Figure 16: surface plating thickness 0.85-0.9 mil (21-22.5 μm), dimple < 0.5mil (12.5 μm). The operating electrolyte is stable, has extremely long life and no secondary breakdown product that adversely affect via filling was accumulated in the bath. Plating is consistent across the plated boards, Figure 17.

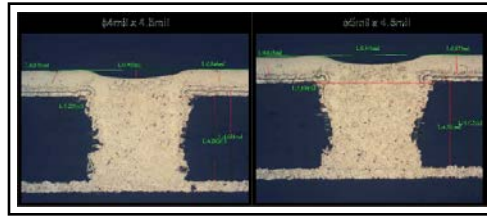


Figure 16 – 650L tank, 0.7L/nozzle*min, 20ASF for 65 minutes



Figure 17 – Soluble anodes; 22.4ASF for 12 minutes + 16ASF for 48 minutes

Through Via Hole Copper Filling Application

In the manufacturing of multi-function electronic products, the fabrication of advanced printed circuit boards (PCBs) with high-density interconnection (HDI) is essential. Copper electrodeposition is particularly beneficial to fill through vias in core layers of HDI and IC package substrate. The results from the Process A optimization was used further in developing a process for filling through micro vias. The interaction of the organic additives, discussed above is very important in determining the proper conditions for an accelerated filling process and a suppressed deposit growth onto the substrate surface.

The most common thicknesses of the plated boards vary from 60 μm up to 200 μm and the through hole diameters are 45 – 100 microns. The holes are either mechanical drilled or laser drilled, resulting in different hole shapes with different requirements for the filling process. Laser drilled through holes usually have a X shape since a laser beam is applied from both sides of the substrate. This makes filling easier, the closure of the hole in the middle being easily achieved.

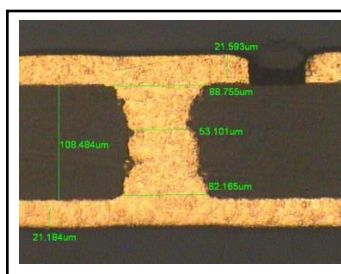
In this study laser drilled X-through via holes in boards up to 0.150 mm thick and diameter at the hole opening of 85 - 90 μm , were used. Filling capability in terms of dimple size, void formation within the filled hole, and metal distribution on the cathode surface are used as measures to describe the capabilities / effectiveness of the technology.

Tests were run to determine the conditions for the best plating process performance. A high copper, low sulfuric acid and low chloride concentration electrolyte was the most favorable for hole filling. Voids during X-plating occur easier for smaller through hole diameter and higher board thickness. The shape and the drilling quality affect significantly the void occurrence as well. In addition, depending on designs, different pitches on one board increase the difficulty to achieve an acceptable plating uniformity.

Using eductor nozzles/fluid impingement, “knife” cathode movement, low CDs and current and/or flow ramping resulted in a uniform plating and in reduction or completely elimination of the voids within the holes. Examples for void-free performance are shown in Figure 18, dimple 0 or < 5 μm .



For pattern plate, electroplating uniformity becomes critical. While panel uniformity can be controlled by mechanical parameters like solution flow, usage of insoluble anodes, etc., in pattern plating the uniformity is mainly determined by usage of proper organic additives that have a significant influence on the surface current distribution. Figure 20 shows pattern through via filling in the innovative copper bath, VCP, 100 μm thick substrate, through via hole diameter of 88 μm at the entrance / 51 μm at the hole center, dimple < 2 μm , no voids, surface copper thickness 20 - 21 μm , with uniform and mirror bright surface appearance.



Using carefully selected plating conditions with correct organic additives types and their concentrations, electrolyte agitation / solution flow rates and current density, an excellent void free through via hole filling can be achieved. The process is applicable for vertical plating equipment, including VCP. Further optimization is needed to fill through vias without voids in thicker cores, 200 μm . Although the preliminary tests for this cases showed promising results, more work is needed to confirm and scale up the process.

Tensile strength and elongation of the plated copper were evaluated in accordance with IPC TM-650, 2.4.18.1. Vertical and horizontal pulls were used. Tensile strength $\Rightarrow$ 42,000 psi and elongation $>$ 20% were measured. Tensile strength as a

function of the bath age up to 100 Ah/L are given in Figures 21 and the elongation results are shown in Figure 22. Plating in a fresh and in an aged bath met and exceeded IPC specifications.

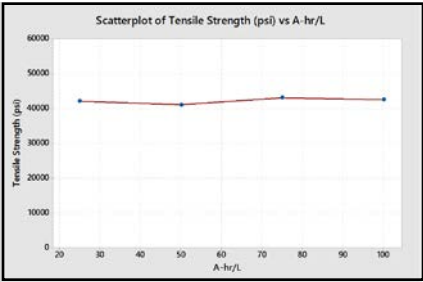


Figure 21 - Tensile Strength versus bath age Ah/L

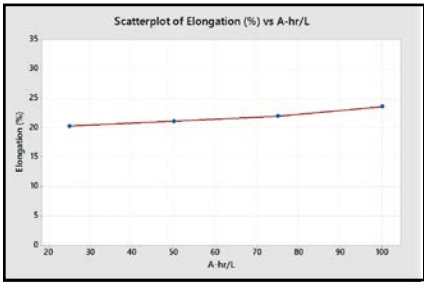


Figure 22 – Elongation, % versus bath age Ah/L

Reliability

For through hole and via reliability, sections were taken and solder shock resistance testing per IPC TM-650 2.6.8 was performed, with 10 second float at 288°C for 6 times. Tests were run with boards plated in baths with soluble and insoluble anodes. The holes were examined for any defects. No corner cracks, starter cracks or TH barrel cracks were present under any plating conditions, Figures 23 refers to TH plating and Figure 24 to via fill.

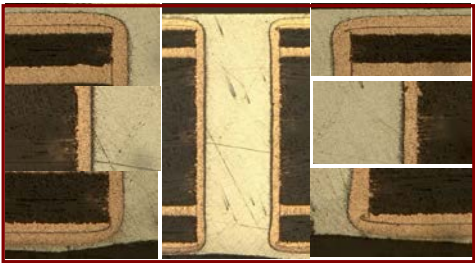


Figure 23 - Solder dip test for through holes after 6x Solder Shock (Eductor flow, soluble anodes)

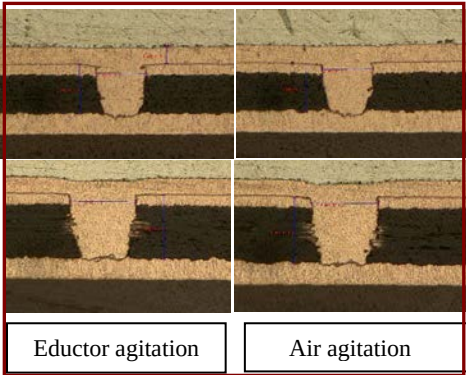


Figure 24 – Solder dip test for blind via after 6x Solder Shock

The thermal characteristics of plated copper met the IPC standards and ensured that no failure occurs during the subsequent soldering operations.

Summary

An innovative DC acid Cu process for simultaneously filling vias and plating through holes was studied in a wide variety of conditions to collect information on its capabilities. The throwing power can be enhanced with optimized physical and chemical plating parameters while keeping very good via fill across a wide range of geometries.

A high copper, low acid solution was used for Through Hole ARs up to 5:1, in 0.8 mm thick panels. The optimization included organic additive concentrations and plating parameters. Conditions of minimum and maximum throwing power and minimum and maximum dimple size were determined and experiments were run under these conditions.

A compromise was achieved between plating conditions that favor via fill and those that are beneficial for TH Plating.

For thicker panels of 1.6 mm, a $TP_{min} = 78\%$ was obtained for 0.25 mm diameter holes, AR = 6.4:1, in a bath containing reduced copper ions concentration and increased acid concentration.

Insoluble and soluble anode applications were shown in this paper.

Filling through via holes in core layers of HDI of the PCB and IC package substrate was discussed. X-through vias, 90 x 150 μm that were filled with <5 microns or zero dimple and no voids or defects were shown. The filling conditions are given. Further work is under way to achieve filling up through via holes in thicker cores.

For mechanical properties, tensile strength $\Rightarrow$ 42,000 psi and elongation $> 20\%$ as well as the thermal resistance of copper deposited from baths with soluble or insoluble anodes meet and exceeded industry standards thus satisfying the need of a highly reliable copper electroplating process.

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