DfR Solutions
RELIABILITY DESIGNED & DELIVERED

sherlock
AUTOMATED DESIGN ANALYSIS™

2019
DESIGN FOR RELIABILITY
CONFERENCE

Using Simulation to Optimize Microvia Placement and Materials to Avoid Failure During Reflow

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03/26/2019

Agenda

01 Introduction

02 Objective 01: Preprocessing

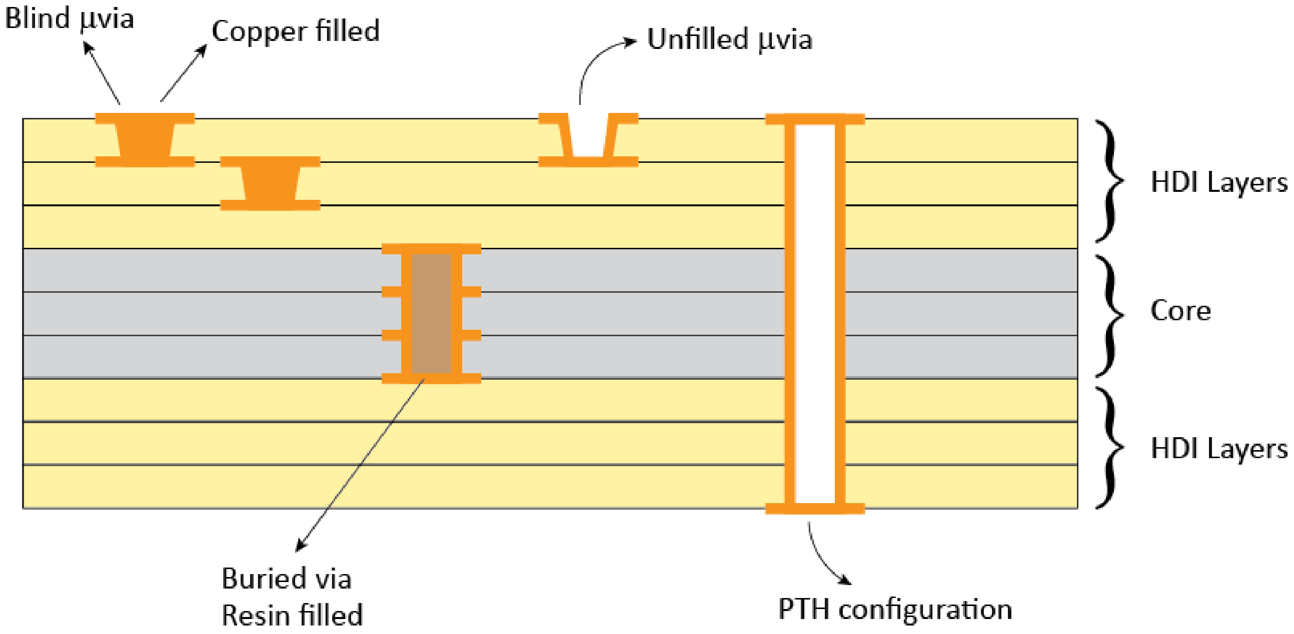
03 Objective 02: Automated FE Scripting

04 Objective 03: Postprocessing, Reliability Analysis of PTHs

05 Objective 03: Postprocessing, Manufacturability of Microvias

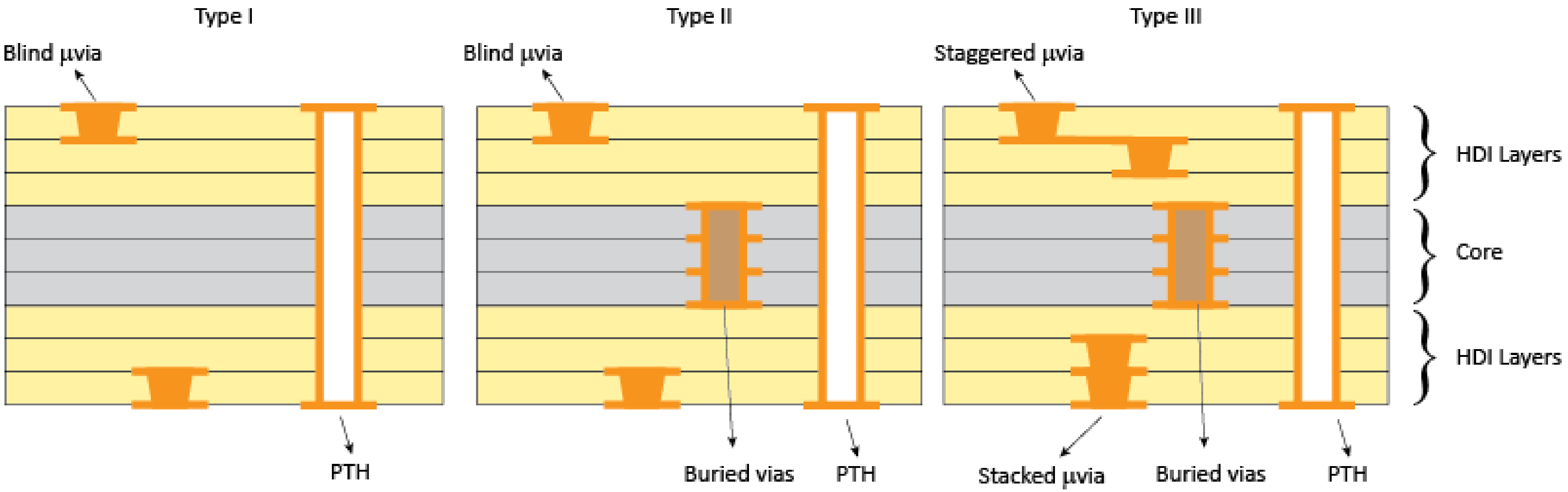
Introduction

- What are PTHs and vias?
  - Structures to interconnect signal circuits at different PCB layers
- Microvia
  - Interconnects between layers for high I/O density of advanced packages in HDI PCBs
  - Aspect ratio (diameter: depth) of $\approx 1:1$
  - With total depth of no more than $0.25\ \mathrm{mm}$
- Type of vias
  - Through via (PTH)
  - Blind via
  - Buried via
  - Filled via
  - Unfilled via



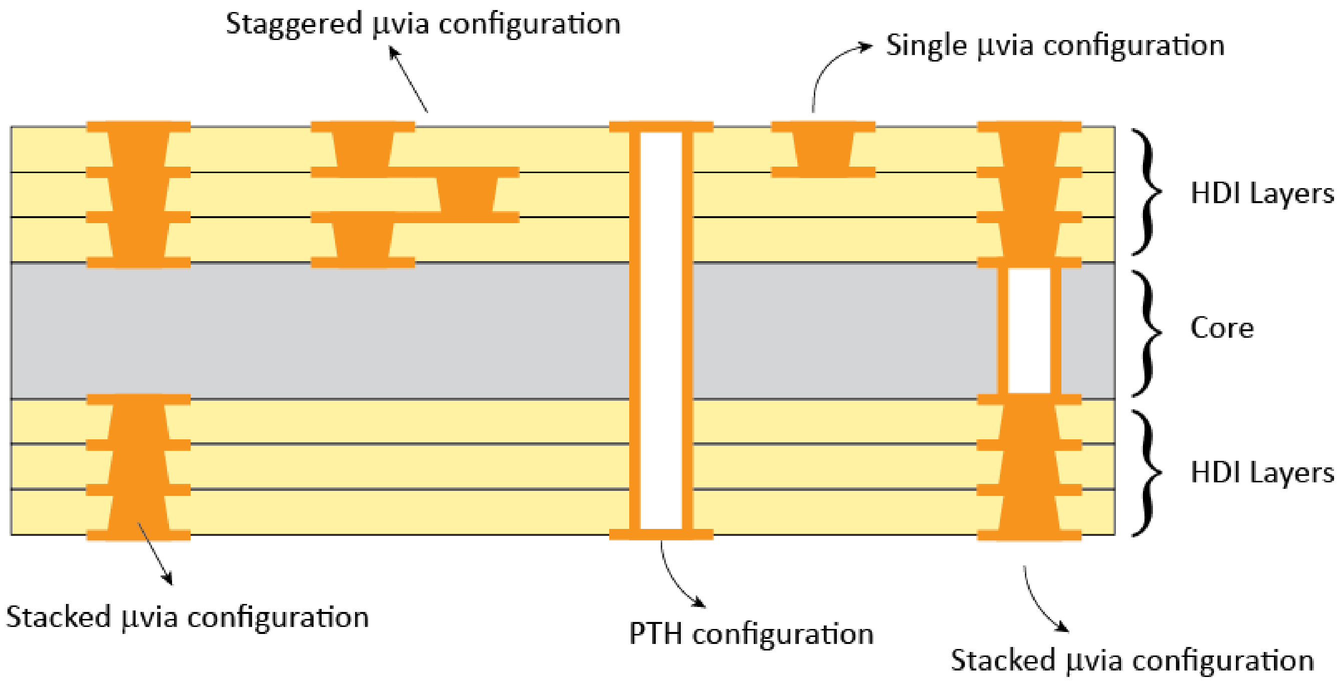
Introduction

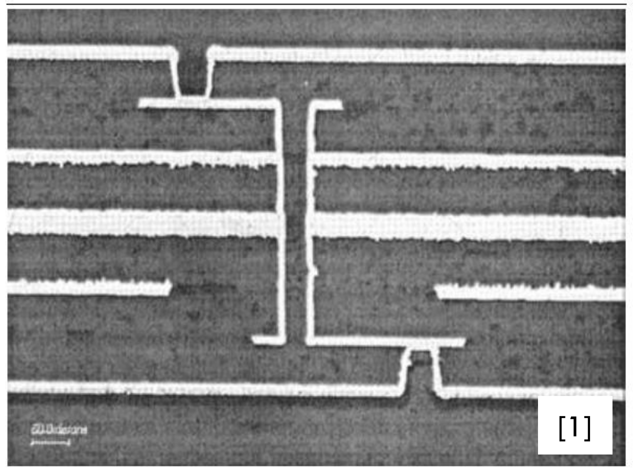
- What is HDI PCB?
  - PCB with higher density per unit area than conventional PCB
- Different HDI Features
  - Type I.
  - Type II.
  - Type III.

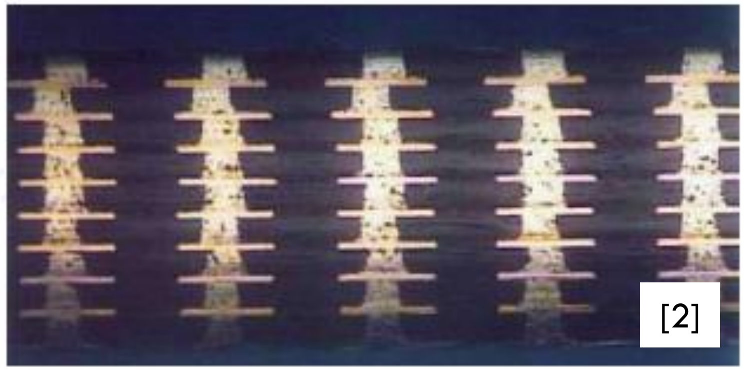


Introduction

- Microvia
  - Based on relative position of microvias
    - Stacked microvias
    - Staggered microvias







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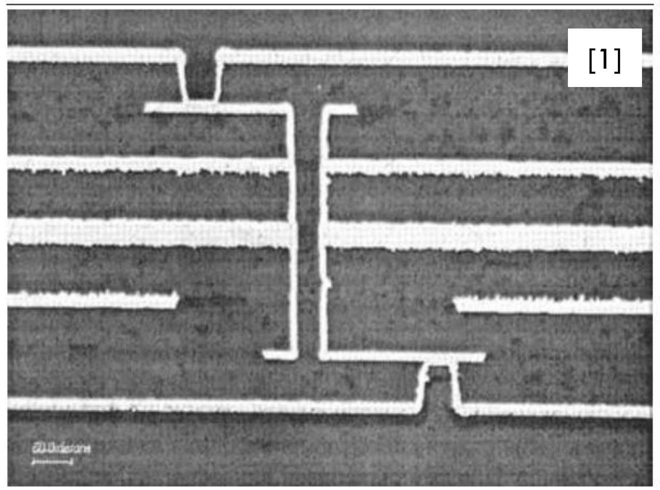
[1] Lau, John H., and Chris Chang. 2000. “An Overview of Microvia Technology.” *Circuit World* 26 (2): 22–32.
[2] Buck, Tom. 2014. “The Future of HDI Via Structures, Power Delivery, and Thermal Management in Next Generation Printed Circuits.”

Introduction

- Design rule of thumbs
  - Robustness
    - staggered μvias > stacked μvias
  - Higher density of interconnects
    - Load sharing between interconnects
    - Lower developed stress and strains
    - Less probability of failure
    - Reality
      - Manufacturing limitation
      - Higher manufacturing defects



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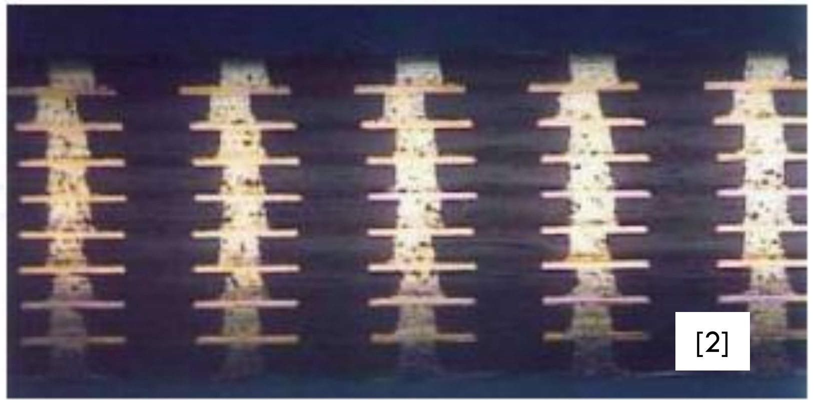

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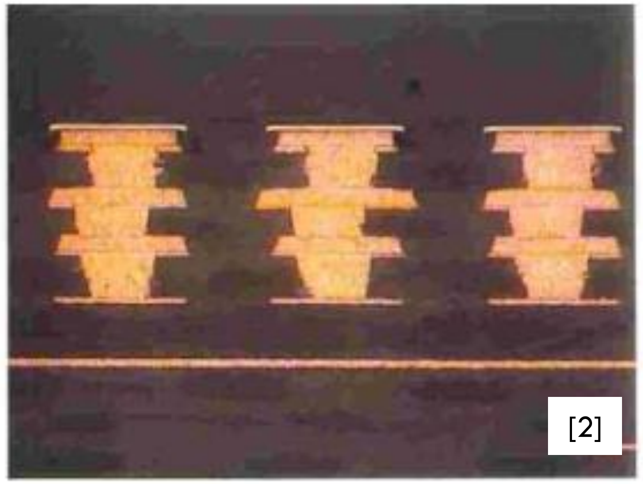

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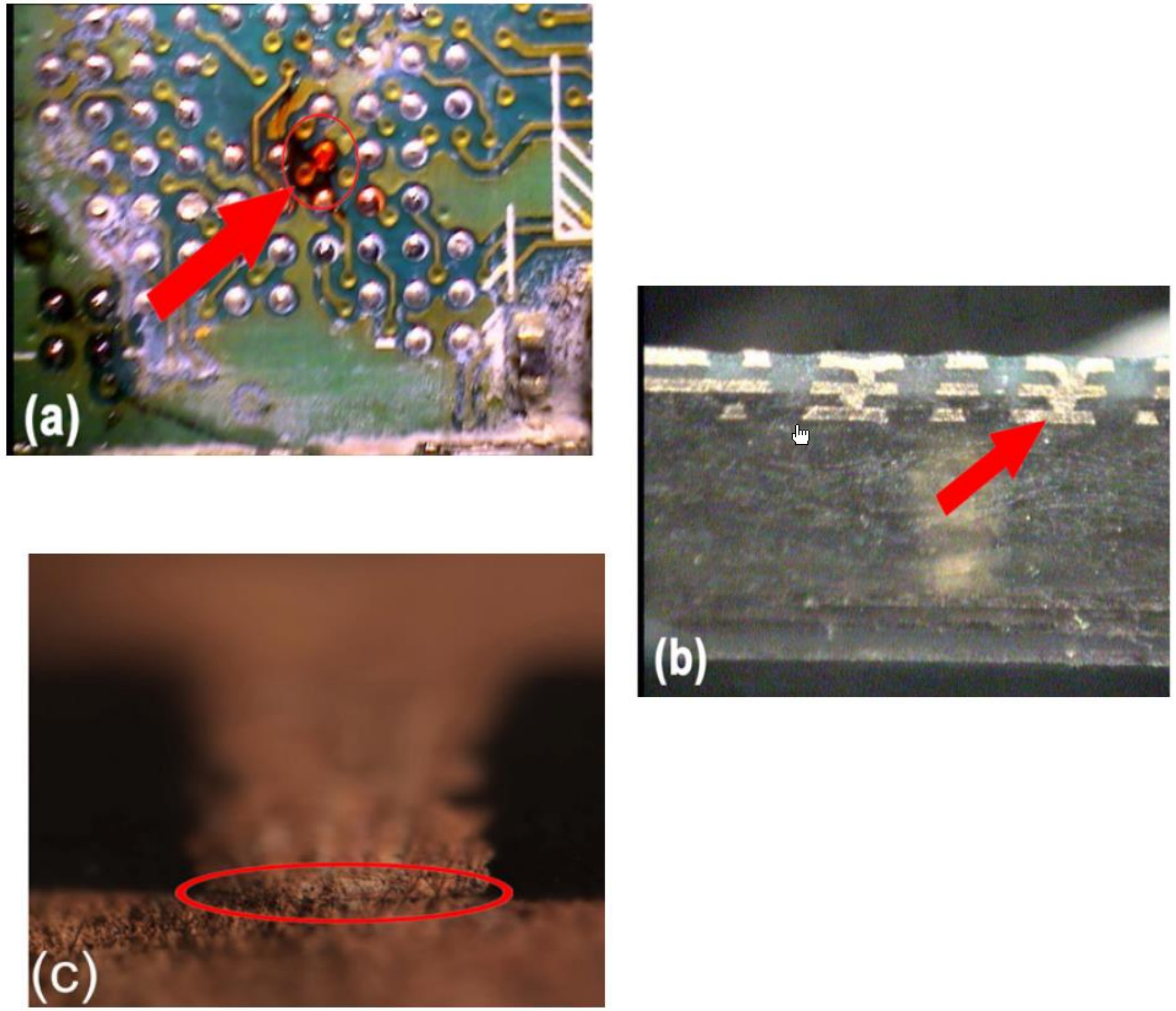
[1] Lau, John H., and Chris Chang. 2000. "An Overview of Microvia Technology." *Circuit World* 26 (2): 22–32.
[2] Buck, Tom. 2014. "The Future of HDI Via Structures, Power Delivery, and Thermal Management in Next Generation Printed Circuits."

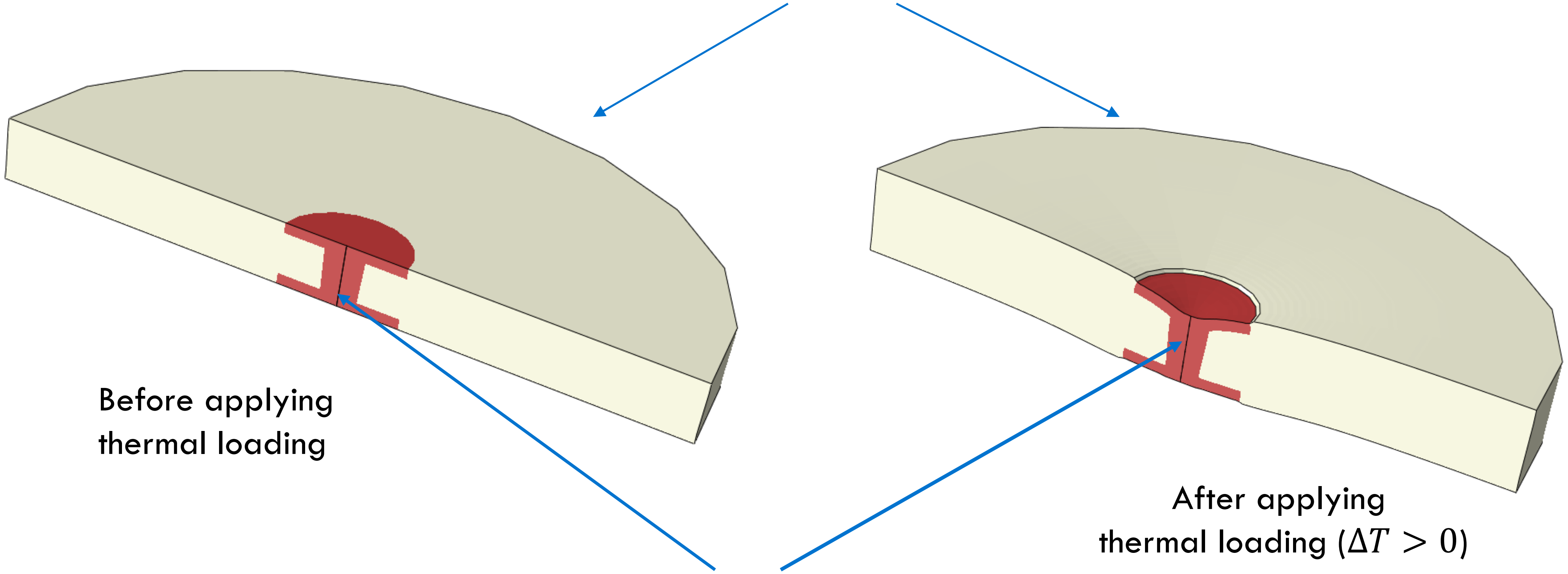
Introduction

- Main cause of open circuit in PCBs
  - PTH and via failures
  - Dominant driving force of via failure
    - Thermal stresses due to CTE mismatch between copper and board (17 ppm/°C vs. 55 ppm/°C)



Ji, Li-Na, Yi Gong, and Zhen-Guo Yang. 2010. “Failure Investigation on Copper-Plated Blind Vias in PCB.” *Microelectronics Reliability* 50 (January): 1163–70.

Introduction



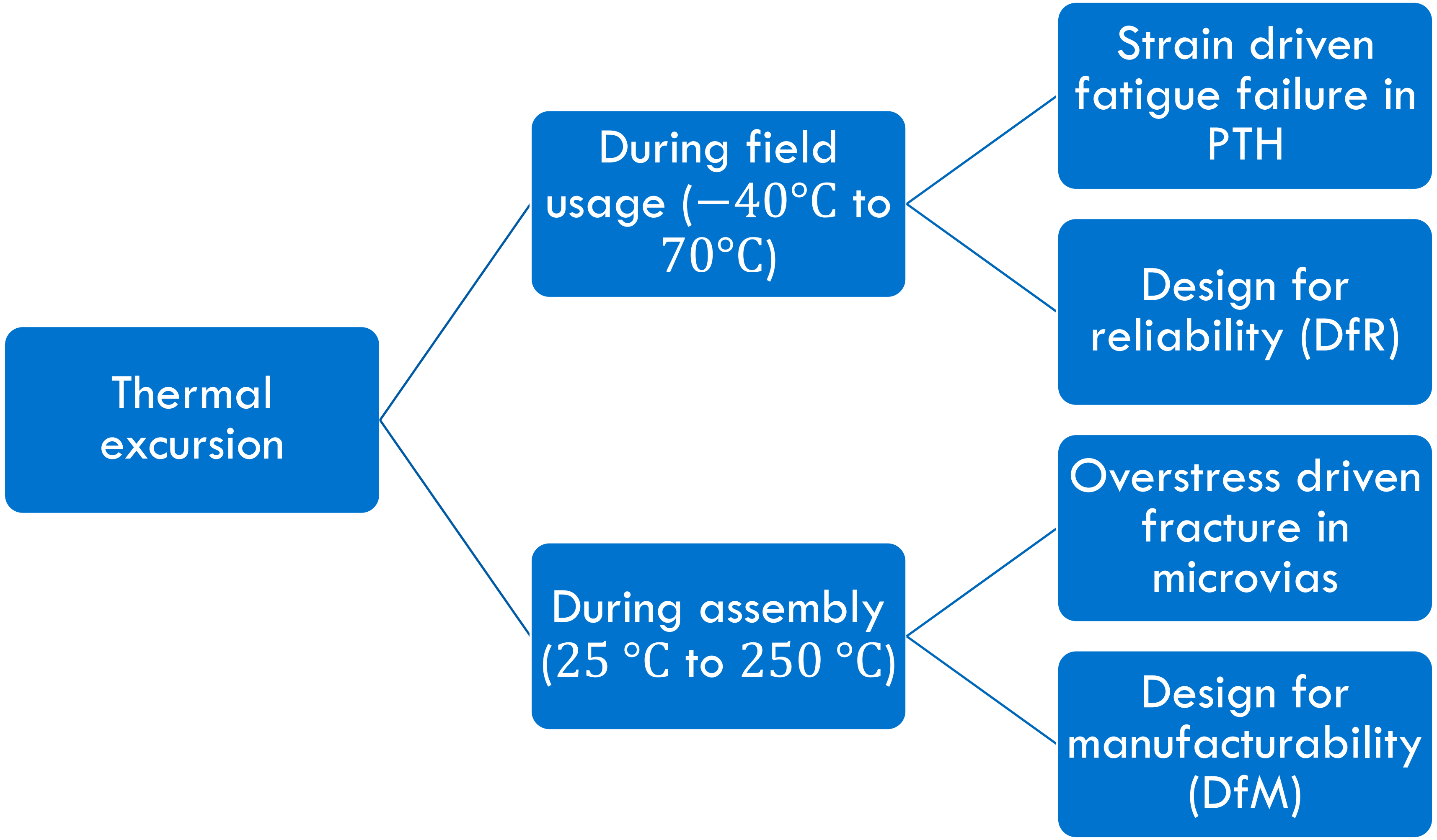
Laminate layer (higher CTE ~ 55)

Before applying thermal loading

After applying thermal loading ($\Delta T > 0$)

Single level filled microvia (copper with much lower CTE ~17)

Introduction



Thermal excursion

During field usage ($-40°C$ to $70°C$)

During assembly ($25\ °C$ to $250\ °C$)

Strain driven fatigue failure in PTH

Design for reliability (DfR)

Overstress driven fracture in microvias

Design for manufacturability (DfM)

Introduction

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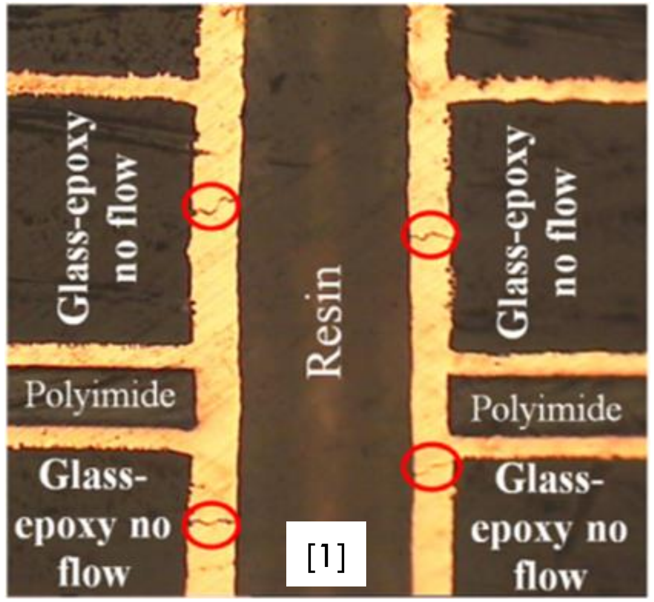
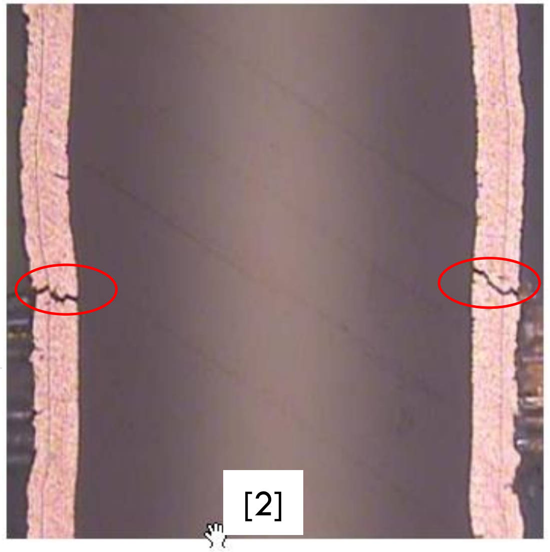
Strain driven fatigue failure in PTHs

- Due to accumulation of plastic strain during thermal cycling
- Manifest as crack along PTH barrel
- Depending on the plating quality, number of cycles to failure varies from 500 to 10,000 cycles





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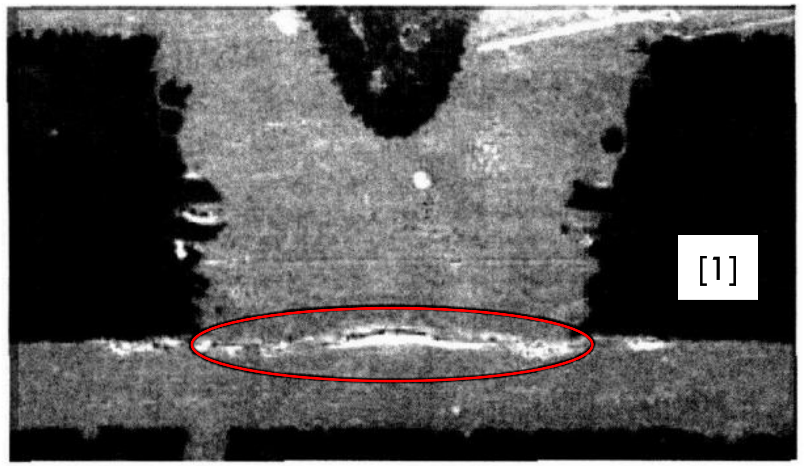
[1] Salahouelhadj, A., M. Martiny, S. Mercier, L. Bodin, D. Manteigas, and B. Stephan. 2014. "Reliability of Thermally Stressed Rigid–Flex Printed Circuit Boards for High Density Interconnect Applications." *Microelectronics Reliability* 54 (1): 204–13.
[2] Wu, Jing-Han, Liao Meng-Chieh, Luo Tzeng-Cherng, and Huang Te-Chun. 2011. "Comparison the Reliability of Small Plated-through Hole with Different Diameters under Thermal Stress." In . IEEE.

Introduction

Overstress driven fracture in microvias

- Due to high tensile stress during solder reflow in the assembly process
- Manifest as
  - Interfacial separation between capture/target pad and microvia body
  - Corner cracks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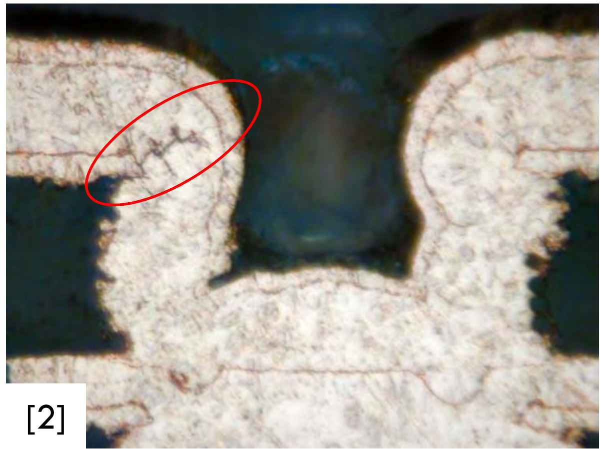
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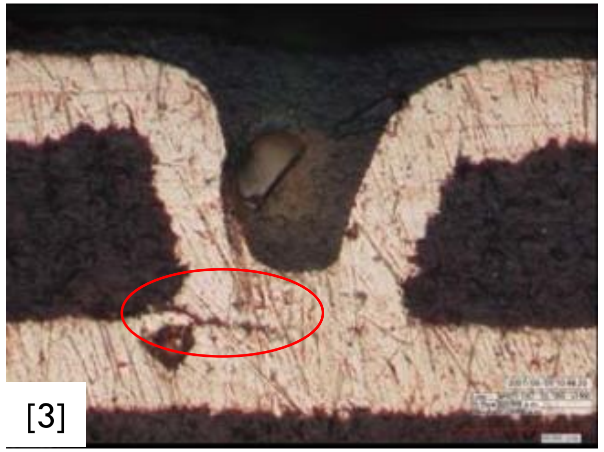
[3]

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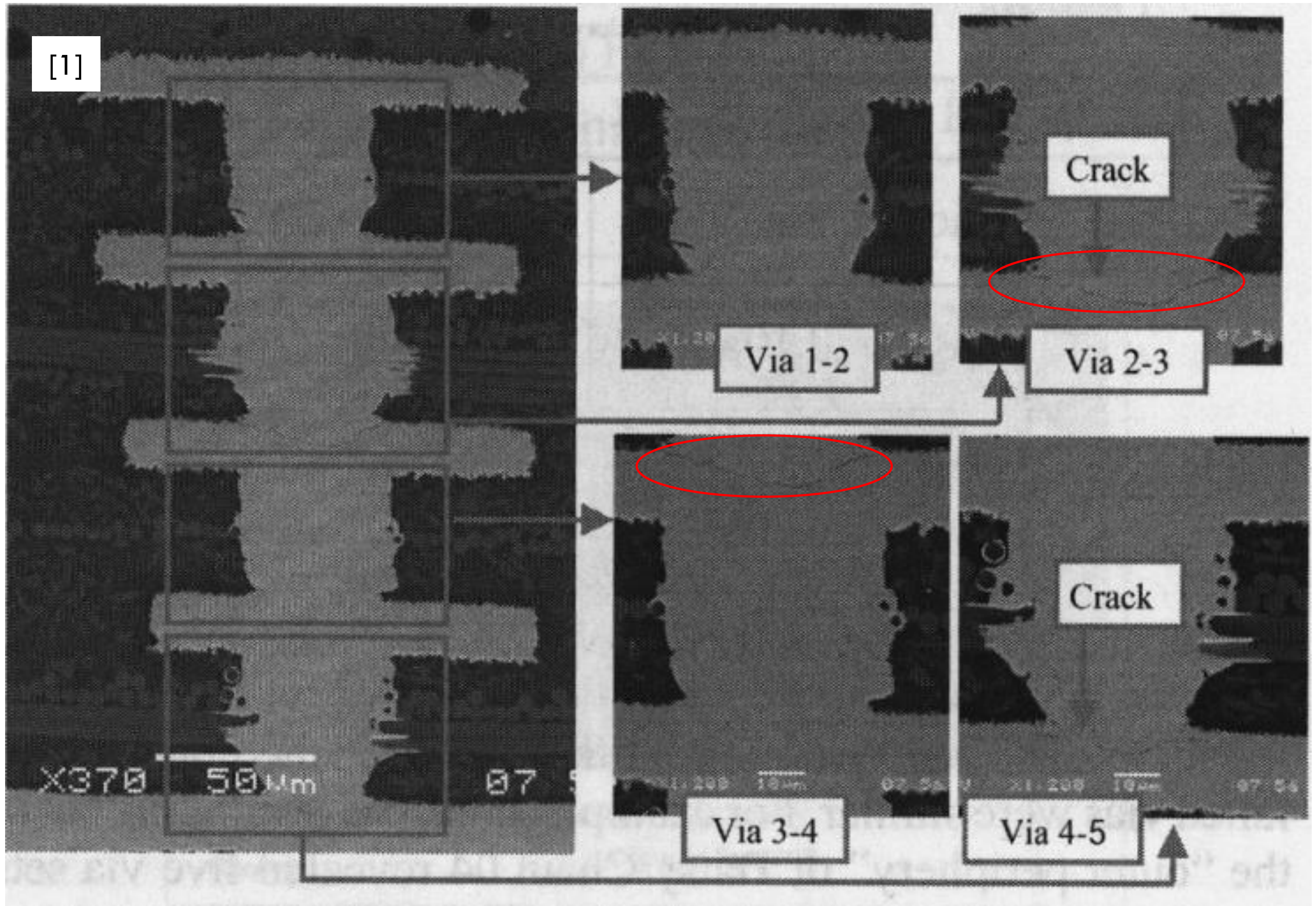
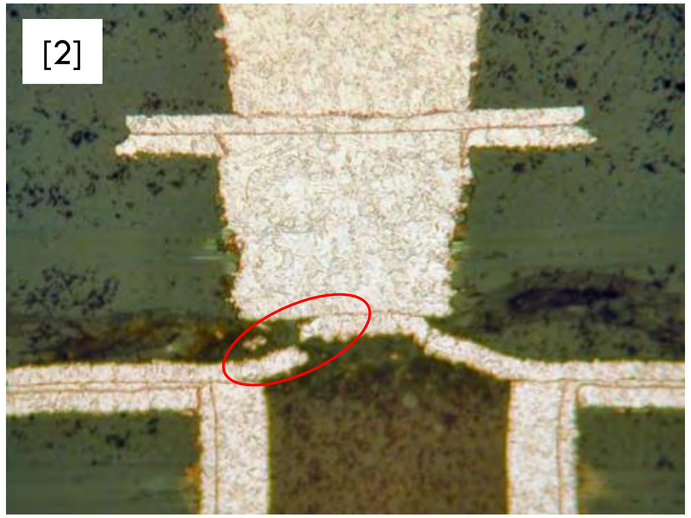
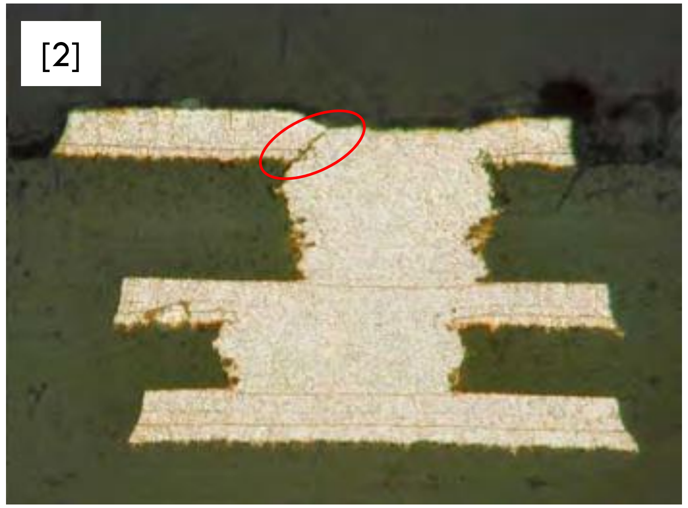
[1] Hong Wang, Tong, and Yi-Shao Lai. 2006. “Stress Analysis for Fracturing Potential of Blind via in a Build-up Substrate.” *Circuit World* 32 (2): 39–44.
[2] Li-Na Ji, Zhen-Guo Yang, and Jian-Sheng Liu. 2008. “Failure Analysis on Blind Vias of PCB for Novel Mbile Phones.” *Journal of Failure Analysis & Prevention* 8 (6): 524–32.
[3] Birch, Bill. 2009. “Reliability Testing for Microvias in Printed Wire Boards.” *Circuit World* 35 (4): 3–17

Introduction







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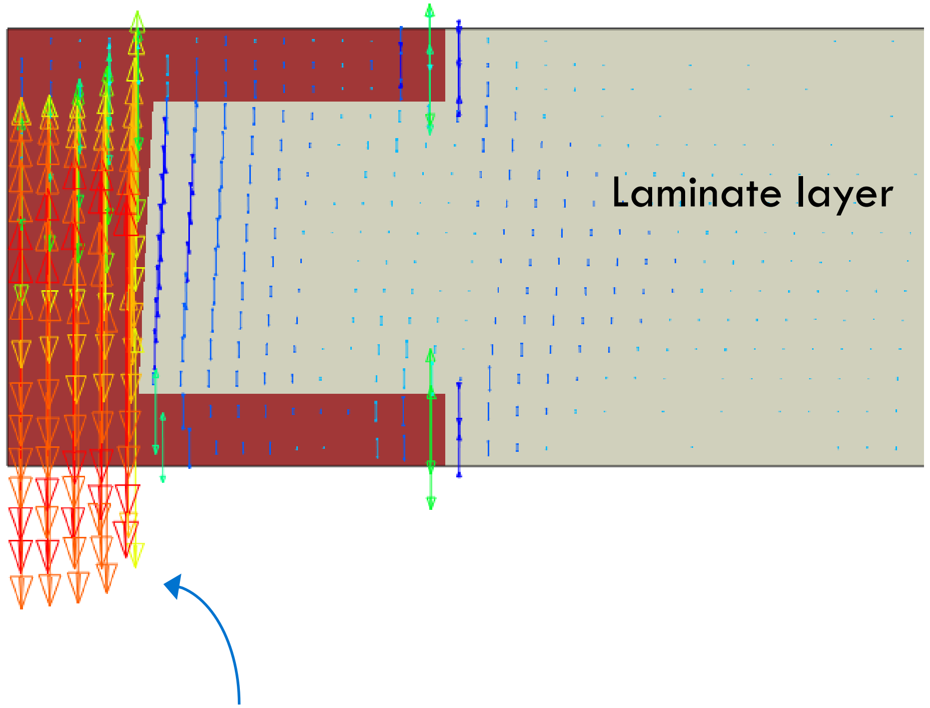
[1] Leung, Dennis, and Guna Selvaduray. 2008. “Effect of Design Factors on Microvia Reliability of Flip Chip Ball Grid Array Polymeric Substrates.” *Journal of Microelectronics and Electronic Packaging* 5 (3): 104–15.
[2] Birch, Bill. 2009. “Reliability Testing for Microvias in Printed Wire Boards.” *Circuit World* 35 (4): 3–17.

Introduction

Overstress driven fracture in microvias

- Due to high tensile stress during solder reflow in the assembly process
- Manifest as
  - Interfacial separation between capture/target pad and microvia body
  - Corner cracks

Single microvia

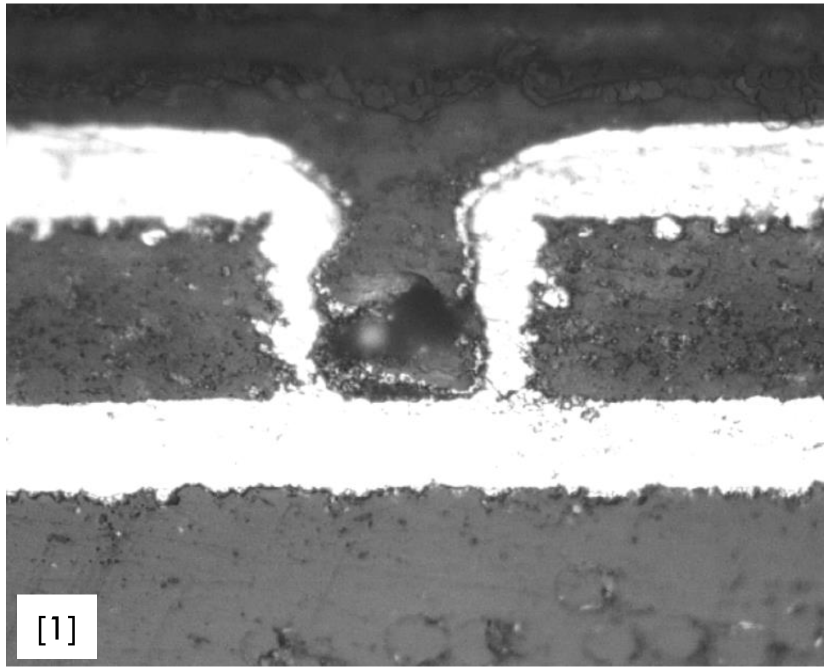


Tensile stress developed
in microvia during thermal extrusion

Challenges In Electronics Industry

- Quality of plating
  - Extreme variation depending on manufacturer
  - The reliability and manufacturability heavily depends on quality
- Lack of robust material characterization (specially for copper)
  - Young's modulus varies from $E = 23 \rightarrow 130\ \mathrm{GPa}$
  - Yield stress varies from $\sigma_y = 70 \rightarrow 310\ \mathrm{GPa}$
- Lack of reliable statistical analysis
  - Long daisy chains with first failure reports only
  - No suspension consideration
  - …

Challenges In Electronics Industry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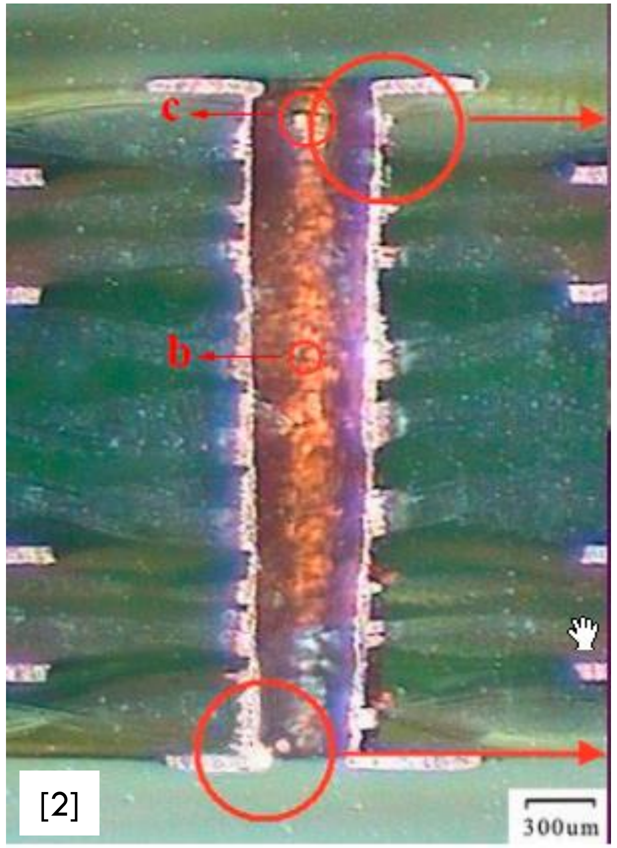

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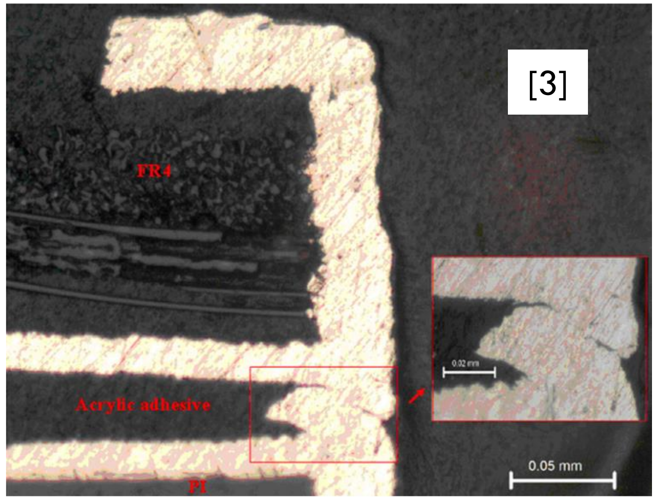

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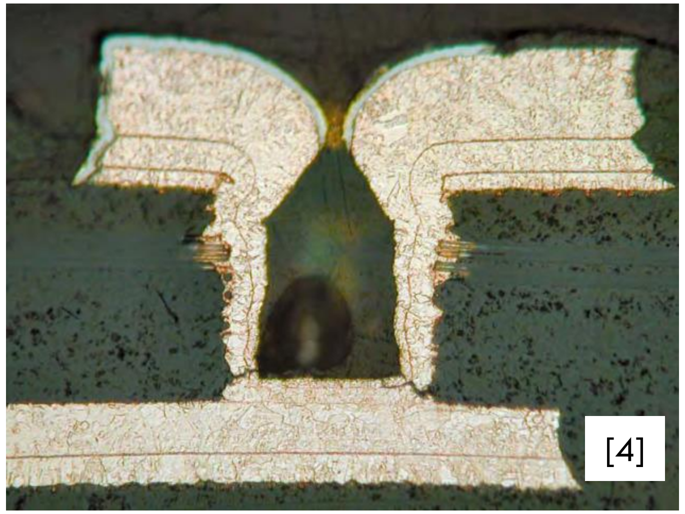
[4]

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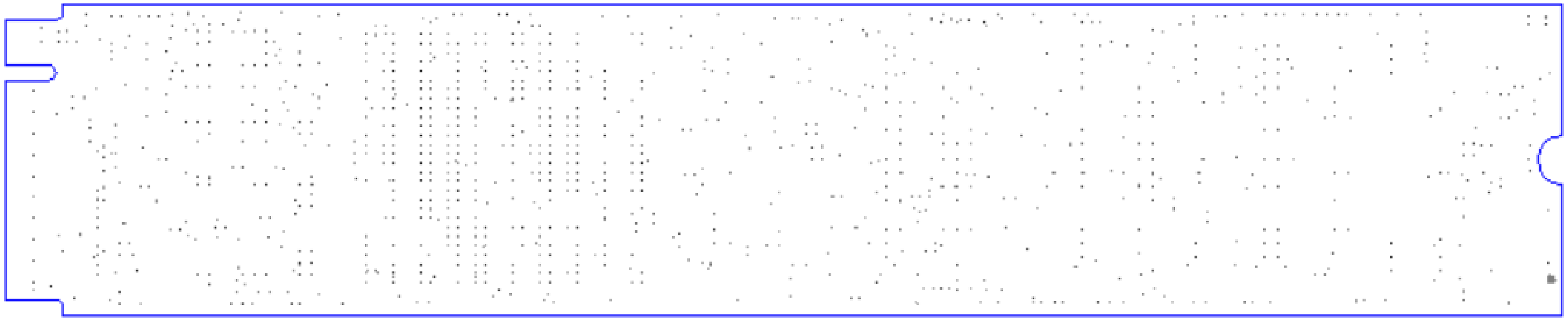
[1] Liu, Fuhan, Jicun Lu, Venky Sundaram, Dean Sutter, George White, Daniel Baldwin, and R. Tummala. 2001. “Reliability Assessment of Microvias in HDI Printed Circuit Boards.” In *2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220), Electronic Components and Technology Conference, 2001. Proceedings., 51st, Electronic Components and Technology*, 1159.
[2] Li, Y., W. Hu, Y. Sun, Z. Wang, and A. Mosleh. 2017. “A Life Prediction Model of Multilayered PTH Based on Fatigue Mechanism.” *Materials (Basel)* 10 (4).
[3] Huang, S. Q., K. C. Yung, and B. Sun. 2012. “A Finite Element Model and Experimental Analysis of PTH Reliability in Rigid-Flex Printed Circuits Using the Taguchi Method.” *International Journal of Fatigue* 40: 84–96.
[4] Birch, Bill. 2009. “Reliability Testing for Microvias in Printed Wire Boards.” *Circuit World* 35 (4): 3–17.

The Big Picture

- Analyze a PCB with tens of thousands of interconnects
- Identify the ones susceptible to failure
- Build and run a FEM on them for reliability as well as manufacturability



Overview

Design Files

- ODB++
- Drill files
- Gerber files
- …

Sherlock

- Preprocessing
  - Parse and bin holes in the PCB
  - Classify holes into three categories; PTH, stacked, and staggered
  - Identify configuration susceptible to failure
  - Gather geometrical and material parameters of marked configs and send them to FEA

→ Objective 1

FEM

- Processing using automated scripting
  - Build and run FE models simulating thermal excursion in reflow process and field usage
  - Send the results back to Sherlock for postprocessing

→ Objective 2

Sherlock

- Postprocessing
  - Perform reliability analysis for PTHs(low-cycle fatigue prediction)
  - Perform manufacturability analysis for stacked μvias (interfacial separation in reflow process)

→ Objective 3

Objective 1: Preprocessing

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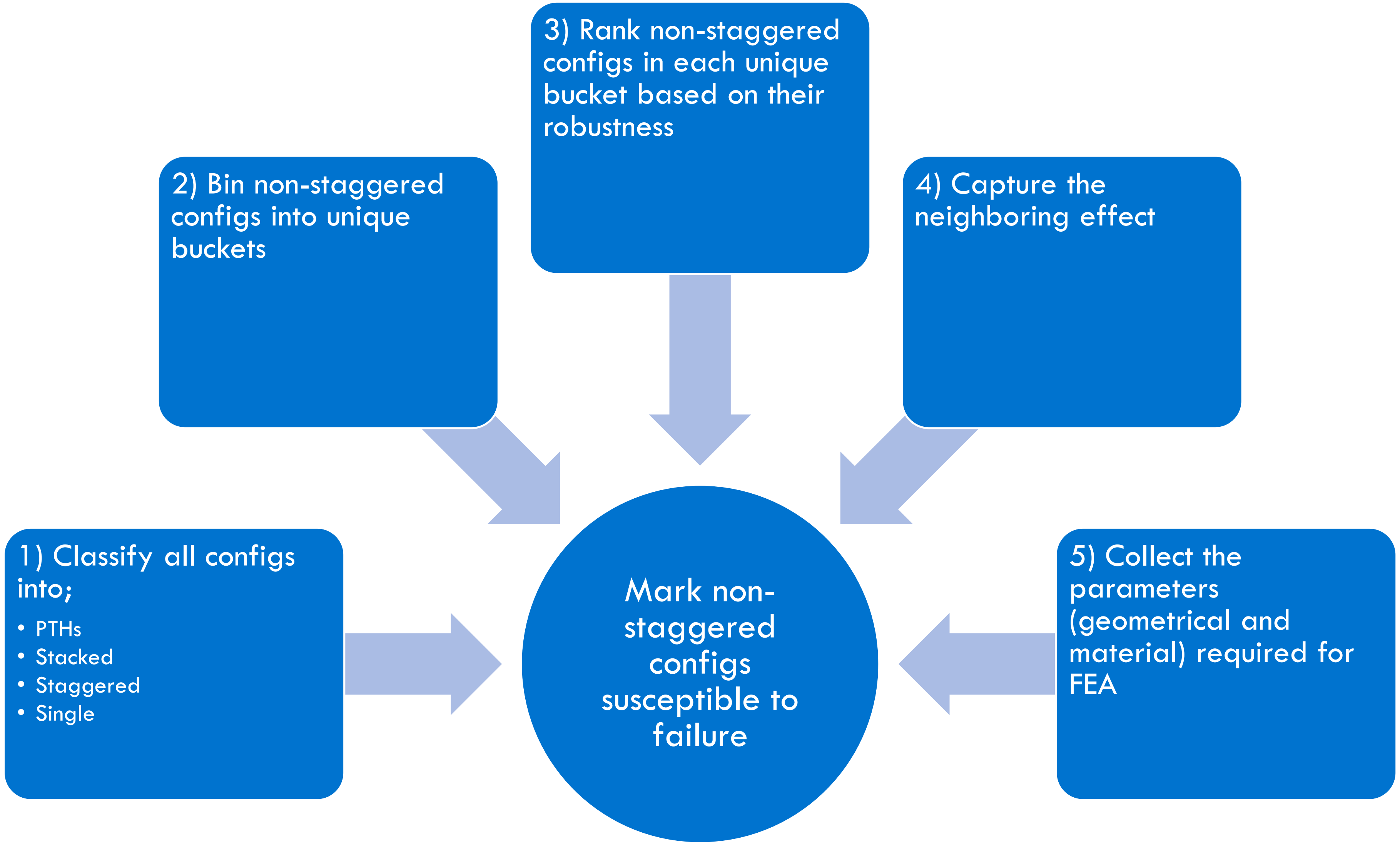


1) Classify all configs into;
- PTHs
- Stacked
- Staggered
- Single

2) Bin non-staggered configs into unique buckets

3) Rank non-staggered configs in each unique bucket based on their robustness

4) Capture the neighboring effect

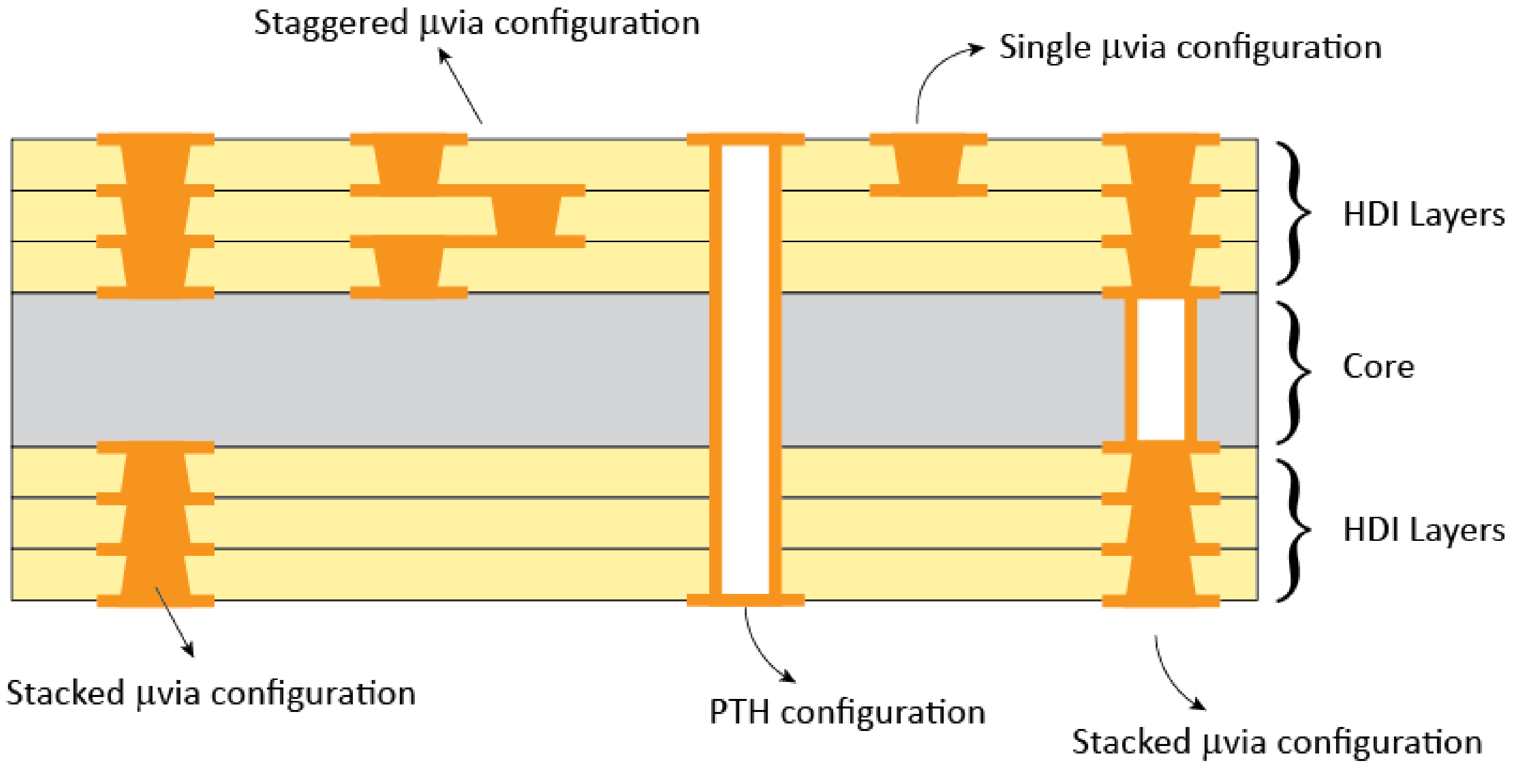
5) Collect the parameters (geometrical and material) required for FEA

Mark non-staggered configs susceptible to failure

Objective 1: Preprocessing

1) Classify all configurations into

- PTH configuration
- Stacked μvia configuration
- Single μvia configuration
- Staggered μvia configuration



Objective 1: Preprocessing

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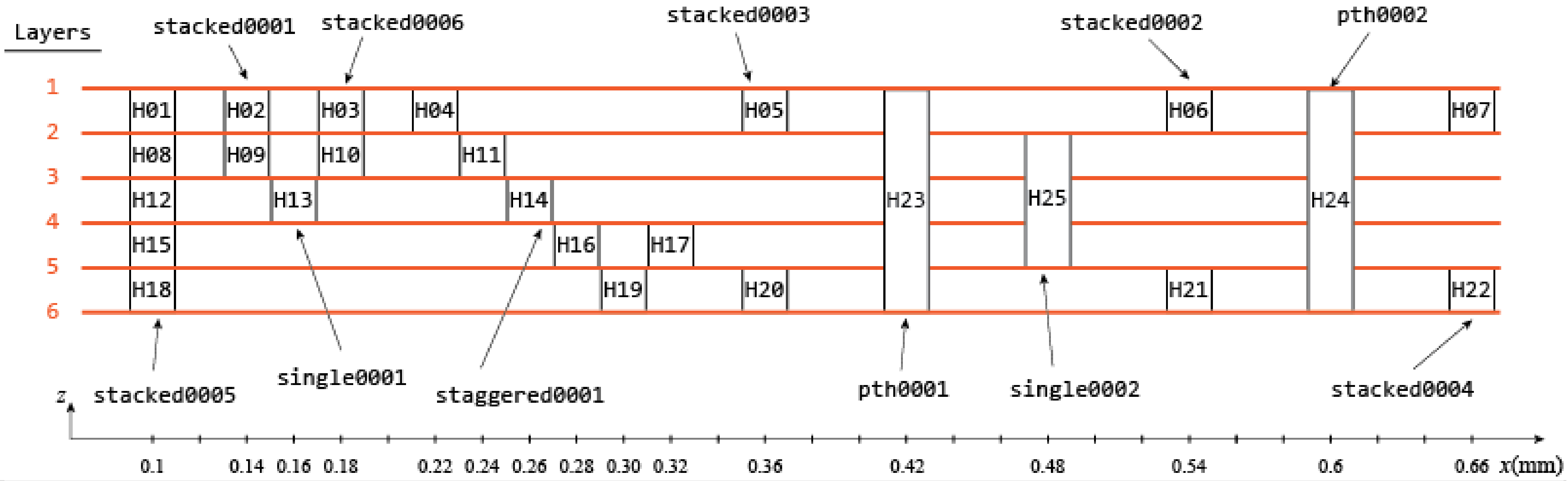
2) Bin non-staggered configurations into unique buckets

- Number of holes involved in the configuration
- Number of layers that are being connected by each hole involved in the configuration
- Location of the holes in the thickness direction of the board e.g.,
    - stacked0001 stacked0006 belongs to one bucket
    - stacked0002, stacked0003, stacked00004 belong to one bucket



Objective 1: Preprocessing

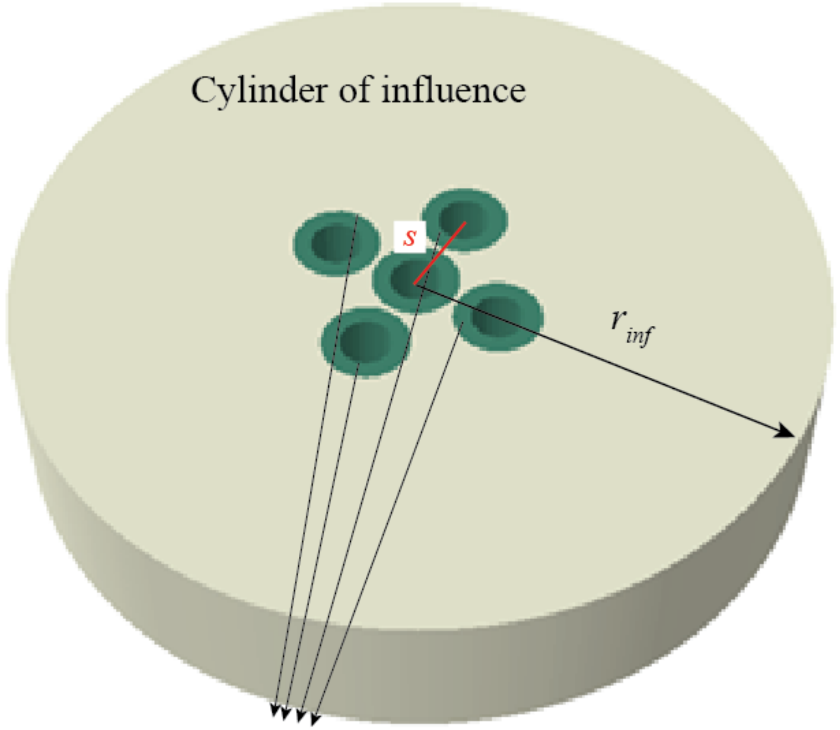
3) Rank non-staggered configurations in each unique bucket based on their robustness

– For each bucket, the neighboring configurations will be the factor determining the robustness

› Neighboring effect

- Interconnects share thermal loadings
- Lower stress and strains in the interconnects
- Less chance of failure

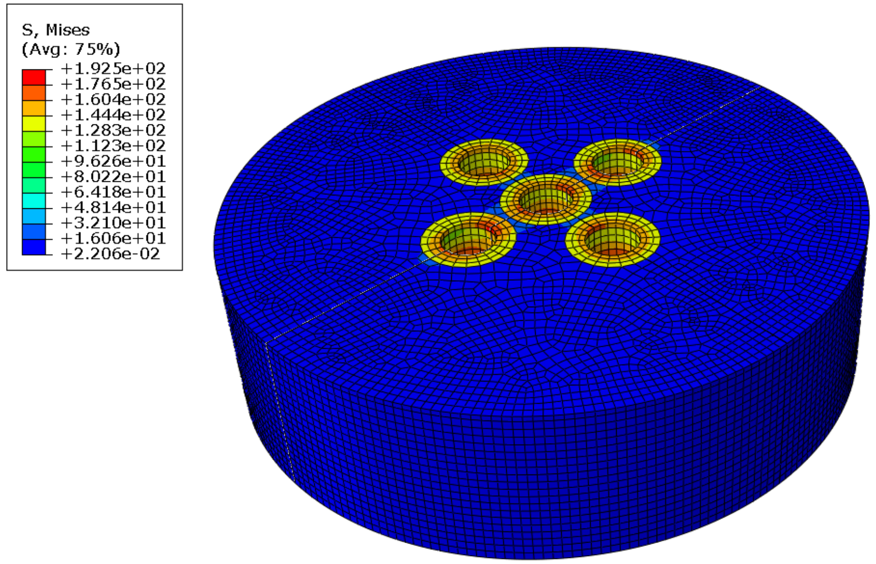
› As the distance between neighboring configurations becomes greater than some critical value $r_{\text{inf}} = 4d$ the neighboring effect become negligible



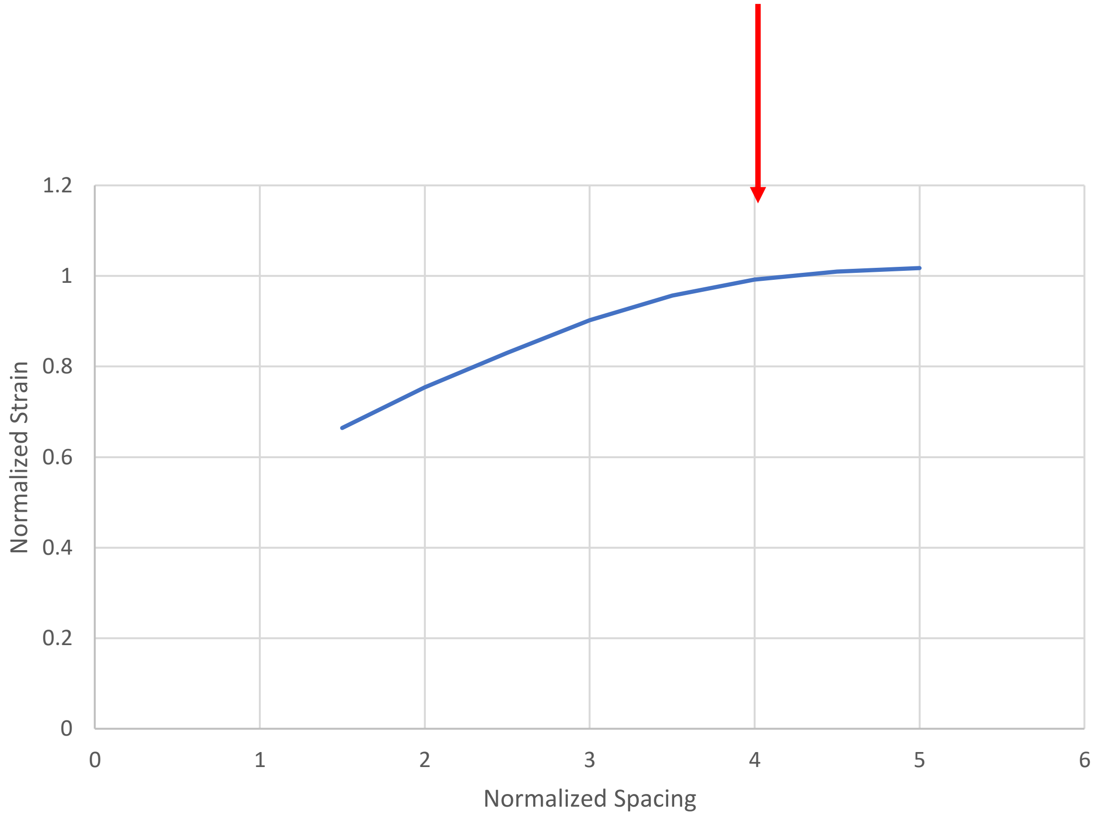
Neighboring configurations contributing to the copper content in the vicinity of the configuration that is being analyzed

Objective 1: Preprocessing

Radius of Influence



$$r_{\mathrm{inf}} = 4d$$



Objective 1: Preprocessing

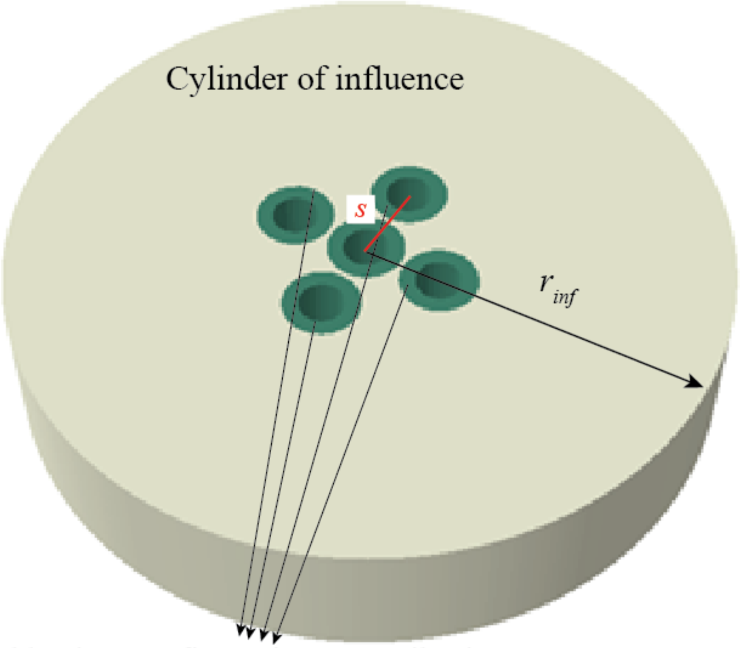
3) Rank non-staggered configurations based on their robustness

- Distance to the nearest-neighbor configuration, s
- Content of copper in the nearest-neighbor configuration
- Number of configurations in the radius of influence

$$\text{grade(non-staggered config)} = \sum_{i=1}^{n} \frac{v_i}{d_i}$$

- v_i is the volume fraction of the copper in the ith nearest config
- d_i is the center-to-center distance to the ith nearest config

Need to identify nearest configurations



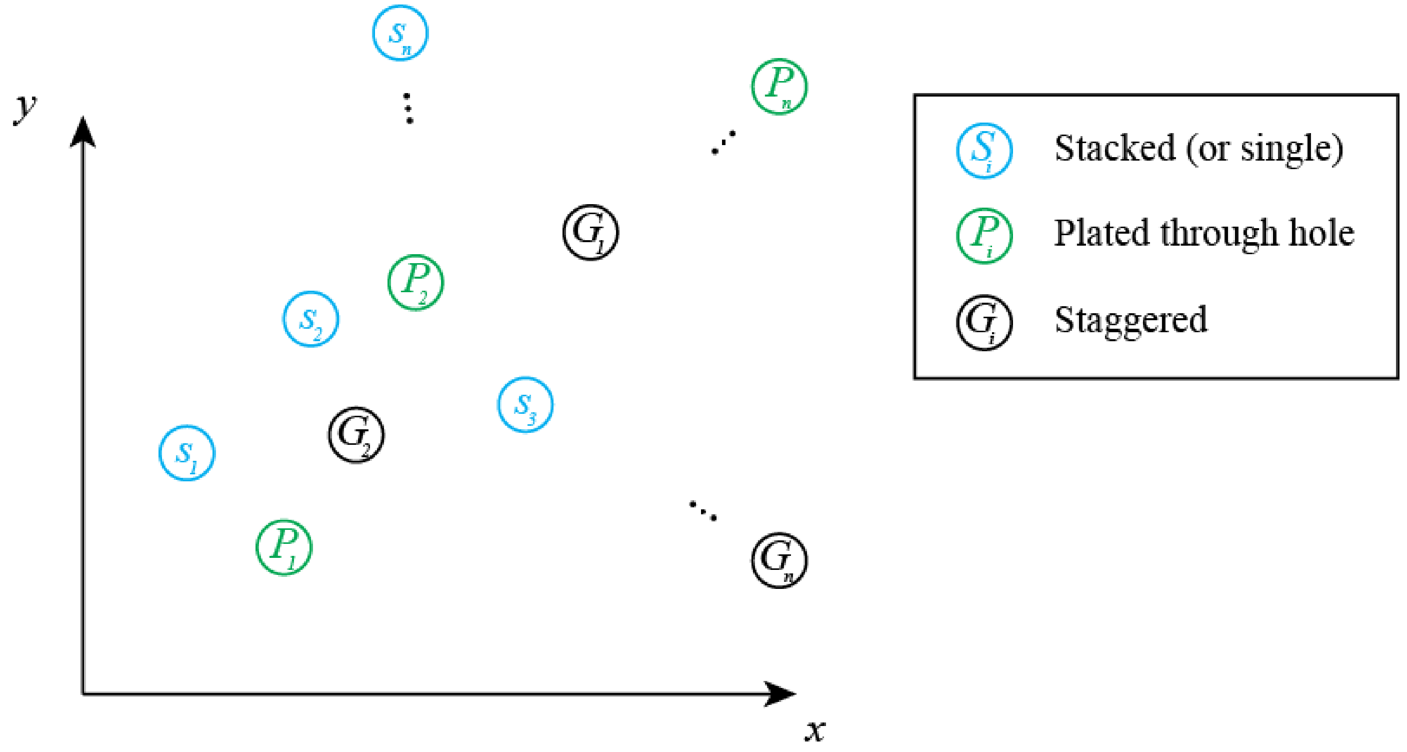
Neighboring configurations contributing to the copper content in the vicinity of the configuration that is being analyzed

Objective 1: Preprocessing

Nearest-neighbor (NN) analysis

- Represent each config by their centroid

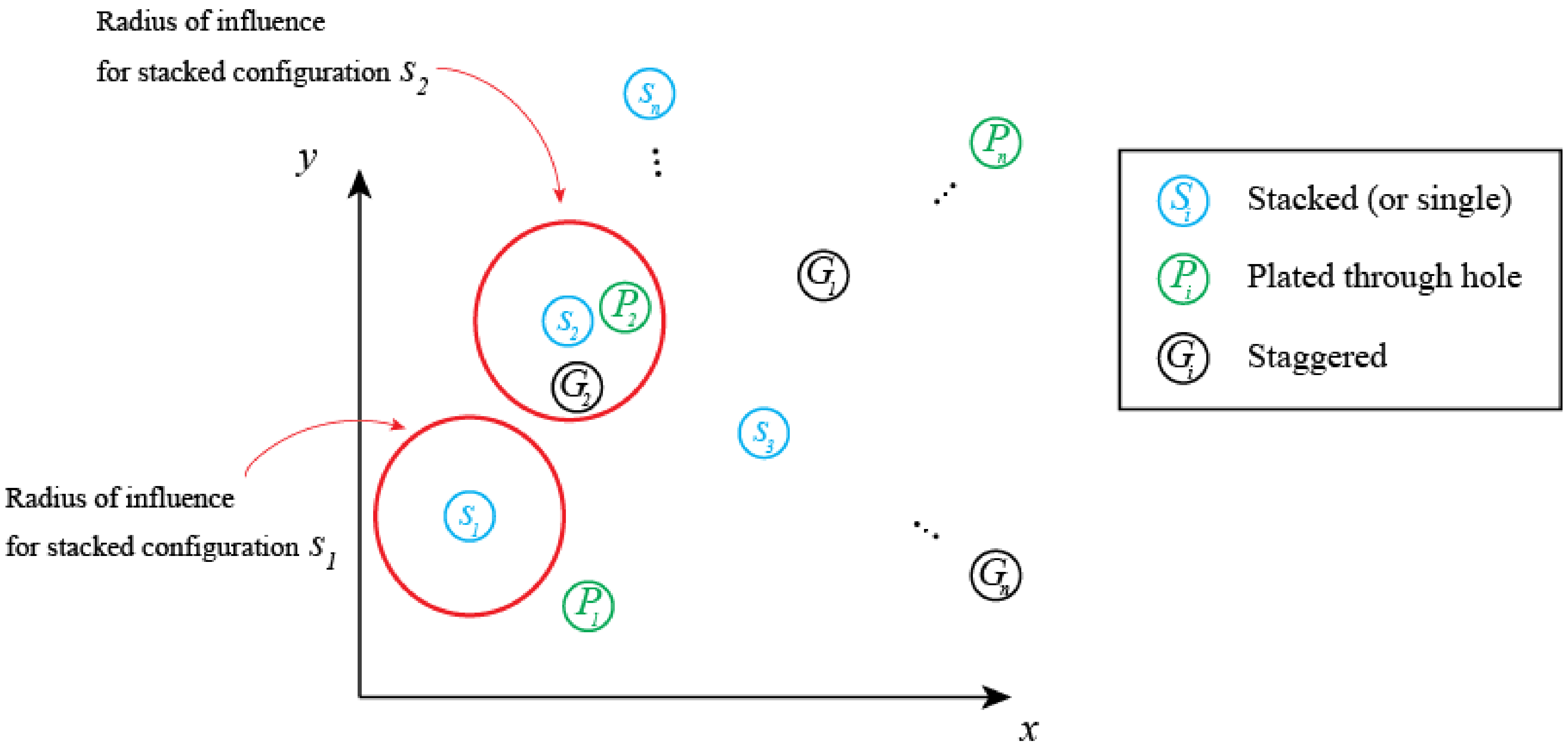
$$\overline{x}_k = \frac{\sum_{i=1}^{m} x_i}{m}, \overline{y}_k = \frac{\sum_{i=1}^{m} y_i}{m}$$



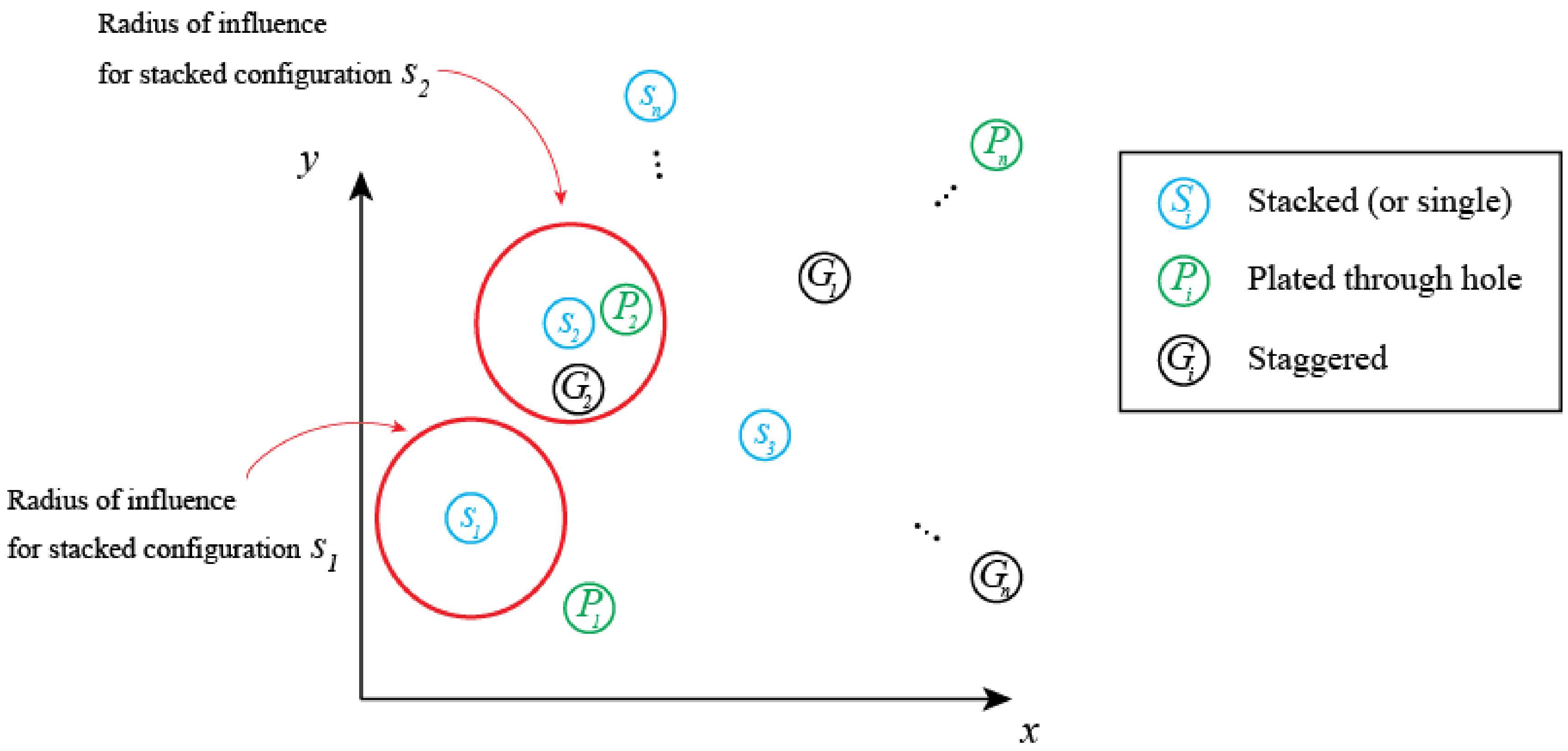
Objective 1: Preprocessing

3) Rank non-staggered configurations based on their robustness

- Cylinder of influence
- Number of neighboring configurations in cylinder of influence
- Content of copper in cylinder of influence



Objective 1: Preprocessing

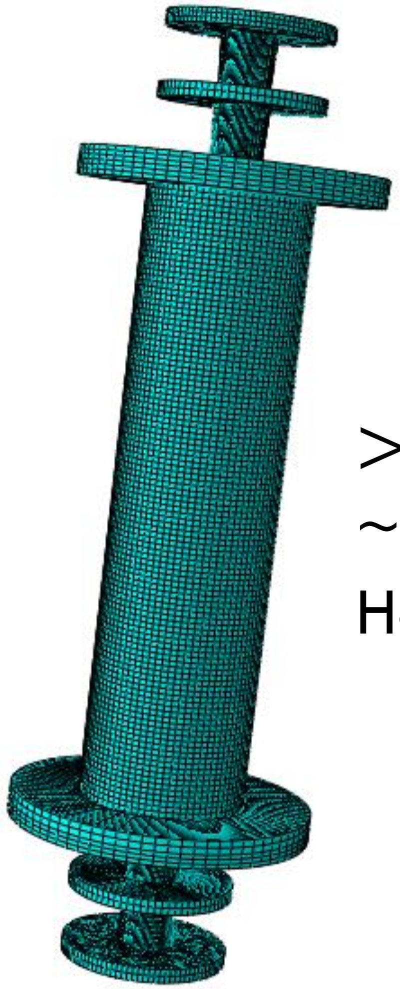


$$\text{grade}(s_1) = 0.0$$

$$\text{grade}(s_2) = \frac{v_{p_3}}{d_{p_3}} + \frac{v_{G_2}}{d_{G_2}}$$

Objective 1: Preprocessing

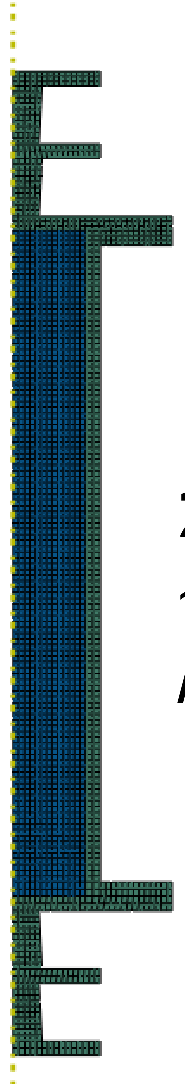
3D



> 200,000 Elements
~ 600,000 DoFs
Hours of computation

VS.

Axisymmetric



25,000 Elements
~ 50,000 DoFs
Minutes of computation

Objective 1: Preprocessing

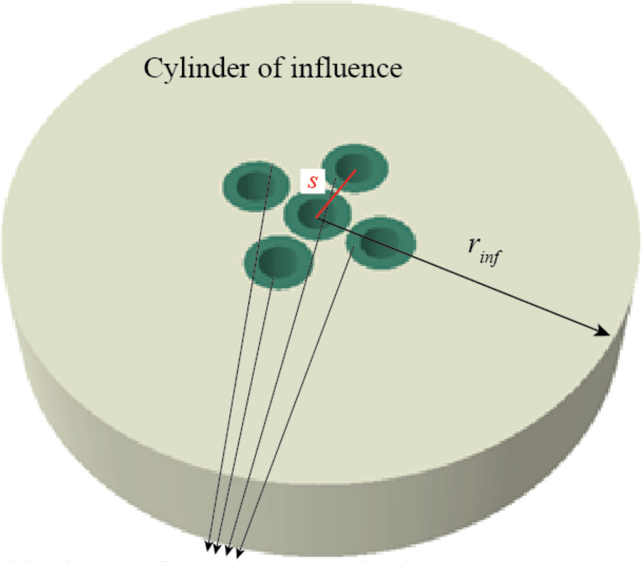
4) Capture the neighboring effect

- Save time (and money) by using axisymmetric model
- Challenge → Capture the neighboring effect in axisymmetric model
- Idea → Replace copper within cylinder of influence with equivalent material
  - Use rule of mixture to compute the material properties

$$E_e = v_1 E_1 + v_2 E_2$$

$$\alpha_e = \frac{1}{v_1 + v_2} \frac{v_1 E_1 \alpha_1 + v_2 E_2 \alpha_2}{v_1 E_1 + v_2 E_2}$$

- E_1, α_1, v_1 → Copper properties
- E_2, α_2, v_2 → Laminate/resin properties
- v_1, v_2 → Volume fractions



Neighboring configurations contributing to the copper content in the vicinity of the configuration that is being analyzed

Objective 1: Preprocessing

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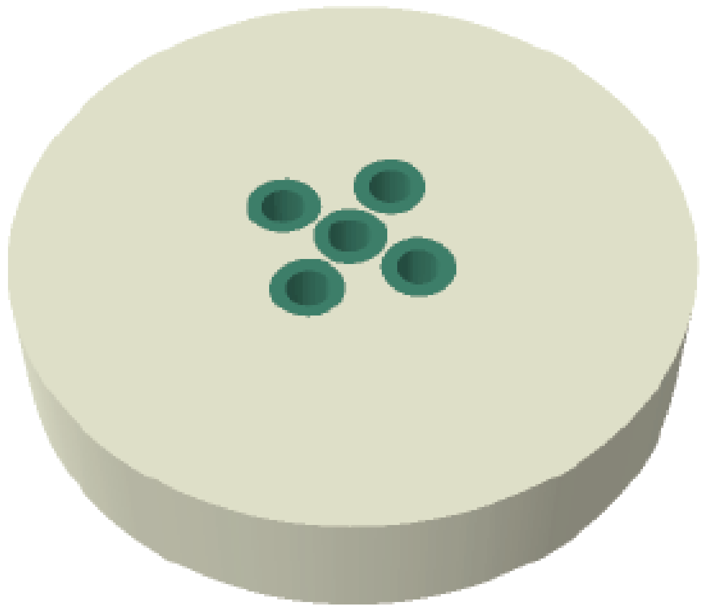
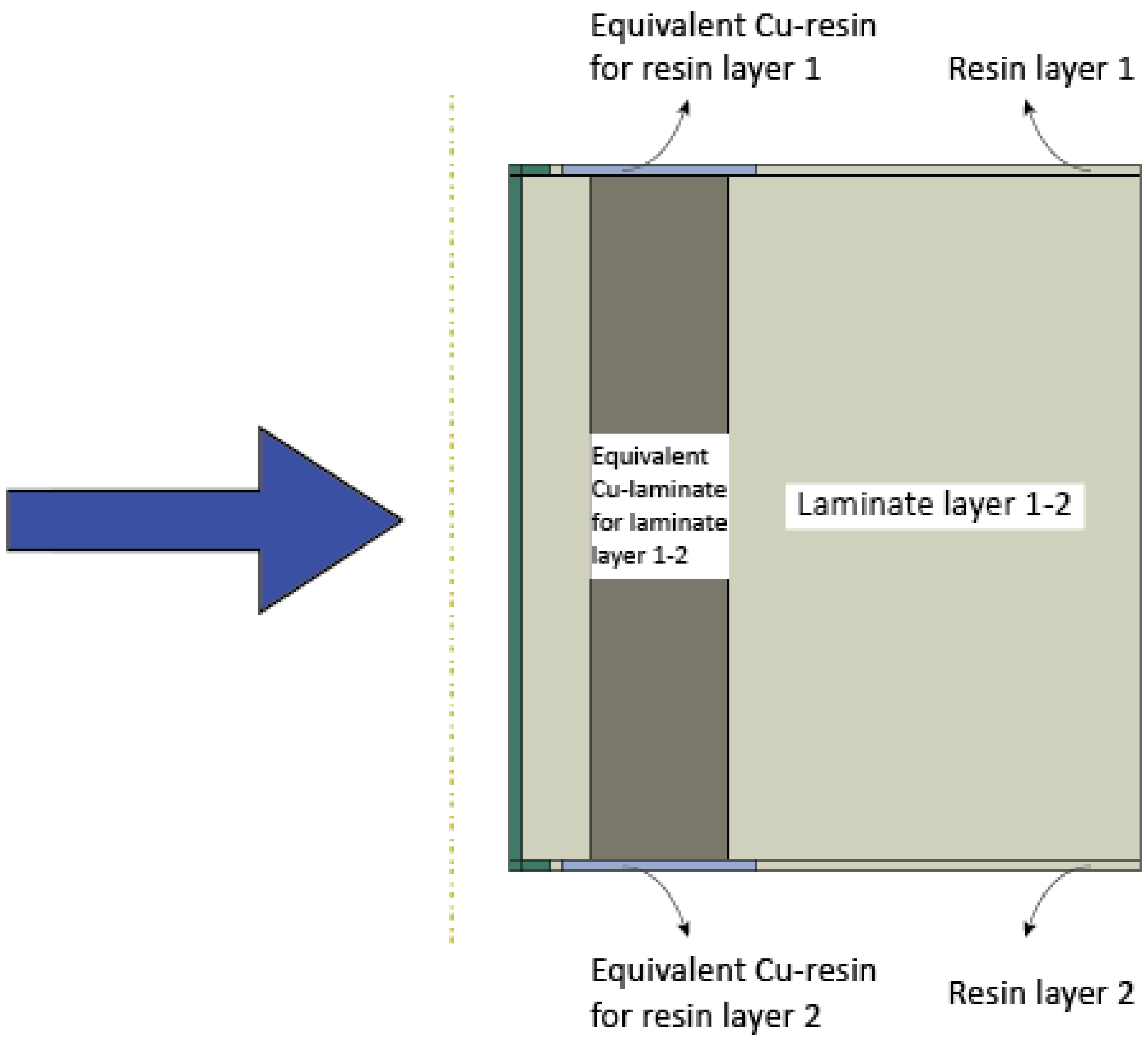
4) Capture the neighboring effect





Objective 1: Preprocessing

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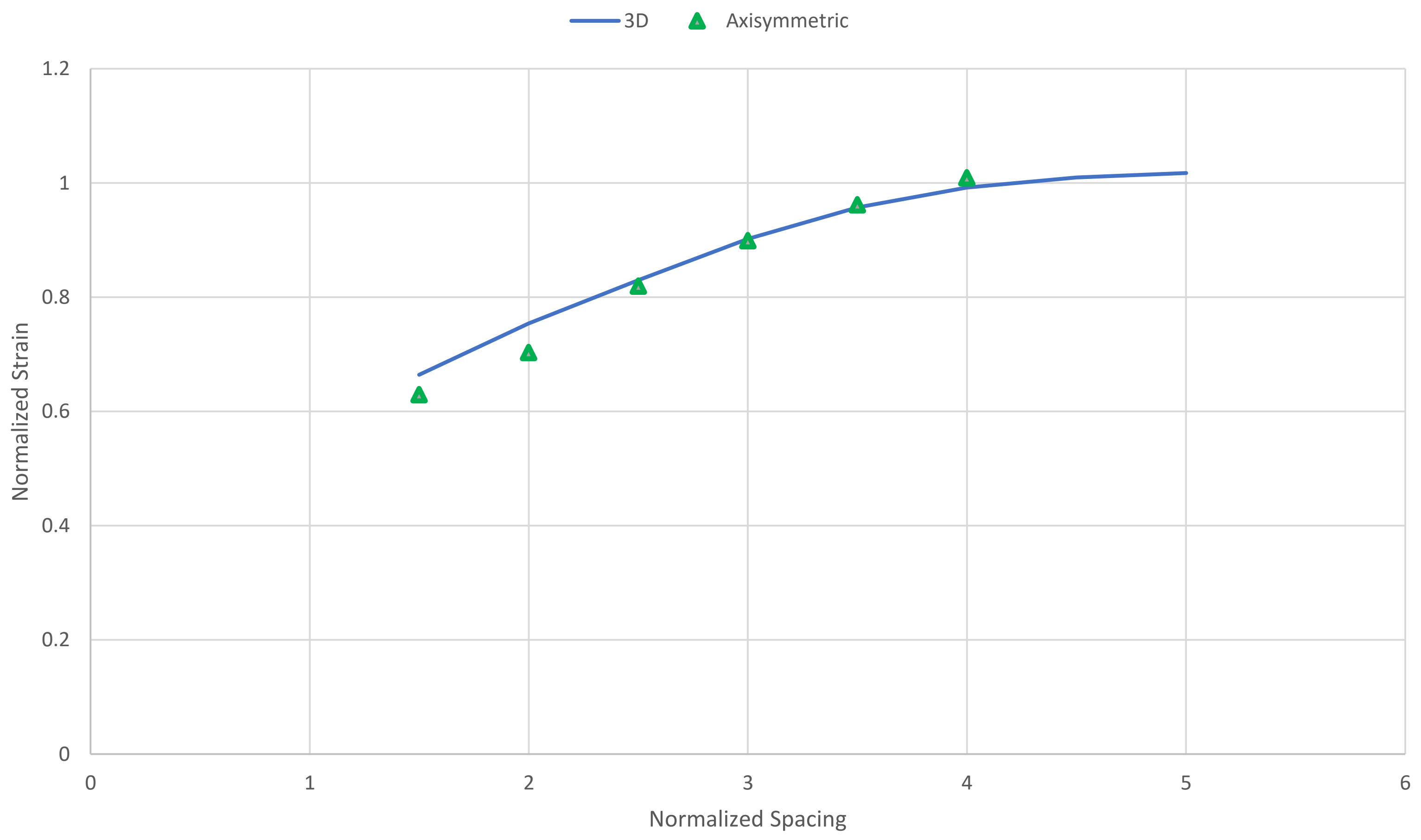
4) Capture the neighboring effect



Objective 1: Preprocessing

- 5) Collect the parameters (geometrical and material) required for FEA
  - totalNumLayers = 8
  - capLayers = (1, 2, 3, 4, 5, 6, 7, 8)
  - mvLayers = (1, 2, 3, 4, 5, 6, 7)
  - lamLayers = ()
  - bvStartLayers = ()
  - bvEndLayers = ()
  - cuSegLayers = ()
  - lamLayerT = ()
  - bvFilling = ()
  - cuSegInnerD = ()
  - cuSegOuterD = ()
  - capD = 8 * (0.3,)
  - capT = 8 * (0.025,)
  - mvBodyTopD = (0.1, 0.1, 0.1, 0.1, 0.09, 0.09, 0.09)
  - mvBodyBotD = (0.09, 0.09, 0.09, 0.09, 0.1, 0.1, 0.1)
  - mvBodyT = 7 * (0.1,)
  - bvInnerD = ()
  - bvOuterD = ()
  - bvTopPlatD = ()
  - bvBotPlatT = ()
  - bvLamLayT = ()
  - bvRingD = ()
  - bvRingT = ()
  - boardSize = 10 * max(bvInnerD)
  - …

Objective 2

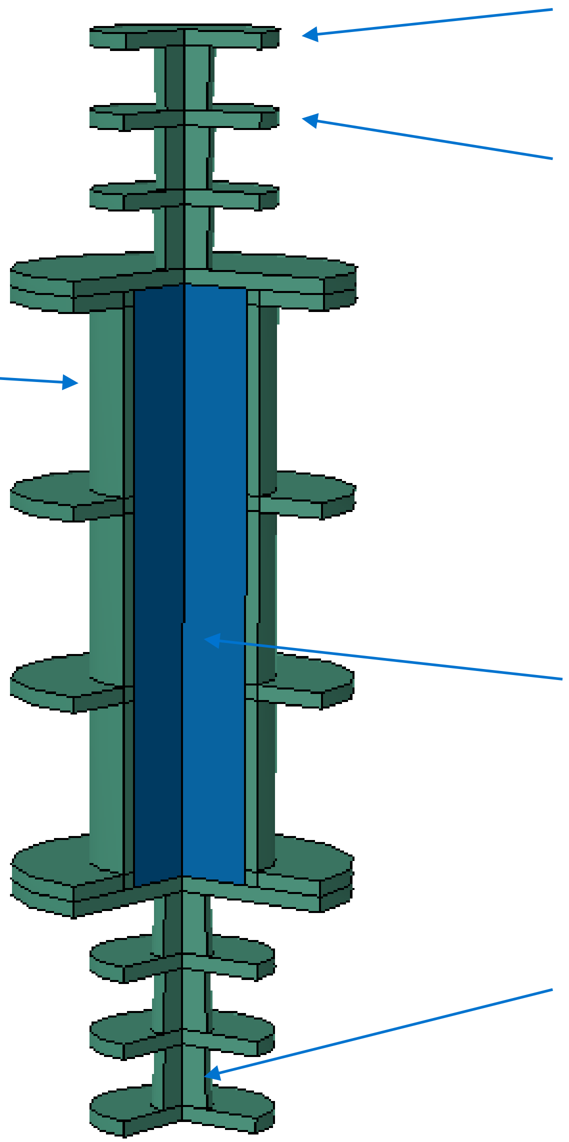
FE Automated Scripting

Objective 2: FE Automated Scripting

- The FE scripts should be capable of
  - Taking input parameters
  - Build a related FE model
  - Run the FE model under required thermal loading
  - Export the engineering results for postprocessing

Objective 2: FE Automated Scripting

- Example
  - 3 + 4 + 3 stacked



Microvia capture pad

Microvia target pad

Buried via

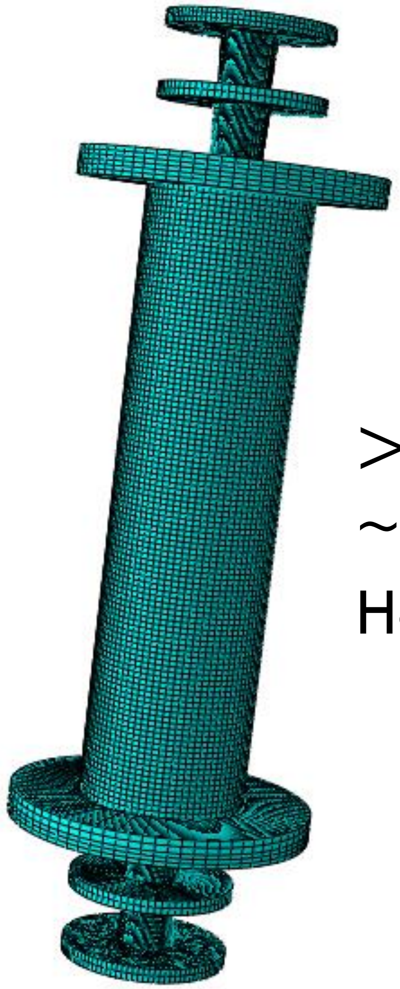
Buried via internal pads

Buried via filling

Copper filled microvia

Objective 2: FE Automated Scripting

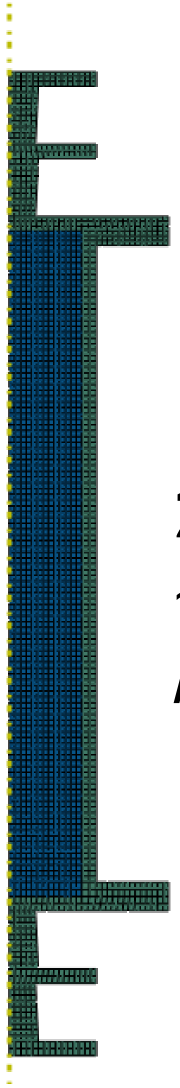
3D



> 200,000 Elements
~ 600,000 DoFs
Hours of computation

VS.

Axisymmetric



25,000 Elements
~ 50,000 DoFs
Minutes of computation

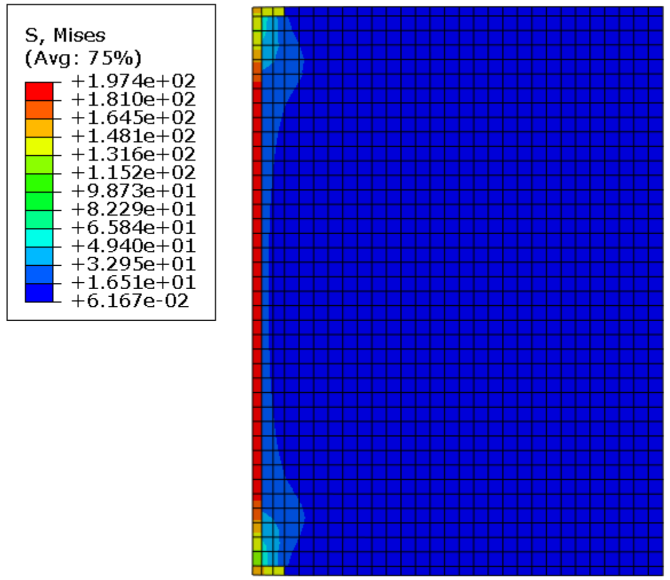
Objective 2: FE Automated Scripting

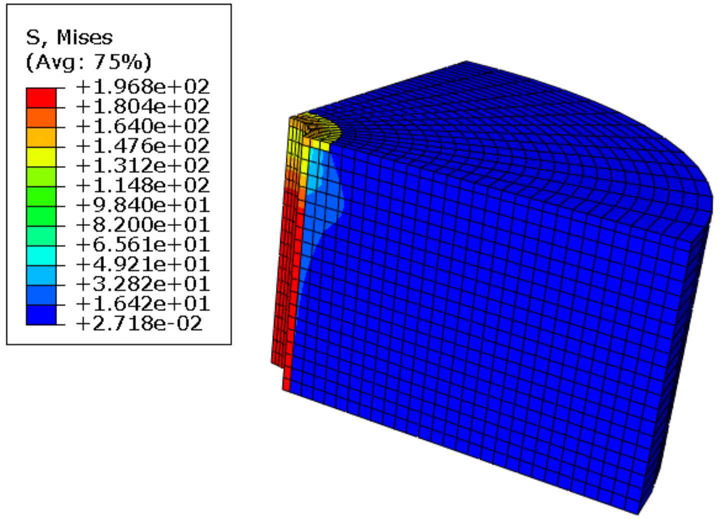
Axisymmetric vs. 3D Modeling

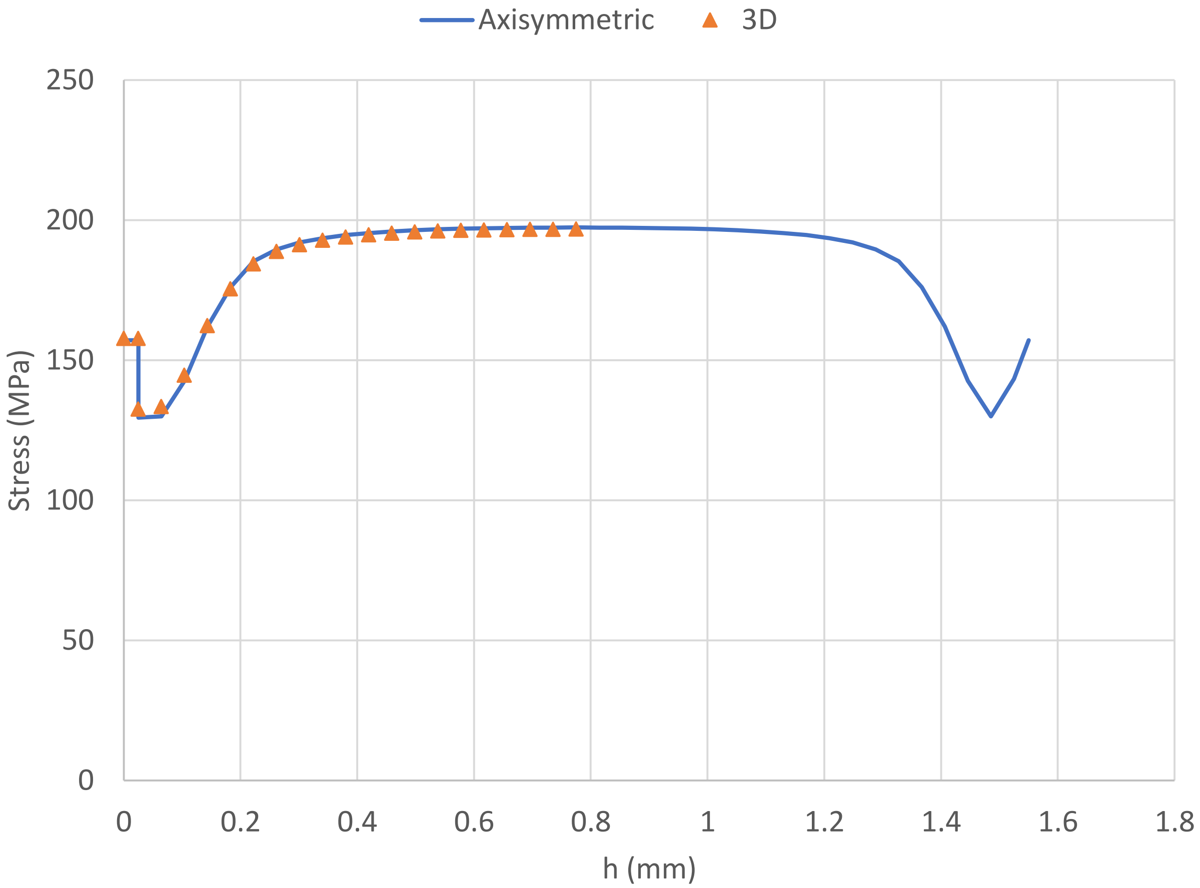
- Geometrical Parameters
  - Hole diameter, $d_o = 0.3$ mm
  - Pad diameters, $d_p = 0.425$ mm
  - Plating thickness, $t = 0.025$ mm
  - PTH inner diameter $\rightarrow d_i = d_o - 2t = 0.25$ mm
  - Board thickness, $T = 1.55$ mm
  - Aspect ratio, $T/d_o \approx 5.2$
  - Board diameter, $d_b = 10, d_i = 2.5 \text{ mm}$
- Loading
  - -55 → 135 C
- Mesh properties
  - 1 element across the thickness
  - Linear elements

Objective 2: FE Automated Scripting

- Axisymmetric vs. 3D Modeling





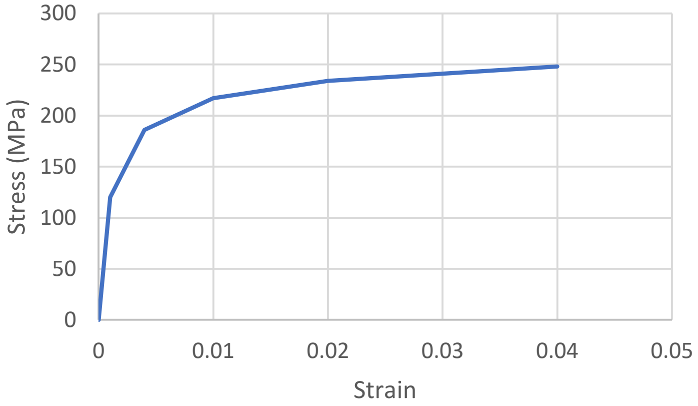


Objective 2: FE Automated Scripting

- Material model
  - Lack of reliable, universal material model for electrodeposited copper
    - Young’s modulus varies from $E = 23 \rightarrow 130 \text{ GPa}$
    - Yield stress varies from $\sigma_y = 70 \rightarrow 310 \text{ MPa}$
    - Micro-scale of the plated copper can influence its grain morphology → Significant difference with bulk copper
  - Copper material model is one of the most critical factors in reliability of the results e.g.,
    - Using annealed copper properties (soft copper, $\sigma_y \approx 40 \text{ MPa}$) result in insensitivity of FEM model to hole diameter
    - The effect of inner planes are influenced by plasticity property of copper and orthotropic properties of PCB

Objective 2: FE Automated Scripting

- Copper
  - Nonlinear elastic-plastic material model with kinematic hardening
  - $E = 121$ GPa
  - $\sigma_y = 120$ MPa at 0%
  - $\alpha = 17.6\ \mathrm{ppm/°C}$



- FR4
  - Orthotropic material
  - Young's moduli
    $E_1 = E_3 = 13.6\ \mathrm{GPa}$
    $E_2 = 6.6\ \mathrm{GPa}$
  - Poisson's ratios
    $\nu_{12} = \nu_{23} = 0.4$
    $\nu_{13} = 0.14$
  - Shear moduli
    $G_{12} = G_{23} = 5070\ \mathrm{MPa}$
    $G_{13} = 2170\ \mathrm{MPa}$
  - CTEs
    $\alpha_{11} = \alpha_{33} = 13.5\ \mathrm{ppm/°C}$
    $\alpha_{22} = 55\ \mathrm{ppm/°C}$
  - T_g effects for reflow simulations
    $T_g = 130 \rightarrow 180°\mathrm{C}$

- Resin
  - Linear elastic
  - $E = 5\ \mathrm{GPa}$
  - $\nu = 0.34$
  - $\alpha = 55\ \mathrm{ppm/°C}$
  - T_g effects for reflow simulations
    $T_g = 130 \rightarrow 180°\mathrm{C}$

Objective 2: FE Automated Scripting

- FR4 Material Properties for Different Temperatures

T(˚C)	E_L (MPa)	E_T (MPa)	v_{LL}	v_{LT}	G_{LL} (MPa)	G_{LT} (MPa)
-50	15,000	7,100	0.14	0.4	6,600	3,100
25	13,600	6,600	0.14	0.4	6,000	2,900
100	13,500	6,000	0.14	0.4	5,900	2,600
150	12,500	5,600	0.14	0.4	5,500	2,500
160	11,000	5,200	0.14	0.4	4,800	2,300
170	9,600	4,600	0.14	0.4	4,200	2,000
180	5,400	2,600	0.14	0.4	2,400	1,100

L is in-plane direction
T is the through-thickness direction

T(˚C)	α_{LL} (10^{-6}/˚C)	α_{TT} (10^{-6}/˚C)
-55	13.5	55
177	13.5	55
178	15.5	250
200	15.5	250

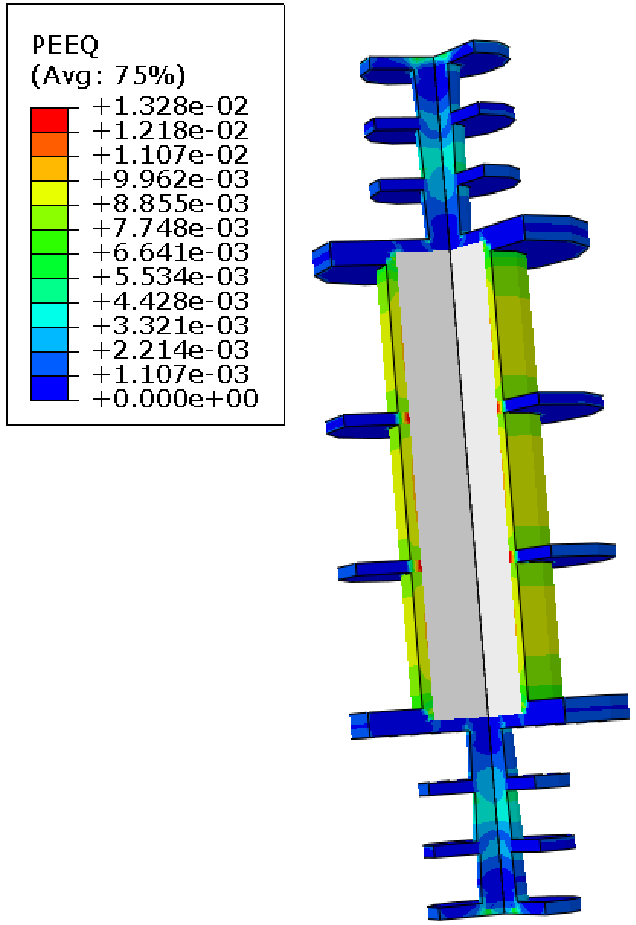
- Resin Material Properties for Different Temperatures

T(˚C)	E (MPa)	v
-50	7200	0.325
25	6600	0.325
70	4500	0.325
100	3300	0.325
150	1300	0.325
200	1300	0.325

T(˚C)	α (10^{-6}/˚C)
-55	56
177	56
178	250
200	250

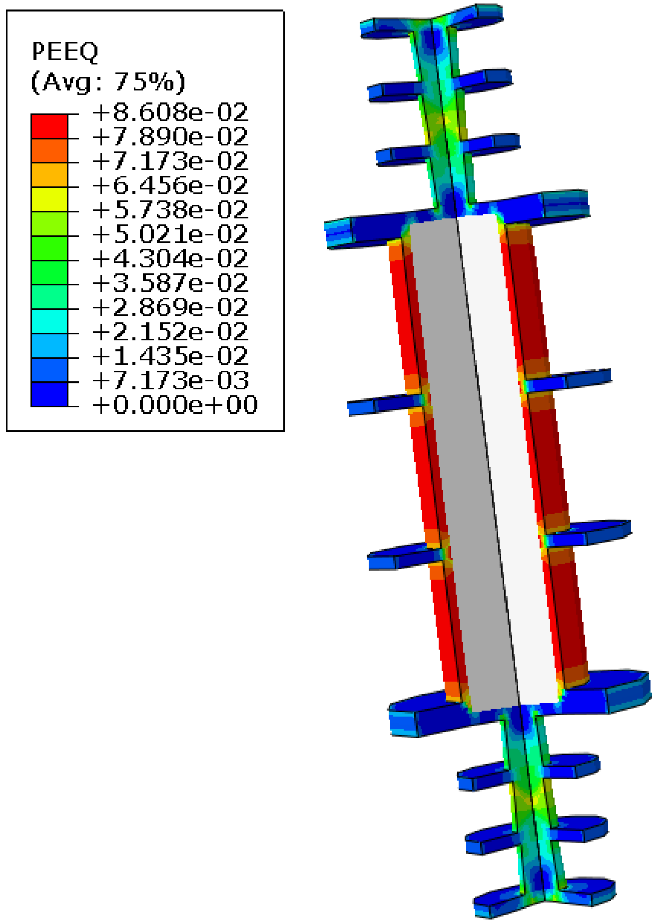
Objective 2: FE Automated Scripting

- Without T_g effect



25°C→250°C

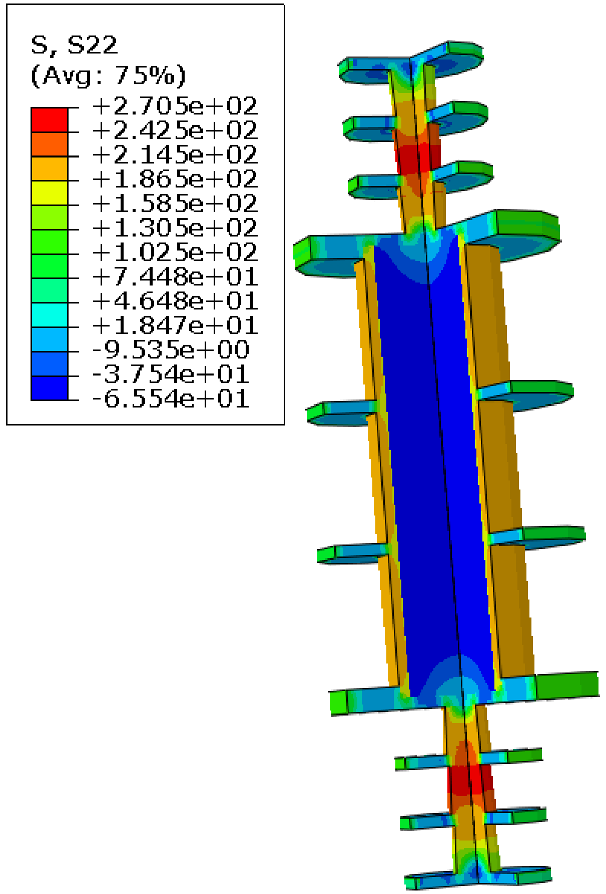
- With T_g effect



25°C→250°C

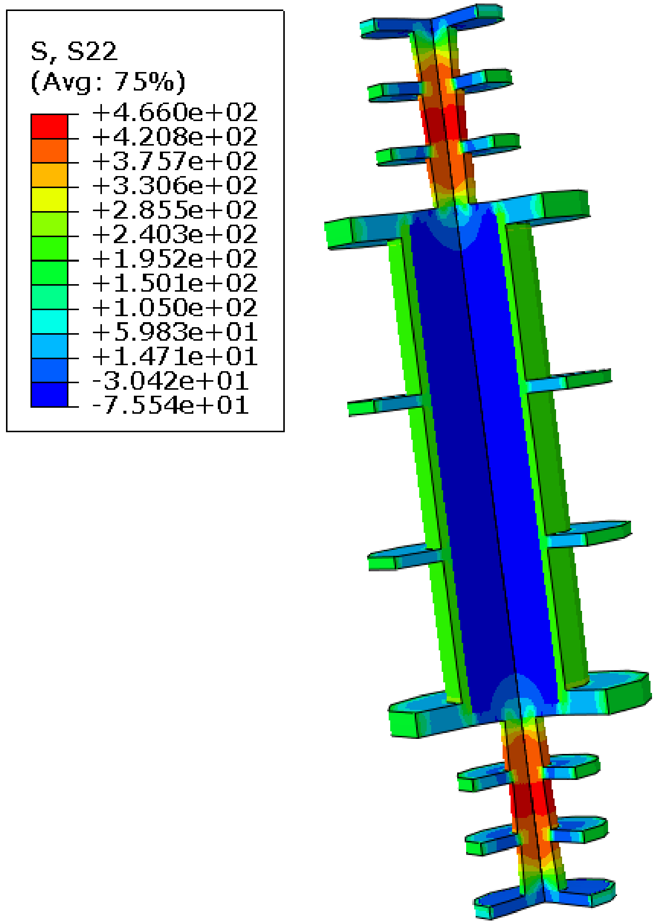
Objective 2: FE Automated Scripting

- Without T_g effect



25°C→250°C

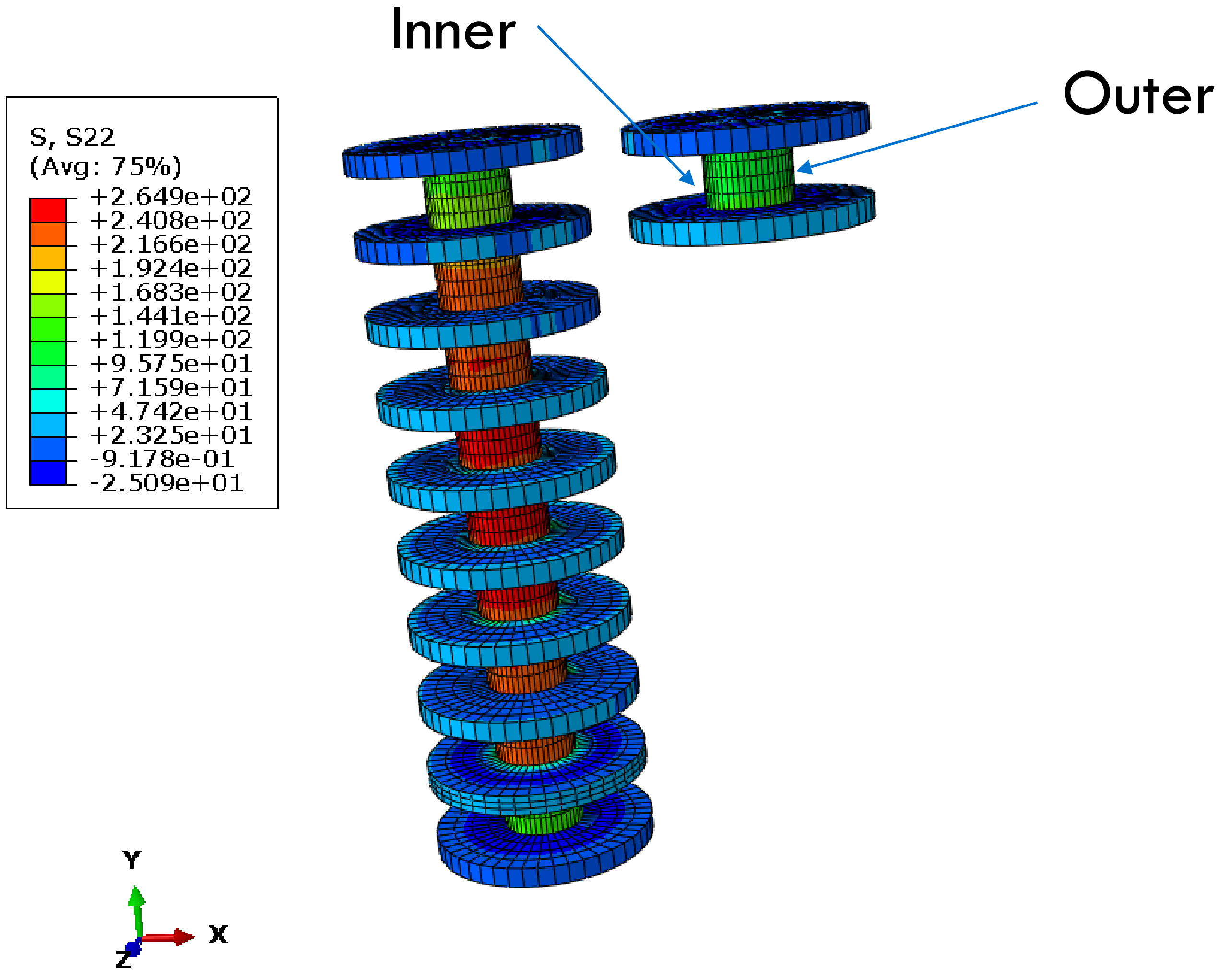
- With T_g effect

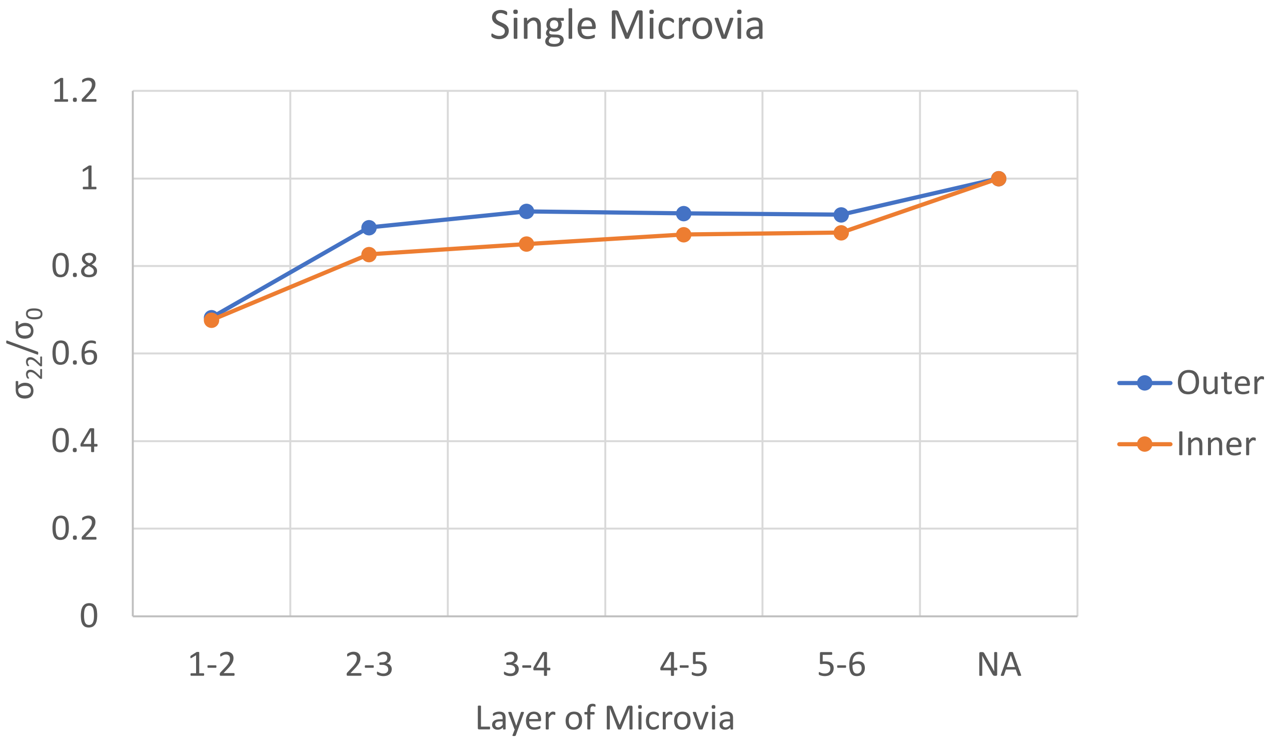


25°C→250°C

Objective 2: FE Automated Scripting

- Parametric study on microvia placement

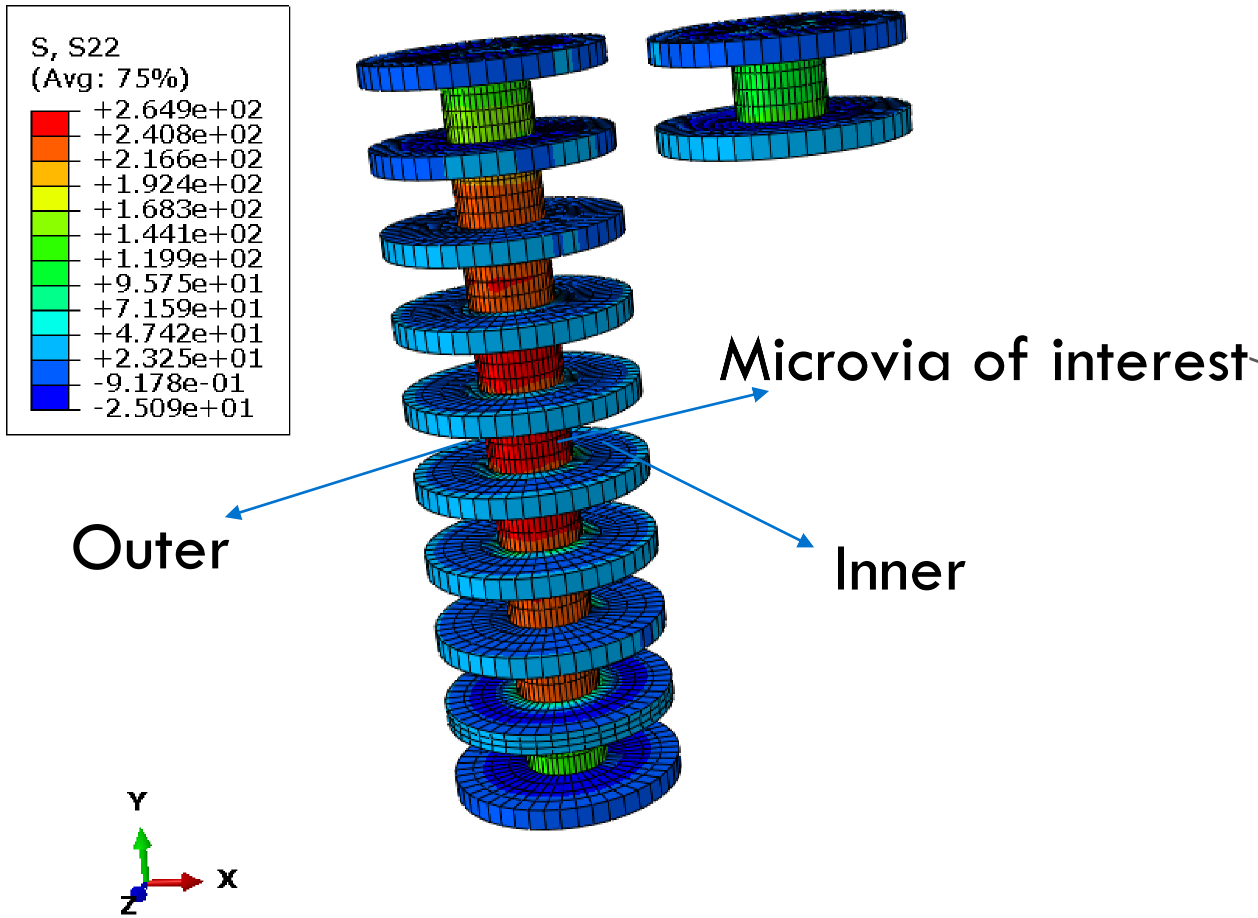


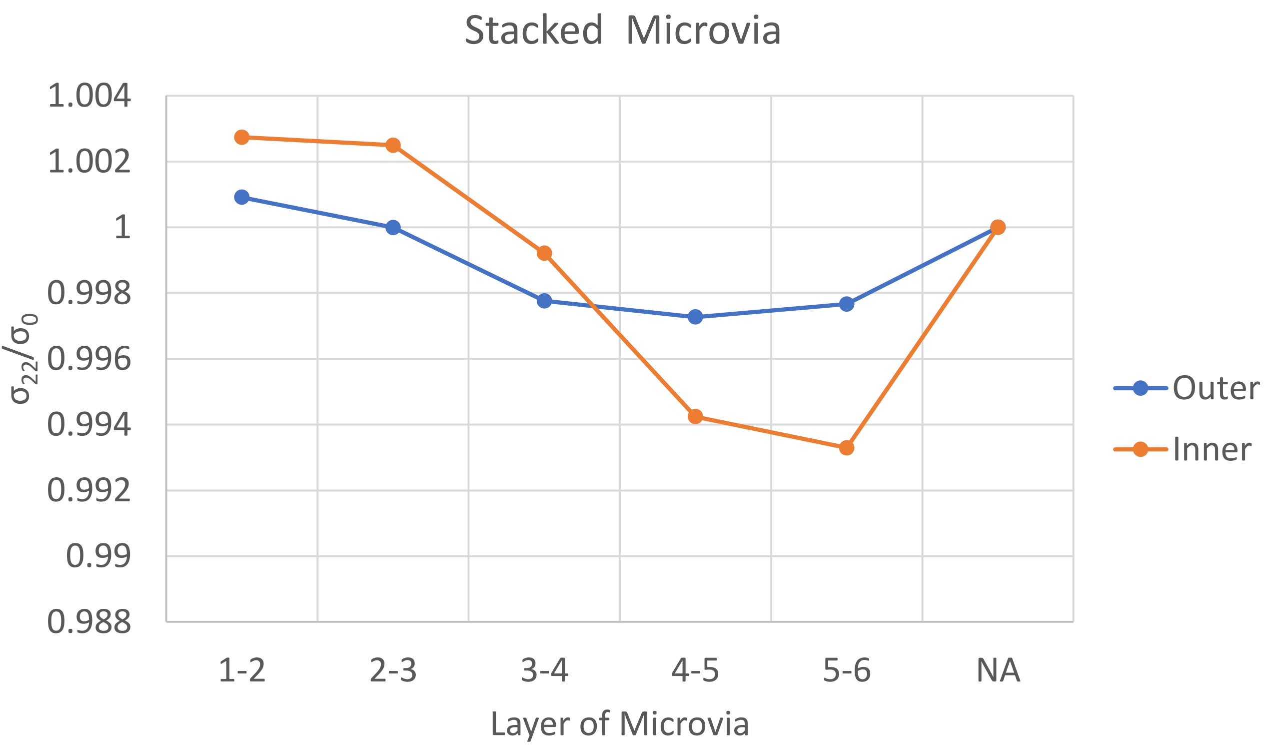


σ_0 is 22 stress component in the single microvia without any neighboring configuration

Objective 2: FE Automated Scripting

- Parametric study on microvia placement





σ_0 is 22 stress component in the microvia between layers 5 and 6 in the stacked configuration without any neighboring configuration

Objective 2: FE Automated Scripting

- Assumptions consistent with the literature
  - No manufacturing defects
  - Plated copper consists of electrodeposited copper only (no electroless copper, no nickel, …)
  - No temperature dependency for copper
  - Uniform temperature across the PCB (the heat transfer within the PCB is not considered)

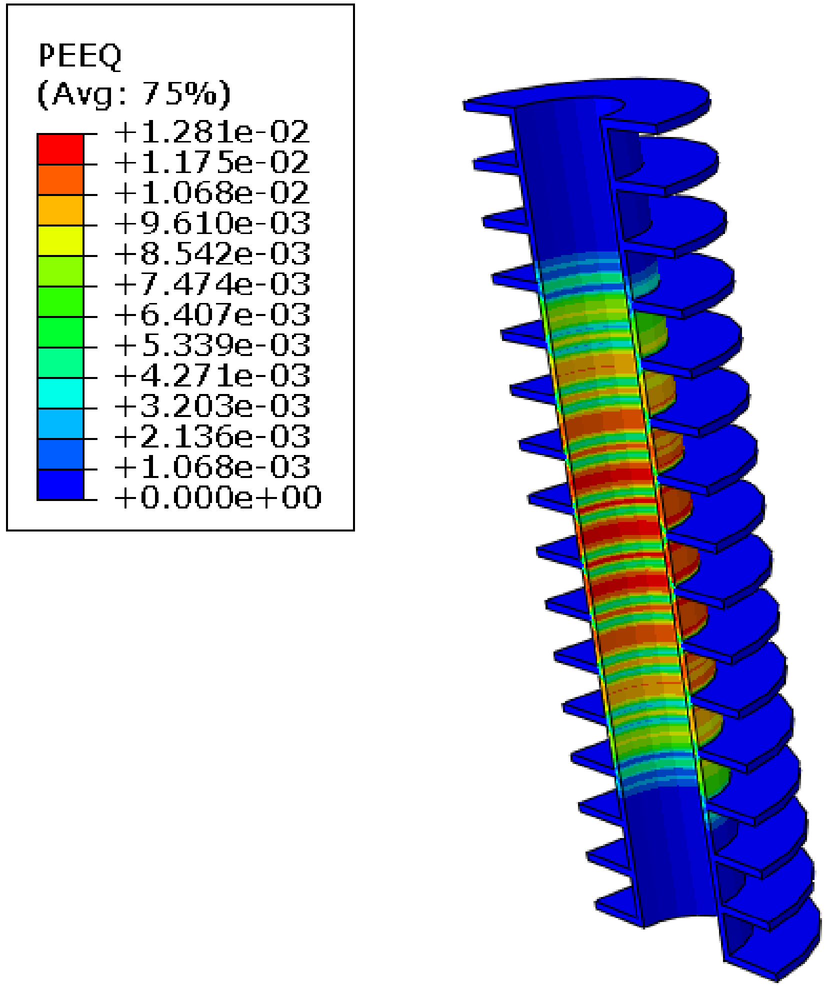
Objective 3

Postprocessing of FEA Results

Reliability Analysis of PTHs

Objective 3: Postprocessing of FEA Results

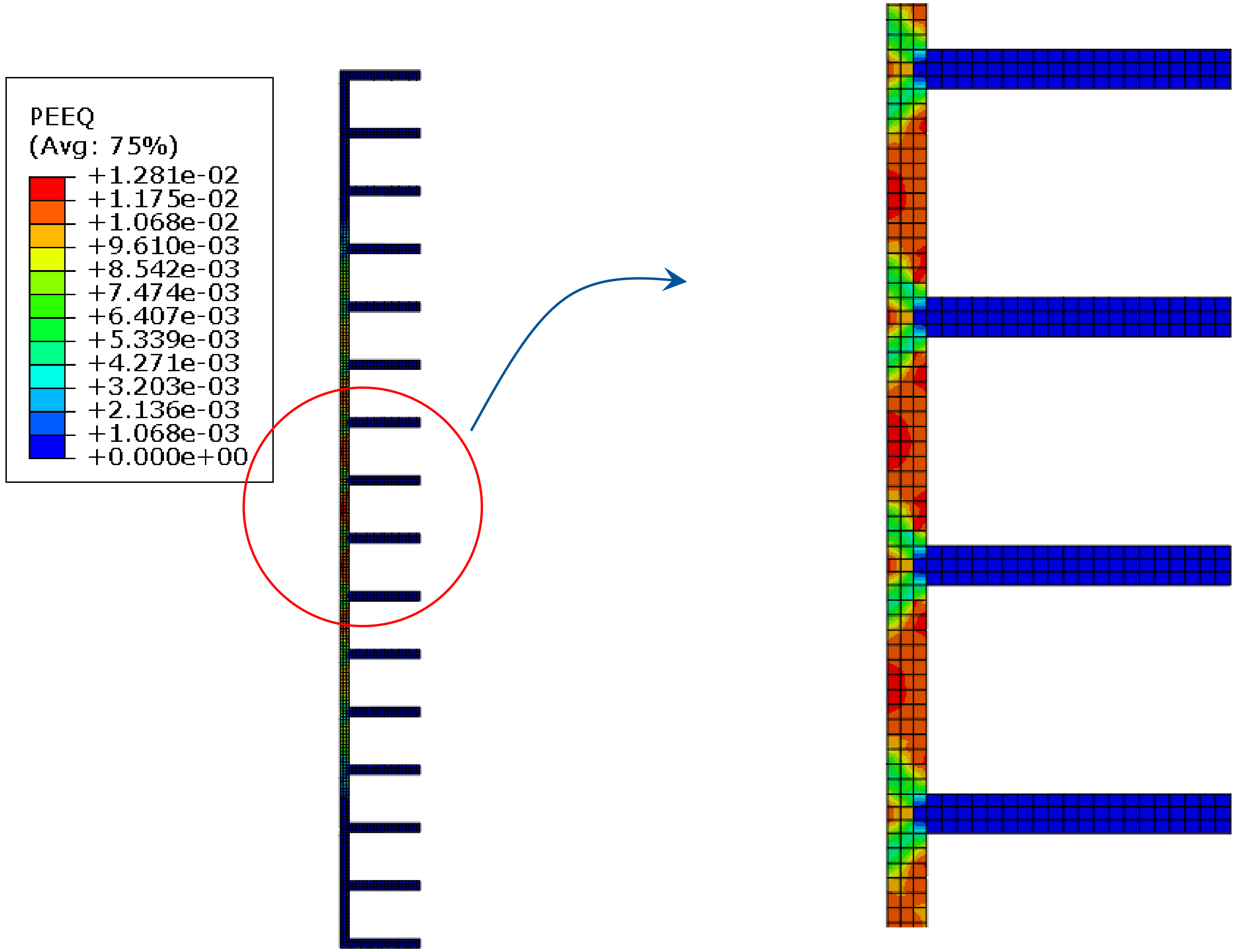
- Reliability analysis of PTHs
  - Equivalent plastic strain



0 → 100°C Example

Objective 3: Postprocessing of FEA Results

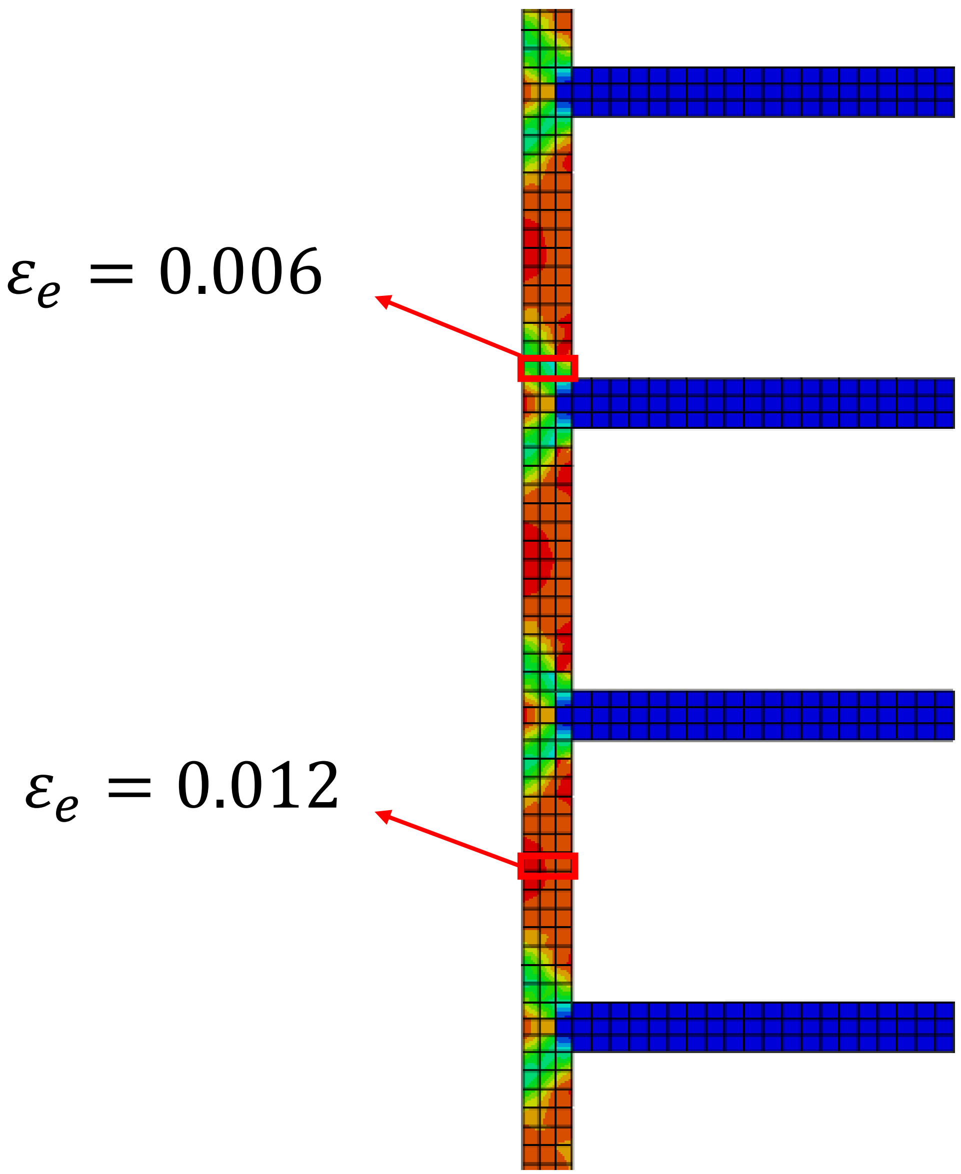
- Reliability analysis of PTHs
  - Equivalent plastic strain



Objective 3: Postprocessing of FEA Results

2019 DESIGN FOR RELIABILITY CONFERENCE

- Reliability analysis of PTHs
  - Average the equivalent plastic strain across thickness of the PTH barrel



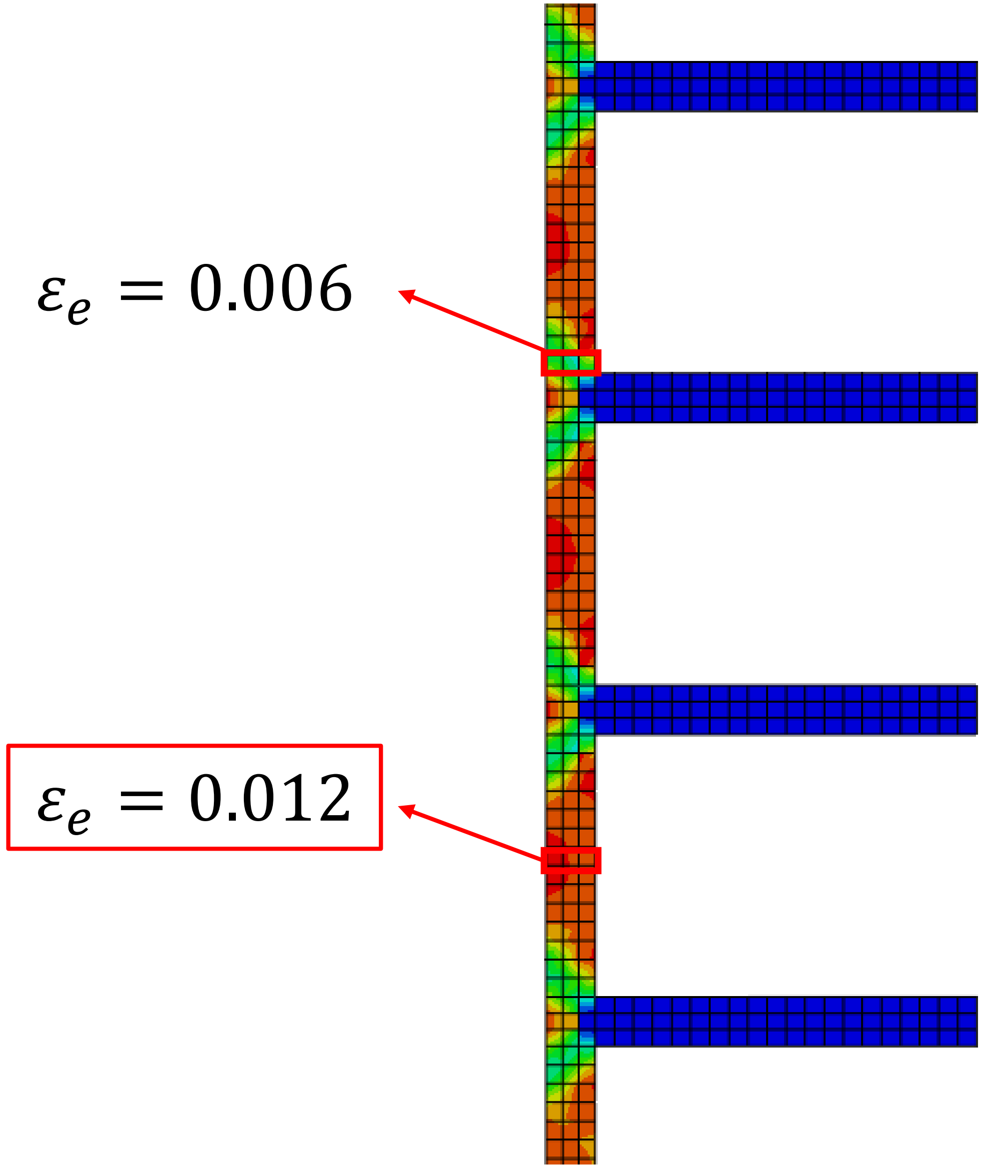
$\varepsilon_e = 0.006$

$\varepsilon_e = 0.012$

Objective 3: Postprocessing of FEA Results

- Reliability analysis of PTHs
  - Average the equivalent plastic strain across thickness of the PTH barrel
  - Pick the maximum
  - Compute the average equivalent plastic strain increment, $\Delta\varepsilon$
  - Use Coffin-Manson equation to estimate the life cycle to failure

$$N_f = \frac{1}{2}\left(\frac{\Delta\varepsilon}{2\varepsilon_f}\right)^{1/c}, \quad \varepsilon_f = 0.3, \; c = -0.6$$

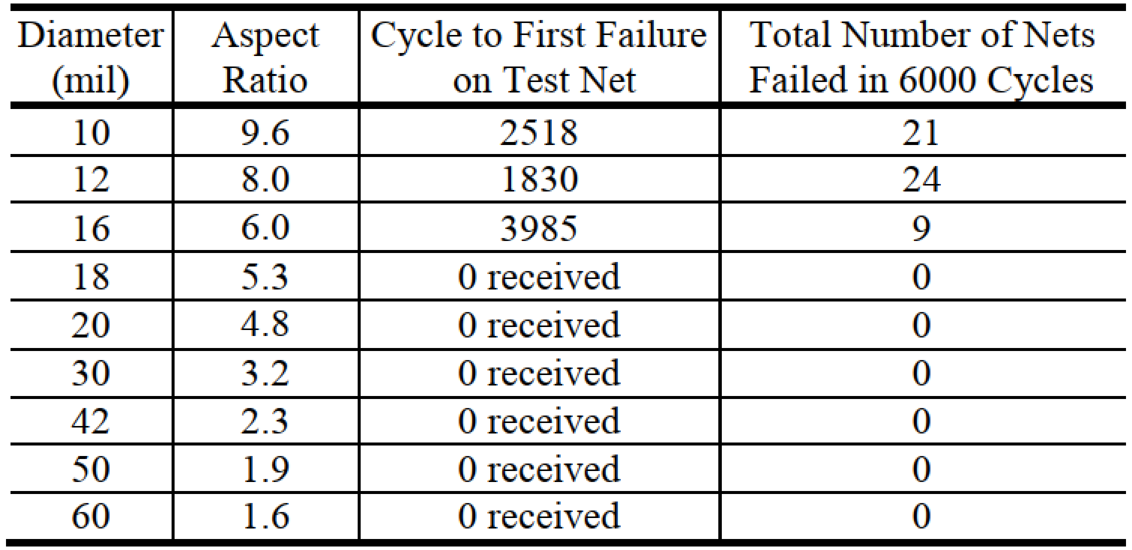


$\varepsilon_e = 0.006$

$\boxed{\varepsilon_e = 0.012}$

Objective 3: Postprocessing of FEA Results

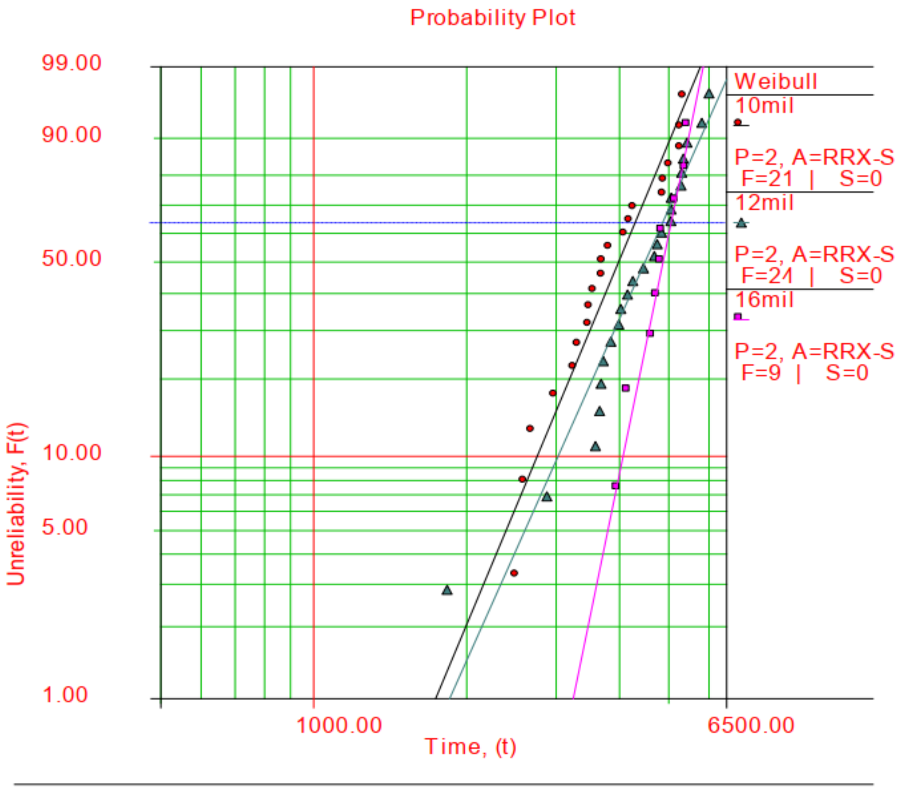
- Validating the PTH model with experimental results by Wu et al.
  - 16-layer MLB
  - MLB thickness of 96 mil
  - Hole diameters of 10 to 60 mil (9 configurations)
  - Plating thickness of 1 mil
  - Thermal cycling 0 → 100°C



Diameter (mil)	Aspect Ratio	Cycle to First Failure on Test Net	Total Number of Nets Failed in 6000 Cycles
10	9.6	2518	21
12	8.0	1830	24
16	6.0	3985	9
18	5.3	0 received	0
20	4.8	0 received	0
30	3.2	0 received	0
42	2.3	0 received	0
50	1.9	0 received	0
60	1.6	0 received	0

Wu, Jing-Han, Liao Meng-Chieh, Luo Tzeng-Cherng, and Huang Te-Chun. 2011. “Comparison the Reliability of Small Plated-through Hole with Different Diameters under Thermal Stress.” In . IEEE.

Objective 3: Postprocessing of FEA Results



Diameter (mil)	Weibull Parameters and MTTF		
parameter	β	η	MTTF
10	4.92	4307	3932
12	5.70	4808	4439
16	11.89	5037	4807

Objective 3: Postprocessing of FEA Results

- Experimental setup used in
  - 32 boards
  - 9 net on each board (for each hole diameter considered)
  - 10 hole in each net
  - → 320 holes for each configuration
  - Statistical analysis are performed based on first cycle to failure without considering
    - how many holes failed in each daisy chain
    - how many holes did not fail (suspensions)
  - Conclusion ⇒ Not the best statistical analysis
  - Common issue with almost all of the works in the literature
  - Solution ⇒ Redo the statistical analysis

Objective 3: Postprocessing of FEA Results

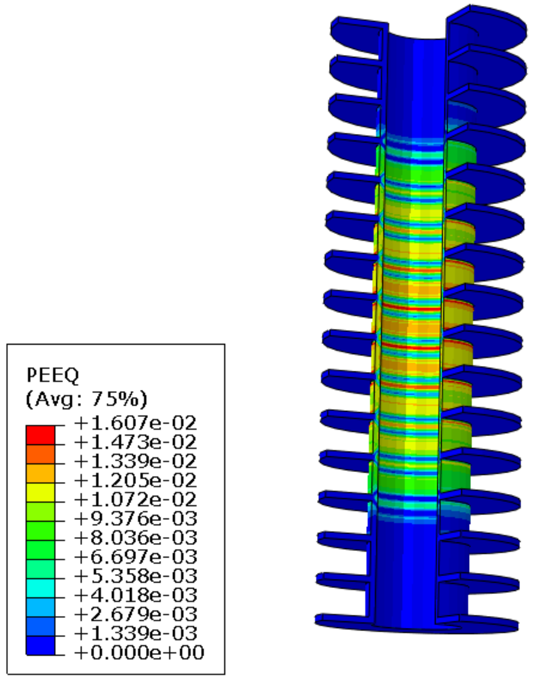
- Redo the statistical analysis considering
  - 320 holes for each configuration
  - Assuming 6 holes of 10 mil diameter fail at the same time on each board
  - Assuming 4 holes of 12 mil diameter fail at the same time on each board
  - Assuming 1 hole of 16 mil diameter fail at the same time on each board
  - With suspensions

Objective 3: Postprocessing of FEA Results

	$\Delta\varepsilon$ (Model prediction)	N_f (Model prediction)	N_f (Experimental results^2)	N_f (Experimental results^1)
Case 1 (10 mil)	2.1931E-3	5765	5839	4307
Case 2 (12 mil)	2.0269E-3	6574	6805	4808
Case 3 (16 mil)	1.7839e-3	8133	8347	5037

1 Characteristic life cycle reported based on cycle to first failure on each daisy chain
2 Characteristic life cycle estimated considering suspended data points

- Takeaways
  - Lack of reliable experimental results in the literature
  - Lack of reliable statistical analysis
    - Long daisy chains with first cycle to failure reports only
    - No suspensions considerations
    - …



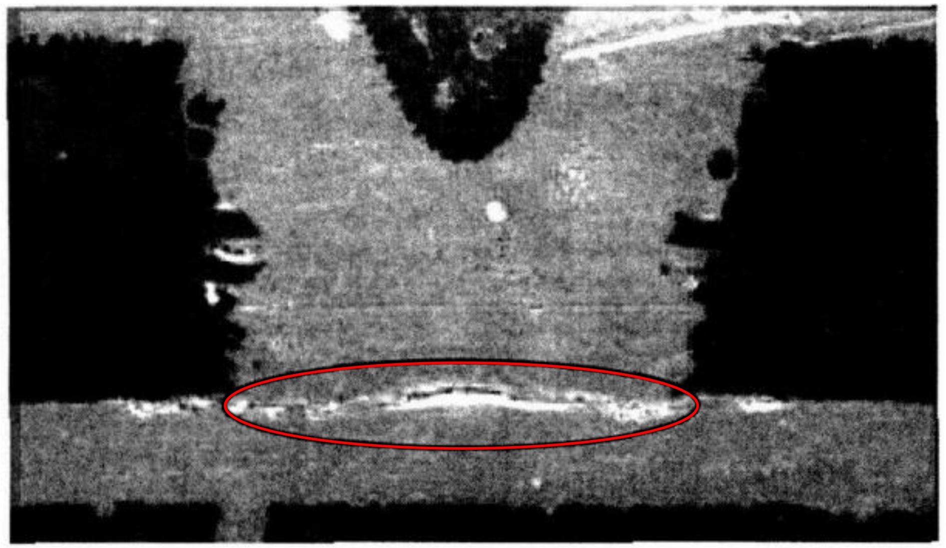
Objective 3

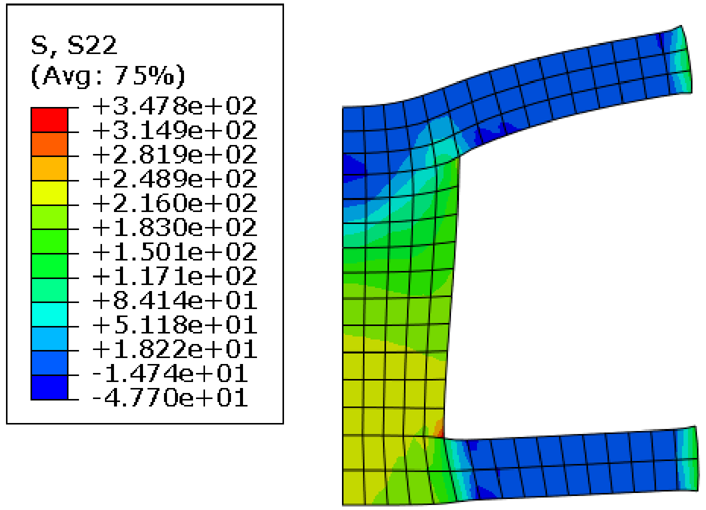
Postprocessing of FEA Results

Manufacturability Analysis of Stacked Microvias

Objective 3: Postprocessing of FEA Results

- Manufacturability analysis on stacked microvias
  - Tensile overstress
  - Interfacial separation between microvia body and target/capture pads



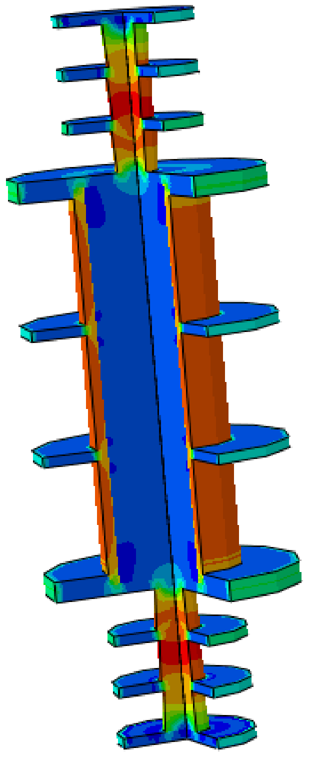


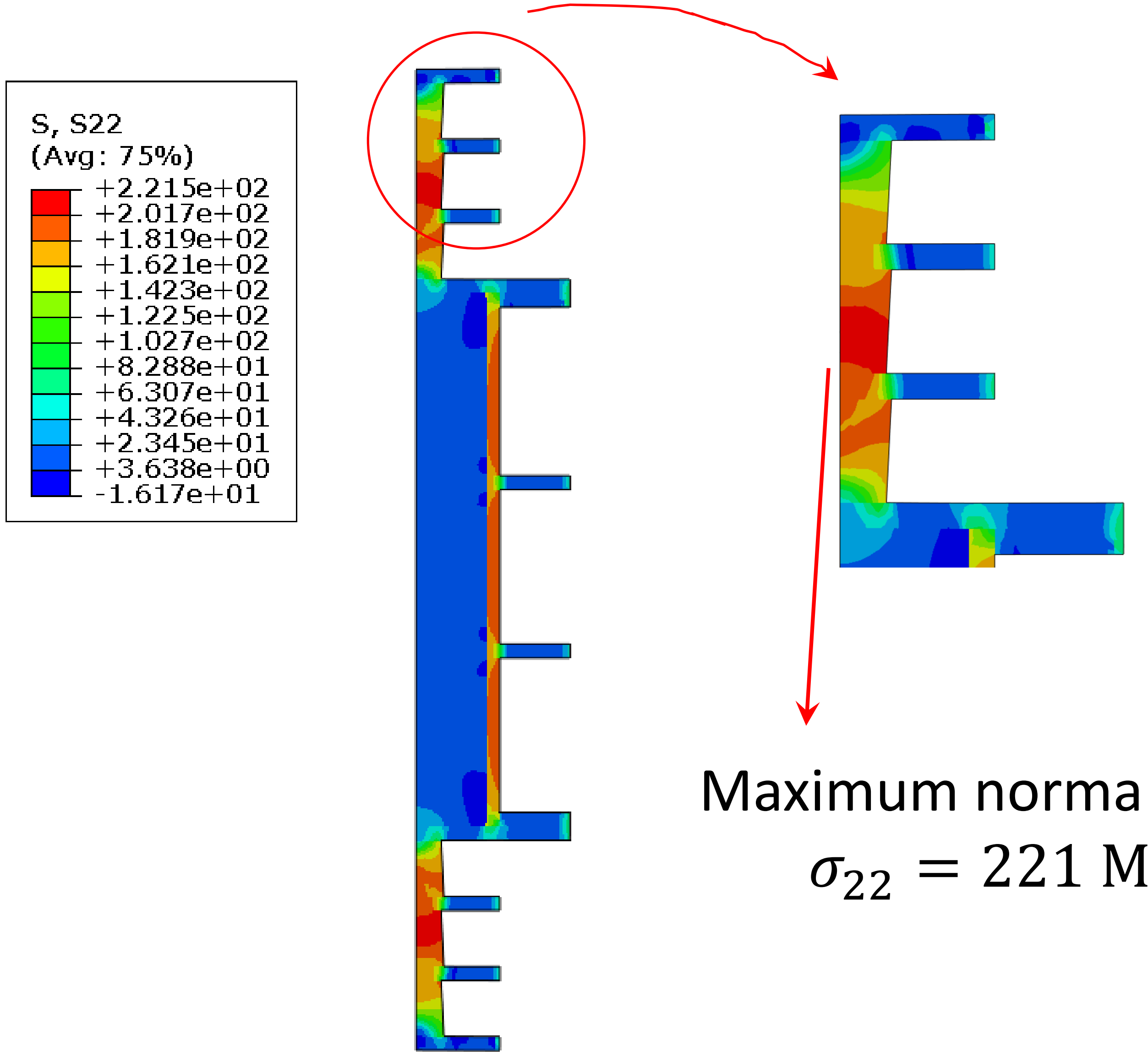
Objective 3: Postprocessing of FEA Results

- Manufacturability analysis on stacked microvias
  - Based on in-house experimental results and copper properties
    - $\sigma_{22} < 120\ \mathrm{MPa} \rightarrow$ Pass
    - $120\ \mathrm{MPa} \leq \sigma_{22} < 160\ \mathrm{MPa} \rightarrow$ Need attention
    - $160\ \mathrm{MPa} \leq \sigma_{22} \rightarrow$ Failure

Objective 3: Postprocessing of FEA Results

- Example
  - $3 + 4 + 3$
  - $25°\mathrm{C} \rightarrow 150°\mathrm{C}$



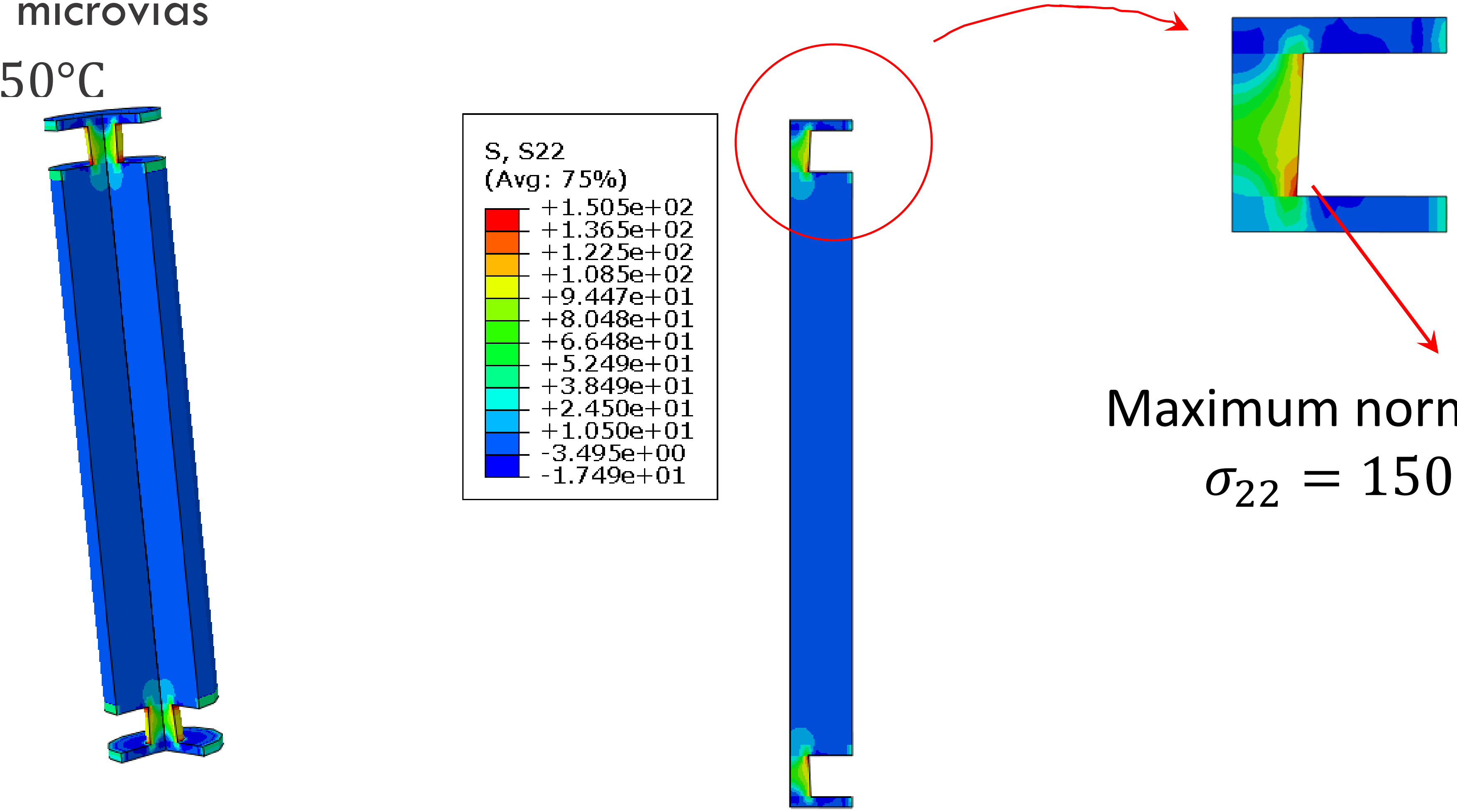


Maximum normal stress

$\sigma_{22} = 221\ \mathrm{MPa}$

Objective 3: Postprocessing of FEA Results

- Example
  - Two single microvias
  - $25°C \rightarrow 150°C$



Maximum normal stress
$\sigma_{22} = 150 \text{ MPa}$

Conclusions

- A fully automated methodology is developed for implementation in Sherlock to analyze a board with many interconnect structures
- Thermal stress due to CTE mismatch between board and copper is the dominant driving force for failure of these interconnects
- Staggered microvias are less of a concern due to their low aspect ratio (topic of future studies)
- Increasing density of interconnects tends to increase their robustness (manufacturing limitations)
- Two main failure mechanisms
  - Interfacial separation in microvias due to overstress during reflow
  - Barrel cracking in PTHs due to fatigue during field usage
- Axisymmetric conditions can be used to model stacked microvia and PTHs configurations
- Nearest-neighbor effect can be captured in the axisymmetric model by using equivalent material properties and rule of mixture

Bio Slide

Dr. Kourosh Kalayeh

As a Research Engineer, Dr. Kalayeh leverages his expertise in mechanical engineering to further develop DfR Solutions' failure prediction capabilities. Dr. Kalayeh has published research with organizations such the Institute of Electrical and Electronics Engineers (IEEE), the International Journal for Non-linear Mechanics, and Sensors. He studied for his PhD in Mechanical Engineering at the University of Maryland, Baltimore County.

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Dr. Nathan Blattau, Senior VP at DfR Solutions

Dr. Blattau brings nearly a decade of experience in failure analysis, accelerated testing methods, electronic equipment packaging and reliability to DfR Solutions, bolstered by extensive, focused research in design for reliability (DfR) in electronic packaging, nonlinear finite element analysis, solder joint reliability, fracture and fatigue mechanics of materials.

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