iNEMI Project on Process Development of BiSn-Based Low Temperature Solder Pastes

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ABSTRACT

The 2017 iNEMI Board and Assembly Roadmap forecasts that, due to economic, environmental and technical drivers, use of low temperature solder pastes will increase significantly and reach 10% of all solder paste used for board assembly by 2021.

The Bi-Sn solder system is the primary target for low temperature soldering. To overcome potential drawbacks in the reliability of Bi-Sn solder joints caused by the inherent brittleness of the Bi-Sn eutectic solder composition, solder suppliers have developed new solder pastes adopting due distinct strategies. One is enhancing the ductility of the Bi-Sn alloy using fundamental metallurgical principles; the other is providing a polymeric reinforcement of the solder joint by incorporating resin in the solder paste.

To address the challenge of evaluating these new formulation solder pastes from multiple suppliers by determining their suitability in surface mount processing and resistance to mechanical shock and fatigue stresses, iNEMI initiated the BiSn-Based Low-Temperature Soldering Process and Reliability (LTSPR) Project, with 20+ member participants. This paper reports out the results from the initial phase of this project, which is assessing the processability of these solder pastes through surface mount soldering steps.

Five solder pastes from the ductile Bi-Sn solder paste category and four solder pastes from the Joint Reinforced Paste (JRP) resin containing solder paste category were evaluated. Three Bi-Sn eutectic composition pastes with Ag added in varying amounts and one SnAgCu (SAC) solder paste were also evaluated for comparison as the baseline pastes. The aspects of processability assessed were the printability, reflow profiling, solder joint yield and defects analysis, component removal and site re-dress in the rework operation and the surface insulation resistance (SIR) of the paste flux residue.

The results indicated the following. Ductile Bi-Sn paste and JRP pastes performed equivalent to the baseline Bi-Sn and SAC solder pastes over the range of stencil aperture area ratios studied, except that at the lowest aperture ratio of 0.50 the JRP resin paste have lower transfer efficiencies and coefficient of variation than the others. JRP resin pastes have a trapezoidal reflow profile topography in comparison to the ramp-soak-peak topography for the other category pastes. Initial ramp rate for JRP paste is critical to avoid premature gelling of the resin before the molten solder has full wetted the terminations. Partial wetting and non-wetting will occur if this ramp rate is lower than required. An unusual `hot tearing` solder joint defect was observed for Flip Chip Ball Grid Array (FCBGA) components. This hot tearing phenomena is caused by an interaction of the bismuth stratification at the package substrate interface, the FCBGA dynamic warpage characteristic as it cools down from the peak reflow temperatures and the cooling rate during reflow soldering. Hot Tearing was observed in solder joints formed with the four solder pastes that had the highest bismuth mixing level in the SAC ball.

A quantitative assessment by rework operators for removal of and subsequent site redress for FCBGA and QFN components showed that the lower melting temperature of the solder joints formed with Bi-Sn solder pastes facilitates easier part removal and site redress. All solder pastes passed the minimum requirement for the SIR measurement.

Key words: BGA solder joints, low temperature solder, Bi-Sn metallurgy, Mechanical shock reliability, Temperature cycle reliability, Polymeric reinforcement

INTRODUCTION

The advent of new and emerging product markets such as ultra-mobile computing and the Internet of Things (IoT) has driven the need for smaller, thinner and highly integrated packages and boards. These small and sophisticated systems require an evolution in both Surface Mount Technology (SMT) processes and SMT materials to meet the product needs and maintain high assembly yields. Moreover, the desire to lower assembly costs continues.

Low Temperature Soldering (LTS) provides a cost-effective solution that improves the yield impact induced by high temperature (HT) warpage of SMT components while reducing cost. HT warpage is widely recognized as one of the major challenges for SMT. By lowering the peak temperature during reflow, warpage is reduced, resulting in higher SMT yields. Energy consumption is also reduced resulting in measurable operational cost savings. Furthermore, LTS creates opportunities to optimize process flows, such as the elimination of wave soldering, based on these new conditions. To accomplish this requires the development of a whole new class of durable and reliable low temperature solder pastes and processes.

Successful transition to low temperature soldering requires fundamental understanding of the chemistry and mechanics of joint formation as well as the SMT manufacturing challenges to build confidence and consensus across the industry. Most of the low temperature alloys are based upon an addition of bismuth (Bi), with SnAgBi and SnAgCuBi alloys being the primary candidates. Bismuth, however introduces solderability, flux chemistry and most of all, mechanical reliability issues to the alloyed interconnect structure. Bi containing alloys are well known for their brittle properties and susceptibility to mechanical shock.

The above alloys, SnAgBi and SnAgCuBi, though melting below the 220ºC melting temperature of the SnAgCu (SAC) family of alloys in wide usage, still have melting points above 200ºC. The peak reflow temperatures of such alloys are still too high to realize fully the economic and technical benefits of lower temperature soldering. Alloys in the Bi-Sn system are better candidates due to the low 139ºC eutectic temperature of this system.

The interest in the use of alloys in this Bi-Sn system is not new. The 58Bi42Sn alloy was a strong candidate to replace eutectic Sn-Pb solder during the mandated Pb-free transition from Pb based alloys in the early 2000's, and extensive research was done to investigate its feasibility. Ferrer and Holder [1] alone lists 69 publications on this alloy system between 1991 and 2001. As noted at the time however, its low melting point limited its storage and operating temperatures and any under-the-hood automotive or aerospace applications [2]. More importantly, fear from residual Pb contamination was a primary deterrent to Sn-Bi adoption at that time. This arose from the real possibility of the formation of a ternary eutectic 51.5Bi33Pb15.5Sn due to residual Pb in the manufacturing environment. This BiPbSn eutectic has an extremely low melting temperature of 95ºC [5-6]. Ultimately, SnAg/SnAgCu alloy systems were chosen to replace Pb-Sn. [2-3].

The 2007 version of the iNEMI Roadmap [7] initially predicted the migration to lower temperature and lower cost lead-free solder materials in the 2011–2017 time frame. The current 2017 version of the iNEMI Roadmap, anticipates a rising trend in the % of low temperature solder used for board assembly, with a projection of 10% in 2021. As an industry-led consortium, part of iNEMI's mission is to identify future technology trends, infrastructure gaps, and, together with its membership from supply chain to producers, accelerate innovation and technology deployment in the global electronics industry. Therefore, based on the roadmap gap analysis and member's interest, iNEMI established the *"BiSn Based Low Temperature Soldering Process and Reliability Project" (LTSPR)* in 2015.

The purpose of this project is to assess the surface mount processing and mechanical reliability of the solder joints formed when enhanced Bi-Sn based solder pastes are used for assembling electronic components on printed circuit boards. Currently, there are 22 member participants in this Project. These participants comprise of a diverse mix of Original Design Manufacturers (ODMs), Original Equipment Manufacturers (OEMs), Material Suppliers and Universities.

The LTSPR project is divided into three phases. Phase 1 is the material selection and process development phase. Phase 2 is the Mechanical Shock testing phase and Phase 3 is the temperature cycling and other related reliability tests phase. This paper reports out the initial results of Phase 1.

The solder paste materials selected for evaluation are first described followed by the test vehicles designed for their SMTA process capability evaluation. Results from the key SMT process steps, such as stencil printing, reflow, and rework are also described, including descriptions of observed solder joint defects. Surface Insulation Resistance (SIR) of the selected solder pastes are also reported due to lack of data for the electrochemical reliability of solder paste flux residues from the for new Bi-Sn pastes. Finally, future work planned in the subsequent phases of the LTSPR project is described.

SOLDER PASTE MATERIALS SELECTION

To overcome the poor mechanical shock [8] and lower fatigue resistance [9] of 58Bi42Sn eutectic alloys two pathways have been explored by solder paste manufacturers [10]. One is the improvement of the ductility of the BiSn solder alloy by optimizing the metallurgical compositions of the alloy [11] and the other is the use of polymeric reinforcement of the solder joint [12] by using solder pastes containing resin, which are termed Joint Reinforcement Pastes (JRP). Both these pathways have shown promise in enhancing the mechanical shock resistance of mixed SAC-BiSn BGA solder joints [11,13,14].

Various suppliers of the ductile Bi-Sn alloy solder pastes and resin incorporated JRP paste were approached with the aim for obtaining an appropriate paste from their development or product paste portfolio to evaluate in the LTSPR project. Each supplier that initially showed interest was requested to present appropriate data on their selected paste to the project team. The project team then selected the solder pastes based on the following criteria: (i) prior experience of project team members with the proposed solder pastes, (ii) the maturity of the solder paste based on its usage at various manufacturers

such as ODMs, (iii) the quality and quantity of reliability data, particularly for mechanical shock robustness, presented by the supplier and (iv) the willingness of the supplier to submit the desired quantity of solder paste to the project team for evaluation.

The project team also decided to select two `control` pastes for comparison with the ductile Bi-Sn alloy and the JRP resin pastes. One of the controls was the SAC305 composition. The paste selected was a leading paste from a supplier who was a member of the project team. The other control were three compositions of the BiSnAg system, containing 0%, 0.4%, and1.0% Ag. Addition of Ag has been shown to improve the mechanical properties of the Bi-Sn eutectic [15]. Again, three pastes in this control were selected from three different suppliers, two of whom were members of the project team. Eventually, 3 solder pastes, in four different categories, were selected for evaluation during the process development phase. The distribution of these pastes was as follows:

- 5 Ductile Bi-Sn Metallurgy pastes
- 4 Resin Reinforced Bi-Sn pastes
- 3 Bi-Sn baseline pastes (0%, 0.4%, 1%Ag)
- 1 SAC paste to serve as current technology baseline

These 13 solder pastes were assigned code numbers and code names to ensure that each paste supplier, most of whom were members of the project team, did not know the identity of each of the pastes being evaluated, except for the one submitted by them. The code names were derived by a Malaysian project team member, using the various species of Durian fruit available in Malaysia. Table 1 lists the Code number and name, the paste category, the board assembly site, and the liquidus temperatures for these 13 pastes.

Evaluations conducted in this study were carried out at three different manufacturing sites, two in the Far East and one in the US. These sites are identified as a number in Table 1 and subsequently in this document. The liquidus temperature of the solder pastes ranged from 139ºC for the eutectic compositions to 191ºC for a hypoeutectic composition with 15 wt% bismuth.

Table 1. Paste Code # & Name, Category, Board Assembly Site and Liquidus Temperatures for all pastes evaluated

Code		Paste Category	Board Assm Site	Liquidus Temp, ºC
#	Name			
D197	Raja Kunyit	SAC	1,2	219.6
D166	Balik Pulau	Bi-Sn Baseline	1	142.8
D165	Chee Chee		2	139.0
D160	Teka		3	139.0
D158	Kan You	Ductile Bi-Sn	3	174.0
D200	Black Thorn		2	191.4
D175	Red Prawn		1	142.2
D164	Red Flesh		2	179.0
D24	Sultan		2	151.1
D163	Horlor	JRP Resin Bi-Sn Based	1	139.0
D159	Golden Pillow		3	141.0
D145	Beserah		1	139.0
D123	Chanee		1	140.0

TEST VEHICLE DESIGN AND SETUP

Board Test Vehicle

The board test vehicle was named the Solder Paste Development Board (SPDB), and its layout is depicted in Figure 1. The various components designed on the SPDB are also indicated in Figure 1. The Bill of Materials (BOM) is listed in Table 2. The components chosen cover a wide variety of termination designs, including spheres soldered to organic substrates and socket paddles, gull wing leads, bottom terminations, through hole pins, and discretes.

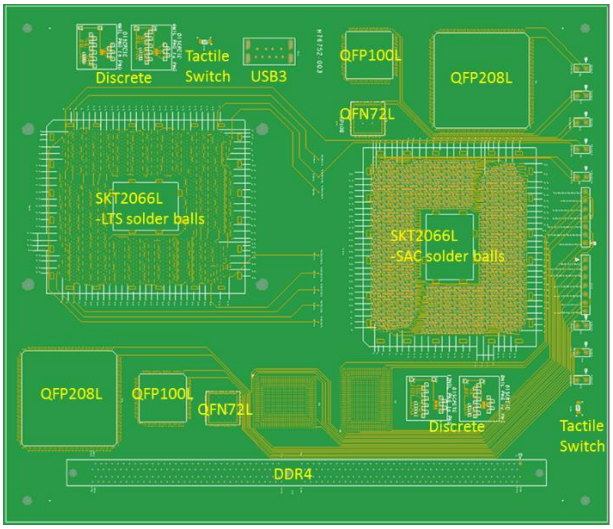

Figure 1. Layout of the Solder Paste Development Board (SPDB) Test Vehicle

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Table 2. Bill of Materials for the SPDB Test Vehicle

Designation	Description		Qnty	Daisy Chain
PCB	6"x7"x0.040", 8 layers, OSP surface finish		1	N/A
FC BGA	16x24mm, 0.4mm nominal pitch, SAC405 solder spheres		2	Yes
Socket R4	2066 pins, Bi-Sn-Ag solder spheres		1	No
Socket R4	2066 pins, SAC305 solder spheres		1	No
QFN	10x10mm, center ground pad, 72 terminations, 0.5mm pitch,		2	Yes
QFP100L	14x14mm, 0.5mm pitch		2	Yes
QFP208L	28x28mm, 0.5mm pitch		2	Yes
Chip Cap	0402	Pad design with 4/6/8/12 mils body to body spacing	20	Yes
Chip Cap	0201		20	Yes
Chip Cap	01005		20	Yes
Switch	Tactile switch with SMT and THM pins		2	No
DDR4	THM Connector		1	No
USB3	THM Connector		1	No

Test Vehicle Setup for Process Development

Due to the SPDB board being newly designed for the iNEMI LTSPR project, a series of design and process verification steps were carried out using the baseline SAC solder paste and one of the Bi-Sn Baseline solder pastes. This preliminary evaluation led to the following process definition and stencil design changes.

- SPDB would need a reflow pallet to prevent the board from sagging during reflow. This pallet design is shown in Figure 2.

- A unit of the fully populated SPDB with thermocouple attached at 10 locations was used for reflow profile development.
- For the 0402 size capacitors, the 4 mils package-to-package air gap design was violating DFM rules and resulted in bridging of adjacent packages. This particular defect would therefore not be recorded during the SPDB yield data collection. This design was intentionally incorporated to determine whether the Bi-Sn composition would lower this package-to-package distance limit for small chip components.
- To accommodate the pin-in-paste (P-i-P) process for Through Hole Mounted (THM) components, a 4 mils thick stencil was adopted.
- Stencil aperture design for the FCBGA was modified to accommodate a flatter peak reflow temperature warpage and the required volume of solder paste that needed to be printed on the PCB land to form a good quality solder joint, as the SAC solder balls of the BGA would not melt during the low temperature reflow process.
- The area ratio of the stencil aperture for the 01005 size chip capacitors was much lower than the current industry standard of 0.66. This was expected to result in insufficient solder paste being printed on the lands. But no insufficient solder joint defects were observed for these components during the setup stage of process development. Stencil aperture design for all discrete components are 1:1 vs. pad size and of a round shape.
- More solder paste volume was needed for Socket R4 leads due to the component warpage and the SAC solder spheres not collapsing during low temperature reflow.
- Center ground pads of QFN components was designed with 4 through hole vias to facilitate gas release. The stencil aperture was designed to minimize voids also.
- Rest of the THM components' stencil apertures were design to attain 100% hole fill, except for USB3's retention pins, which were only designed to attain ~60% hole fill.

EXPERIMENTAL RESULTS

Stencil Printing of Solder Pastes

Stencil printing of pastes, as well as subsequent reflow, inspection, test and rework assessments on the SPDB test vehicle was performed at three different factory sites, each of which used various pastes in the four different categories, as noted earlier. Each factory used one printer for all prints, but the printer make and model were different across all three manufacturing sites.

Laser etched stainless steel stencils were used as were stainless steel squeegees. Nano coating and other paste transfer enhancements were NOT used. This was intentional with an aim to get an assessment of the transfer efficiency of the solder pastes under identical baseline stencil material and design conditions. The stencil apertures were circular with fourteen different area ratios from 0.50 to 4.35. The volume of the stencil printed solder paste deposit was measured with SPI equipment, the make and model of such equipment being different at each manufacturing site.

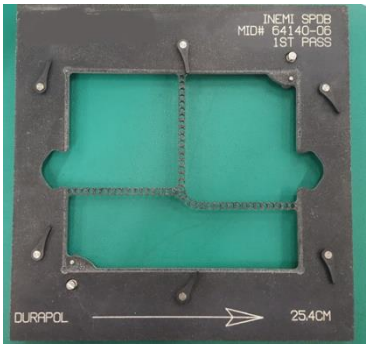

Figure 2. Design of the pallet used for the SPDB test vehicle during reflow soldering

The printer equipment related printing parameters were set as per the recommendations of the solder paste manufacturers. However, while the printing evaluation was being carried out, these parameters were tweaked at each site to optimize the transfer efficiency of the paste.

The paramount goal in this study was to determine the effect of the solder pastes in the various low temperature categories and compare with that of the SAC baseline paste. Hence, though Cpk is a more desired metric to determine how much nearer the data is to a desired target value, the more common industry metrics, transfer efficiency and coefficient of variation, were analyzed instead and compared for the four different categories of pastes.

Stencil area ratios greater than 0.66 have generally resulted in acceptable transfer efficiency across the -50% to 150% range from the target value. Area Ratios less than 0.60 have pushed the limits of the stencil printing process, and enhancements such as nano-coating and finer powder particle sizes have become necessary to meet printed solder paste requirements. Hence, solder paste transfer efficiencies for the various solder pastes were compared for the two land patterns below 0.66 area ratio on the SPDB. These two were the 01005 chip component and the FC BGA component land patterns, as listed in Table 3. Also listed in Table 3 is the next highest area ratio above the 0.66 industry limit, which was 0.75 for the 0201 chip capacitors. The stencil printing volume data for this was also analyzed for comparison with the other two.

Figure 3 plots the transfer efficiency (TE) of the four categories of pastes, Bi-Sn baseline, Ductile Bi-Sn, JRP resin and SAC baseline.

There is a downward trend in the TEs, as expected, when the area ratio decreases from 0.75 to 0.50. All boxes and whiskers are above the minimum 50% process control limit for the 0.75 area ratio. For the 0.59 area ratio, the whiskers for all three low temperature categories are below 50% limit. For the 0.50 area ratio, the entire box is below the minimum process

control limit for the JRP resin pastes, whereas for the other three categories, which includes the SAC baseline solder paste, the boxes partially fall below this line. This indicates that there is enhancement required for the solder paste printing process for all categories of solder pastes at the 0.50 area ratio, but the JRP resin pastes printability degrades much more than the other categories.

Figure 4 plots the coefficient of variation (COV) of the four categories of solder paste for the three area ratios at the low end.

Table 3. Component Land Patterns and their Stencil Aperture Area Ratios measured for Printing Process Evaluation

Component	Area Ratio
Chip 01005	0.50
FC BGA	0.59
Chip 0201	0.75
QFN 72 Edge pad	0.79
QFP 100	0.93

Component	Area Ratio
QFP 208	1.00
Chip 0402	1.25
Socket R4 Non-Oblong pad	1.53
Socket R4 Oblong pad	1.59

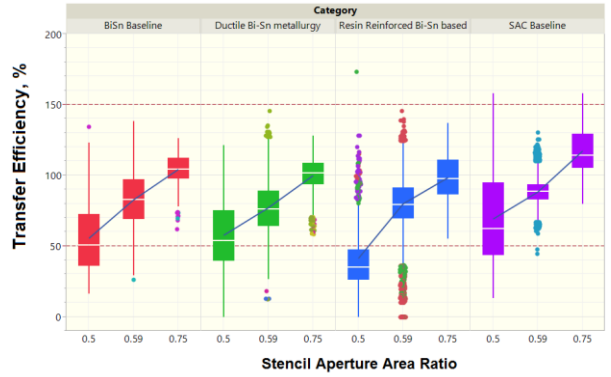

Figure 3. Transfer efficiency of four categories of solder pastes evaluated for three different stencil aperture area ratios at the low end

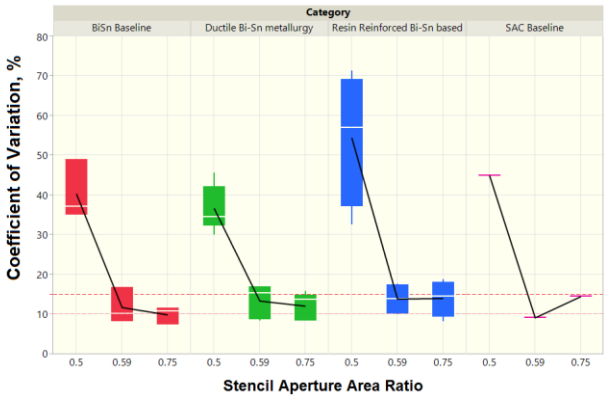

Figure 4. Coefficient of Variation of stencil printed solder paste volume for four categories of solder pastes evaluated for three different stencil aperture area ratios at the low end

As is the case with TE, the COV trends are in the opposite direction to that of TE, increasing with a decrease in area ration, but identical with respect to impact on the process quality since a larger coefficient of variation results in a larger process variability leading to solder joint yield and quality impairment. The JRP resin solder paste category is again the worst for the lowest area ratio (0.5) evaluated.

In summary, the stencil printability of solder pastes in the ductile Bi-Sn, and Bi-Sn baseline categories is equivalent to that of the baseline SAC solder paste evaluated in this study for all ranges of aspect ratios on the test vehicle. As expected, the printability degraded with decrease in area ration below 0.66 and this degradation was significantly worse for pastes in the JRP resin category.

Reflow Profile Development

Reflow profiles are critical to forming reliable solder joints during the reflow soldering process. The first thing to consider for a reflow profile is the melting point of the solder paste alloy. Slightly different elemental compositions can cause the melting behavior to differ. For instance, alloys can have a single melting point if they are eutectic or they will have a pasty range if they have an off-eutectic composition. In this study, the control paste is SAC305, which melts around 220ºC; this differs from the Bi-Sn eutectic alloy which melts at 139ºC and from most of the ductile Bi-Sn composition pastes, which are hypoeutectic.

The flux system is also different in pastes of different metallurgical powder compositions. This difference can be reflected in the soak zone time and temperature parameters. The resin in the JRP pastes notably affects the reflow profile topography.

Typical profiles for all four categories of solder pastes are depicted together in Figure 5 to elucidate pivotal differences.

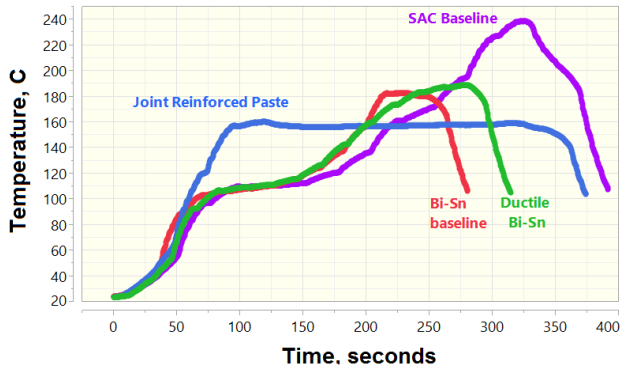

Figure 5. Typical reflow soldering profiles for SAC baseline, Bi-Sn baseline, Ductile Bi-Sn and Joint reinforced (resin) pastes.

The trapezoidal reflow profile for the JRP resin pastes and the shorter reflow process time for the Bi-Sn based (non-resin) pastes when compared with the SAC baseline paste, are facets that are easily obvious in this figure. Other differences

in key parameters required statistical analysis for comparison using data from the reflow profiles of all pastes evaluated.

Table 5 lists the results of the comparison of the six key reflow profile parameters between each of the four paste categories investigated.

Table 5. Results of Comparison of Reflow Profile Properties between each of the Four Paste Categories Investigated

Reflow Soldering Profile Zone	Reflow Profile Property	Comparison Between Paste Categories
Initial Ramp	Ramp Rate	SAC is significantly lower
Soak	Temperature	SAC significant higher
	Time	No significant difference
Reflow	Peak Reflow Temperature	SAC is significant higher JRP resin is significant lower
	Time above Liquidus	JRP Resin is significant higher Bi-Sn baseline is significant lower
Cool Down	Cooling Rate	No significant difference

The initial ramp for the Bi-Sn based solder pastes is faster than for the SAC baseline paste. This initial ramp is most critical for the JRP resin pastes because the paste needs to reach its melting point and wet the termination and land surfaces before the resin within starts to gel.

The Soak zone temperature is significantly higher for the SAC baseline than the Bi-Sn pastes, due to the flux chemistry being different for SAC solders and Bi-Sn solders.

The peak reflow temperature is obviously higher for the higher melting SAC solder paste. Time above liquidus is significantly longer for the JRP resin pastes since time is required for the resin to cure sufficiently for sufficient adhesion to the solder joint and solder mask on the board as well as cohesive strength. For the eutectic Bi-Sn solder pastes, the time above liquidus is the lowest of all categories since the liquidus temperatures are the lowest and wetting kinetics are the fastest due to the lack of a pasty range.

Each material supplier provided a reflow profile recommendation for the solder pastes in this study. Reflow profiles were developed at the three manufacturing sites with oven settings that tried to follow these recommendations closely. In some cases actual values of the key reflow profile parameters was different to some extent than those recommended. Table 6 below lists the instances where this was the case. Ten thermocouples were place on the reflow board during this reflow profile development step, nine on solder joints of different components and one on the PCB surface.

Table 6. Comparison between Actual Measured vs Supplier recommended of Key Reflow Profile Parameters

Paste Code Name / Number	Paste Category	Reflow Profile Parameter	Where Measured Value was in relation to Recommended Value
Black Thorn / D200	Ductile Bi-Sn	Initial Ramp Rate	Higher
		Peak Reflow Temperature	Higher
		Time Above Liquidus	Lower
Chanee / D123	JRP (resin)	Peak Reflow Temperature	Higher
Golden Pillow / D159	JRP (resin)	Soak Time	Higher
Horlor / D163	JRP (resin)	Peak Reflow Temperature	Lower
Raja Kunyit / D197	SAC	Initial Ramp Rate	Higher
Sultan / D24	Ductile Bi-Sn	Initial Ramp Rate	Lower
		Time Above Liquidus	Lower
		Cooling Rate	Lower
Teka / D160	Bi-Sn baseline	Time Above Liquidus	Higher

Manufacturing Yield

The manufacturability comparison between low temperature Bi-Sn category solder pastes (Bi-Sn baseline, Ductile Bi-Sn and JRP Resin) and the baseline SAC paste was assessed via component level manufacturing yield. The manufacturing yield does not include solder joint voids due to insufficient understanding of voids being generated for JRP resin containing solder pastes, avoiding misleading judgement. To avoid overlapping, the manufacturing yield of each of solder paste legs were verified and summarized from the defect record of post reflow inspection, electrical test, X-Ray and cross section inspections, excluding known DFM violations and manufacturability issues of the SPDB test vehicle, as mentioned earlier. These as listed below:

1. DFM violation:
   - 0402 chip capacitors' 4 mils package-to-package spacing generated a higher failure rate due to bridging / skew.
   - USB3 ground pins were designed for wave soldering, not for P-i-P reflow soldering, causing a hole fill calculated as ~68% maximum.
   - 01005 chip capacitors' insufficient solder due to the area ratio being R <0.66 with a 4 mils thick stencil.
2. Know manufacturing issues:

- Rough handling during shipment caused damage to SKT R4 with SAC spheres, and caused bent leads on DDR4 and QFP components.
- Soldering Socket R4 with BiSnAg solder spheres using SAC305 solder paste would result with larger voids, per the mechanism illustrated in Figure 6. The generation of such large voids when using a solder paste metallurgy that melts at a higher temperature than the solder sphere of a BGA or socket, has been seen before for forward compatible SnPb-SAC solder joints [16,17]. Examples of Socket R4 solder joints with large voids are shown in Figure 7.

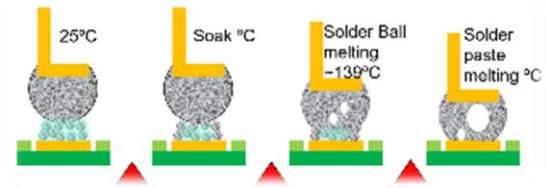

Figure 6. Proposed Mechanisms by which large voids form in Socket R4 with BiSnAg spheres when soldering with SAC305 paste.

The overall yield for each solder paste leg is listed in Table 7. Salient observations from the yield data follow.

- All THM solder joints formed by the pin-in-paste method when using JRP resin pastes were observed with voids and non-wetted regions. Cross-sections of these THM solder joints are shown in Figure 8.
- Except for, the FCBGA solder joints formed with all JRP resin pastes, except for D163 (Horlor) exhibited multiple issue, such like Head-on-Pillow (HoP) like and partial wetting. Cross-sections of these defects are seen in Figure 9.
- Boards assembled using D158 (Kan You), D160 (Teka), D165 (Chee Chee) and D200 (Black Thorn) pastes were observed with hot tearing failures, as seen in Figure 10. This hot tearing failure mechanism is discussed further in the next section.
- Only boards assembled with D166 (Balik Pulau), D24 (Sultan) and D164 (red Flesh) were observed without any manufacturing yield loss.

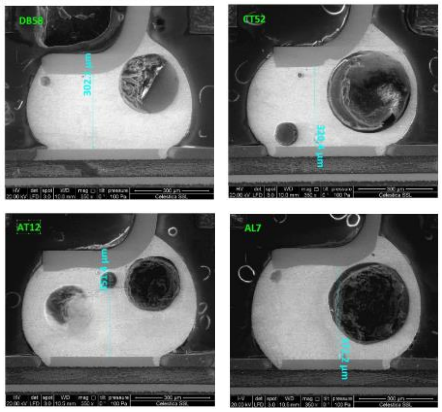

Figure 7. Cross-sections of four solder joints formed when Socket R4's BiSnAg solder balls were soldered with SAC305 solder paste. Large voids are clearly visible

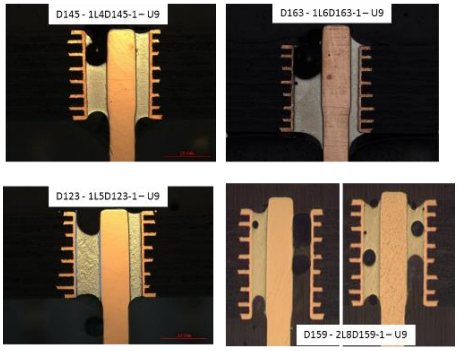

Figure 8. THM solder joints formed when using JRF Resin solder pastes. Voiding is clearly visible

Table 7. Manufacturing Yield with Board Quantity for all 13 Solder Pastes Evaluated

Solder Paste			Board Qty	Component Level Yield			Remark
Code	Name	Category		SMT	THM (P-i-P)	Overall	
D197	Raja Kunyit	SAC Baseline	10	99.85%	100.00%	99.85%	01005 insufficient solder
D160	Teka	Bi-Sn Baseline	5	99.70%	100.00%	99.70%	X-section shows BGA solder joints tearing
D165	Cheh Chee		5	99.70%	100.00%	99.70%	X-section shows BGA solder joints tearing
D166	Balik Pulau		5	100.00%	100.00%	100.00%	
D24	Sultan	Ductile Bi-Sn Metallurgy	3	100.00%	100.00%	100.00%	
D158	Kan You		5	99.70%	100.00%	99.70%	X-section shows BGA solder joints tearing
D164	Red Flesh		5	100.00%	100.00%	100.00%	
D175	Red Prawn		5	99.40%	100.00%	99.40%	01005 & BGA insufficient solder
D200	Black Thorn		5	99.70%	100.00%	99.70%	Taking out BGA Voids >25%, all 5x2
D123	Chanee	JRP Resin	5	97.61%	90.00%	87.85%	multiple issue, HnP liked' BGA SJ, voids at THM
D159	Golden Pillow		5	99.70%	95.00%	94.72%	multiple void at DDR4 THM pins (minor) &
D145	Beserah		5	94.63%	95.00%	89.90%	multiple issue, 0402-PtP 6mils skewed, partial wetting & HnP liked' BGA SJ, voids at THM
D163	HorLor		5	99.40%	95.00%	94.43%	0402-Body to Body 6mils skewed

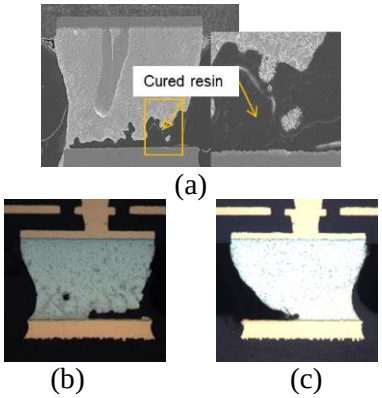

Figure 9. Partial Wetting defects for FC BGA solder joints formed with JRP resin pastes: (a) D145 (b) D123, (c) D159

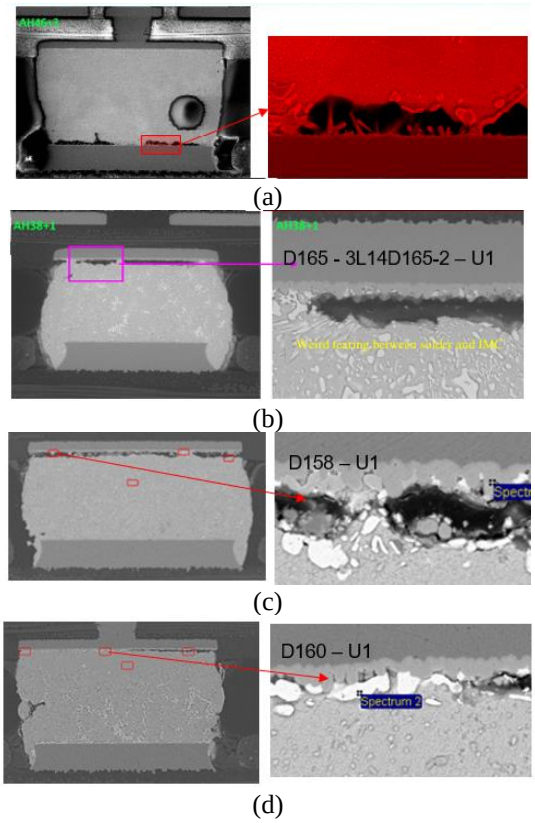

Figure 10. Hot Tearing Defects observed for the FCBGA solder joints when formed by various solder pastes: (a) D200 (Ductile BiSn), (b) D165 (Bi-Sn Baseline), (c) D158 (Ductile Bi-Sn), (d) D160 (Bi-Sn Baseline)

Hot Tearing of Mixed SAC-BiSn solder joints

Hot tearing is not commonly seen in BGA SAC solder joints of BGA components because most BGA components' warpage inversion temperature is much below the solidification temperatures for SAC alloys. In this study, as shown in Figure 10, hot tearing was observed in FCBGA solder joints assembled with four solder Bi-Sn pastes. The common features of these hot tearing defects were:

- The tearing occurred in solder joints under the die shadow; this is the region with largest CTE mismatch between the silicon die and the BGA substrate and hence is the most affected during the package inversion in shape when cooling down.
- The tearing occurred between the solder and the IMC. In three cases, it occurred at the BGA substrate land-to-solder interface and in one case it occurred at the PCB land-to-solder interface.
- For the BGA substrate to land interfaces, there is clear evidence of bismuth stratification between the IMC and the solder. This is seen in Figure 11. Bismuth stratification has been observed in some studies on bismuth containing solder joints [18,19].

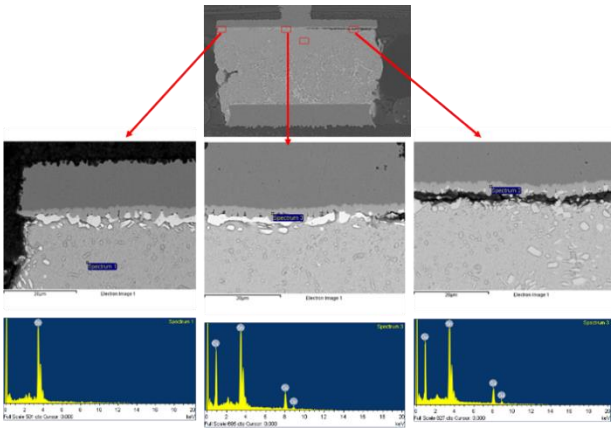

Figure 11. Evidence of Bismuth stratification at the BGA substrate to solder interface for a Bi-Sn solder paste

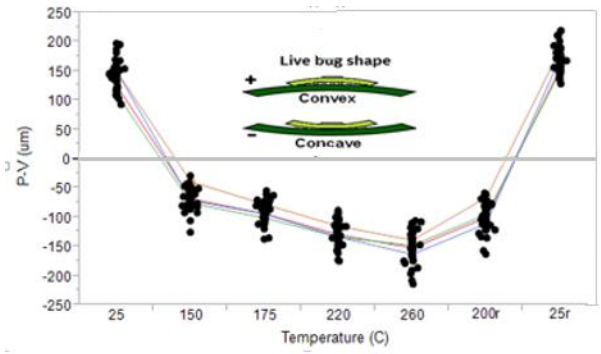

Figure 12. Warpage vs. temperature plot from Shadow Moiré measurements of the FCBGA component. The inversion temperature is in the 120-140ºC range.

Dynamic warpage characteristics of the FCBGA across the temperature range prevalent during the reflow soldering process is shown in Figure 12. As seen in this figure, the FCBGA has an inversion temperature around 120-140ºC. In this range, the warpage inverts from concave to convex.

One hypothesis of the mechanism for hot tearing in FCBGA solder joints is shown in Figure 13 and occurs in the following sequence:

1. During reflow, when the reflow temperature is over the melting point of the solder paste, Bi diffuses into the Tin solder.

a. Some solder paste formulations would cause Bi to diffuse to the interface of the BGA substrate's IMC, forming a continuous Bi layer. This would cause the melting point at that region to be ~138ºC.
b. In one case, that for D200 (Black Thorn), hot tearing occurred even without bismuth stratification. The solder paste metallurgy composition was significantly lower (~15%) than the other Bi-Sn based solder pastes. This case is similar to that observed by Boettinger et. al. [20] for Bi-Sn THM solder joints at low levels of bismuth content (<10%). Boettinger also observed Cu_6Sn_5 IMC needles attached to the THM pads. Figure 10(a) indicated that such needles are seen for the D200 solder joints, too.

2. When the reflow temperature starts to ramp down:
   a. Outer or peripheral joints of the BGA will start to solidify, but inner joints under the BGA, in the die shadow will still be in a molten state.
   b. These solidified joints will act as the planar reference height for the BGA.
   c. At this point, the BGA shape would most likely be concave (smiling face) or flat.
3. When the temperature continues to ramp down, reaching the inversion temperature:
   a. inner solder joints will start solidifying.
   b. the BGA substrate's shape will start to invert to the convex shape (sad face) and generate tensile and peeling stresses to the solder joints, tending to increase the distance between the BGA and the PCB, in the die shadow area
4. When the temperature cools down further, those `cracks` in the joints will continue to propagate, to release the stress caused by the warpage generated by CTE mismatch.

Hot tearing can be overcome by:

a. Ensuring that there is no overlap of the FCBGA's warpage inversion temperature range and the solder's solidification temperature range. Cooling rate during reflow is one factor that can be tuned to ensure this.
b. For solder pastes with high bismuth compositions (>30wt%) limiting the bismuth mixing levels in the SAC solder balls by adjusting the solder paste printed volume on the BGA lands. This will preclude the bismuth solder pastes from wetting up to the top of the solder joint near the component substrate during reflow and forming a bismuth stratified layer at the IMC to solder interface. The three solder pastes that exhibited hot tearing at the package interface had the highest bismuth mixing levels within the SAC solder spheres.
c. For solder pastes with low bismuth compositions, such as the D200 (Black Thorn), increasing the Bismuth concentration at the PCB land area by increasing the solder paste volume printed on the lands in the die shadow.

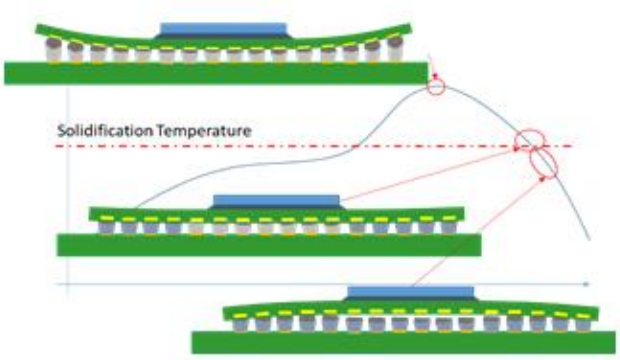

Figure 13. Illustration of how Hot Tearing happens in FCBGA solder joint during the reflow soldering process

Component Rework Assessment

An experiment was done to determine the difficulty and duration of the *some* attributes of a Rework process for specific components soldered using low temperature Bi-Sn based solder pastes, and comparing this with the same components soldered using SAC solder paste. The process steps evaluated were (i) removal of the component using the standard process to melt the solder joints, which entailed hot air, and (ii) site dressing of the land pattern area on the PCB once the component was removed, again using the standard soldering iron and wick method.

Two types of components were reworked – FCBGA and QFN. One of the two FCBGAs and both QFNs on a board. Two boards were reworked per leg, which amounts to 26 total boards, since there were 13 solder pastes evaluated. This rework assessment was done at each of the three manufacturing sites where the various legs with the different solder pastes, were assembled.

This rework was carried out by operators on the manufacturing line familiar and experienced in reworking components on boards.

To quantify the difficulty in reworking the components, guidelines were set on how a score could be assigned to each attribute of the rework process. Table 8 lists these scoring guidelines. This table was adapted from a similar one developed by Rajarathinam et. al. [21] for rework of components having board level underfills. The quantitative scores in the table, indicate the difficulty of each attribute of the rework process. A score of 10 is the best and the highest attainable and indicates the process was easily done. Scores from 5-9 indicate that there was moderate difficulty in successfully carrying out the attribute of the rework process. Scores 4 and below indicate that the attribute step was very difficult and incurred some damage to the board features.

Results of the scoring are depicted in Figure 14. To simplify this depiction and analysis of the scores, they are shown for each of 4 solder paste type categories, and separated out for

each attribute of the rework process, rather than for shown separately for each of the 13 solder pastes evaluated.

For each attribute of the Rework Process, the following observations were noted by the rework operators and confirmed by the scores, as shown in Figure 14.

Part Removal: Higher melting temperatures make the SAC baseline solder joints more difficult to remove in comparison with the solder joints formed by the lower melting Bi-Sn solder pastes. Low voiding of the SAC paste and good wetting on the QFN thermal plane make part removal difficult. The presence of cured resin when using JRP pastes also makes the part removal more difficult.

Amount of Material Remaining: Presence of cured resin when using JRP resin pastes tends to leave more material on the board after part removal. More SAC solder is left on the lands probably due to its higher surface tension than Bi-Sn solder.

Number of Pads Damaged: For the JRP resin legs, pad damage was minimal. The cured resin protects pads during the part removal and site redress.

Number of Traces Damaged: No damage to traces when site dressing lands soldered with for low temperature solders.

Time for Flux or Resin Residue Removal: The presence of cured resin results in a longer time for residue removal.

Time for Solder Wicking: The presence of cured resin requires a longer time for solder wicking.

Solder Mask Damage: Solder mask damage was significantly less for components soldered with lower temperature solder pastes.

Ergo Behavior: All category pastes scored well in ergo behavior; The SAC baseline leg boards needed minimum force.

In summary, *the lower melting temperature of the solder joints formed with Bi-Sn solder pastes facilitates easier part removal and site redress*. Incidences of solder mask and trace damage when reworking solder joints formed with low temperature solder pastes are reduced when compared to the higher melting SAC solder joints. The presence of cured resin for solder joints formed when using resin-reinforced low-temperature JRP solder pastes results in a longer site redress process.

Table 8. Scoring Guidelines for Each of the Attributes during the Rework Process for BGA and QFN Components

Attribute		Score				
		1	3	5	7	10
B	Part removal	Suction + High force, cannot be removed	Suction + High force, to pry and removed	Suction + Medium force to pry and remove	Suction + low force to pry and remove	Removes on tool suction alone
C	Amount of material left	>75%	50%-75%	25-50%	10-25%	0-10%
D	No. of pads damaged	>9	6～9	3～6	1～2	0
E	No. of traces damaged	>9	6～9	3～6	1～2	0
G	Time for flux /resin removal	>10mins	≦10mins	≦8mins	≦5mins	≦3mins
H	Time for solder wicking	>10mins	≦10mins	≦8mins	≦5mins	≦3mins
I	Solder mask damage	Significant damage (>15% area of site)	Damage to 10～15% area	Damage to 5～10% area	Damage to <5% area	No damage
J	Ergo Behavior	Not Possible	High Force	Medium Force	Low Force	Minimal Force

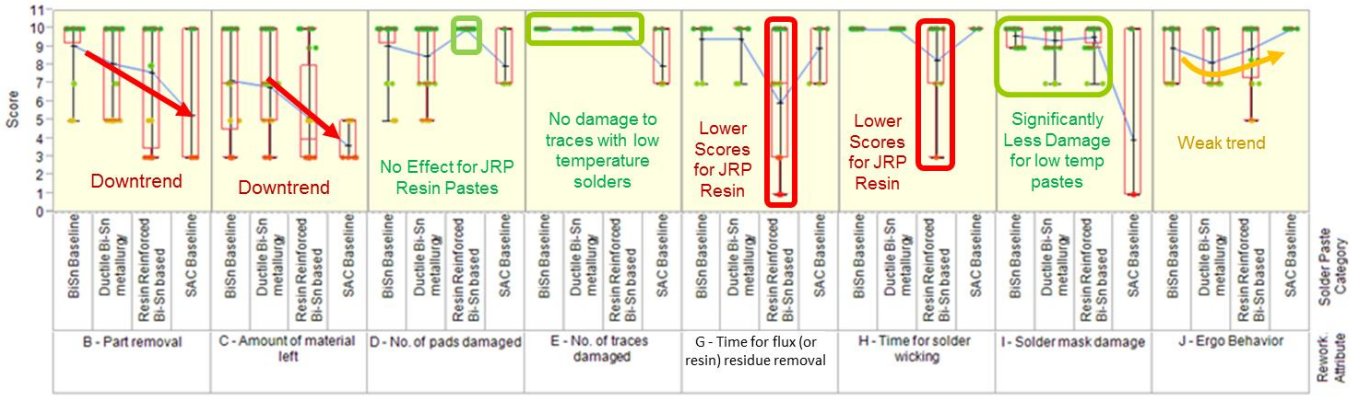

Figure 14. Rework Assessment Scores for each category of solder paste distinguished for each Rework Process Attribute. Denotation on trends and other effects are listed for each Attribute.

SIR Measurement

SIR measurements were performed according to IPC-650 Method 2.6.3.7 [22]. IPC-B-24 comb pattern coupons, with 4 nets per coupon, was the test vehicle. Except for one of the 13 solder pastes, 3 coupons were prepared for each solder paste, by the paste supplier. Control coupons, with no flux or solder paste applied, were also tested from each supplier. The SIR test was run and measurement collected at an independent testing house.

Figure 15 depicts the results of the SIR test for all solder pastes tested. The data from the control coupons for each solder paste is also show for comparison. Since the SIR measurements were run for 168 hours at half hour intervals there are 45,000 data points for each solder paste.

As is apparent, *all solder pastes passed the minimum requirement for the SIR measurement*, since all data points are above the $1x10^8$ ohm limit for SIR. This indicates the flux chemistries used for the Bi-Sn solder pastes, including the resin containing JRP category pastes, are reliable with regards to electro migration risk.

For most of the solder pastes, the paste data and the control data are statistically equivalent, i.e., their box plots and whiskers overlap considerably. However, for two solder pastes in the baseline BiSn category, Teka (D160) and Balik Pulau (D166), and one solder paste in the JRP category, Chanee (D145), the solder paste coupon data is significantly lower than the control coupon data.

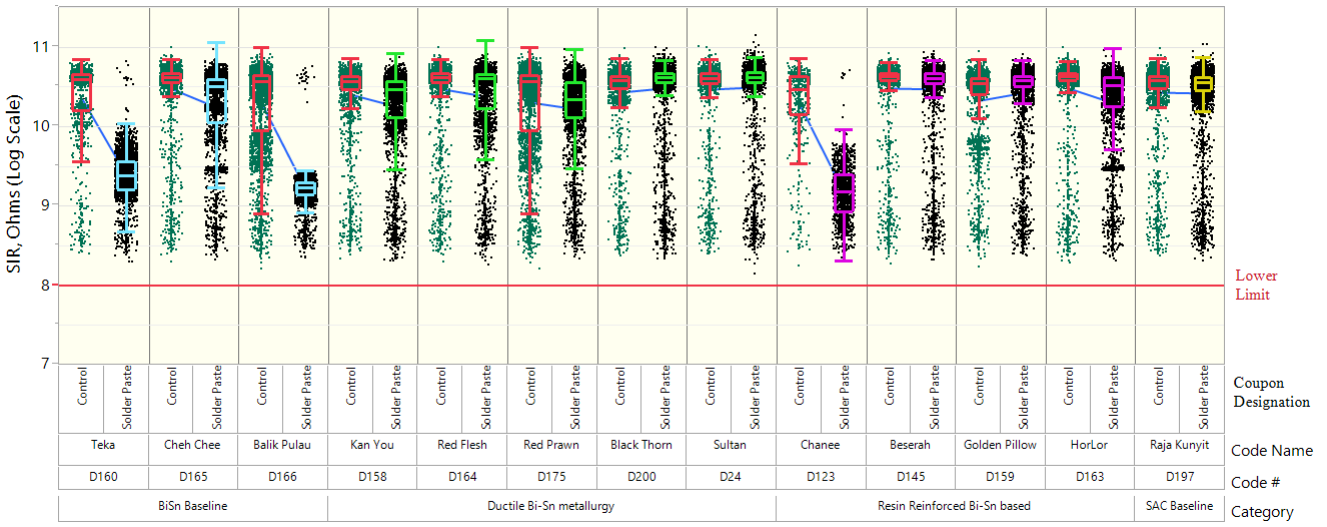

Figure 15: SIR data for all 13 solder pastes evaluated. Data from Control Coupons which had no solder paste applied are also shown for comparison.

CONCLUSIONS

The conclusions from the evaluations of the four different categories of solder pastes for each of the various steps in surface mount soldering are given below.

- Printability: With one exception, stencil printability of solder pastes in the ductile Bi-Sn, Bi-Sn baseline and the JRP resin categories is equivalent to that of the baseline SAC solder paste evaluated in this study for all ranges of aspect ratios on the test vehicle, even though, as expected, the printability degraded with decrease in area ration below 0.66. The one exception was at the lowest aspect ratio (0.50), for which the JRP resin category was significantly worse than the others.
- Reflow Soldering Profile: The ductile Bi-Sn and baseline Bi-Sn category solder pastes have reflow profiles similar to the ramp-soak-peak topography of the baseline SAC paste, but with a lower peak reflow temperature and lower time above liquidus. The JRP resin profiles are trapezoidal in topography with a lower peak reflow temperature and a longer time above liquidus to ensure the resin cures adequately. The initial ramp rate for the JRP resin pastes is more critical to avoid premature gelling of the resin in the reflow process.
- Solder Joint Defects: The following non-design related defects were observed during the process development phase of the iNEMI LTSPR project.
  - When using JRP resin pastes, THM pin-in-paste solder joints and FCBGA SAC sphere solder joints exhibited partial or no wetting. One possible mechanism of this defect is the premature gelling of the resin before the solder has become molten and has wet the THM pin and through hole wall, or the BGA SAC sphere.
  - Hot Tearing was observed in mixed SAC-BiSn FCBGA solder joints located the die shadow area when using four low temperature Bi-Sn solder pastes. This hot tearing phenomena is caused by an interaction of the bismuth stratification at the package substrate interface, the FCBGA dynamic warpage characteristic as it cools down and the cooling rate during reflow soldering. It can also be caused without bismuth stratification, if the solder paste metallurgy composition the solidification temperature to overlap the package substrate inversion temperature.

- FCBGA and QFN Component Removal: When compared to the higher melting SAC solder joints, the lower melting temperature of the solder joints formed with Bi-Sn solder pastes (i) facilitates easier part removal and site redress and (ii) reduces Incidences of solder mask and trace damage. When using resin-reinforced low-temperature JRP solder pastes, the presence of cured resin for solder joints formed results in a longer site redress process.
- SIR of Paste Fluxes: All evaluated solder pastes passed the minimum requirement for the SIR measurement

FUTURE WORK

This paper focused on the surface mount reflow process development aspects when using a number of low temperature Bi-Sn solder pastes. The area array component solder joints, which are of a mixed alloy composition since their SAC solder balls are soldered with Bi-Sn solder pastes, will be therefore characterized for the solder joint height, bismuth mixing levels, and Intermetallic Compound (IMC) thickness.

Further, to understand the solder joint reliability performance of solder joints formed when using these various low temperature pastes, a series of mechanical shock and temperature cycling testing has being planned by the iNEMI LTSPD project team.

Bismuth containing solder joints are prone to catastrophic failures during mechanical shock and drop events particularly for mixed SAC-BiSn solder joints [23]. Mechanical shock testing is planned on two BGA components – (1) 0.4mm ball pitch Package-on-Package (PoP) mounted on a JEDEC B111A shock test board designed for this package, and (2) 0.65mm ball pitch FCBGA component mounted on a standard form factor Shock Test Board (STB) [24]. These mechanical shock tests are currently in progress and will be reported in the near future.

Solder joints age and degrade during service and eventually fail by the common wear out mechanism of solder fatigue [25]. Thermally activated solder fatigue (creep fatigue) is the major wear-out failure mode and major source of failure for surface mount (SMT) components in electronic assemblies [26]. With the evolution of Pb-free solder manufacturing, high reliability end users have recognized the need to characterize and understand the long-term attachment performance of solder joints made with a variety of Sn-based Pb-free solders. Accelerated temperature cycling (ATC) is the preferred technique for evaluating the thermal fatigue performance of solder attachments [26]. The IPC-9701 document provides guidance for assessing reliability of surface mount attachments [27]. Despite significant efforts across the industry, thermal fatigue data is lacking for 3rd Generation, high reliability and low melting point Sn-based, Pb-free solders. Temperature cycling is therefore planned for a variety of components including FCBGAs, molded PBGAs, BTCs, ceramic LGAs and large ceramic chip components. The temperature cycle test vehicle board is currently in the design phase.

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