Resin Coated Copper Capacitive (RC3) Nanocomposites for System in a Package (SiP): Development of 3-8-3 structure

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Abstract

Embedded passives account for a very large part of today's electronic assemblies. This is particularly true for products such as cellular phones, camcorders, computers and several critical defense devices. Market pressures for new products with more features, smaller size and lower cost demand smaller, compact, simpler substrates. An obvious strategy is to reduce the number of surface mounted passives by embedding them in the substrate. In addition, current interconnect technology to accommodate surface mounted passives imposes certain limits on board design which constrain the overall system speed. Embedding passives is one way to minimize the functional footprint while at the same time improving performance. This paper discusses thin film technology based on resin coated copper capacitive (RC3) nanocomposites. In particular, we highlight recent developments on high capacitance, large area, thin film passives and their integration in System in a Package (SiP). A variety of RC3 nanocomposite thin films ranging from 8 microns to 50 microns thick were processed on Cu substrates by liquid coating. Multilayer embedded capacitors resulted in high capacitance 16-28 nF. The fabricated test vehicle also included two embedded resistor layers with resistance in the range of 15 ohms to 100 kohms. To enable high performance devices, an embedded resistor must meet certain tolerances. The embedded resistors can be laser trimmed to a tolerance of <5%, which is usually acceptable for most applications. We have an extended embedded passives solution that has been demonstrated both through its high wireability designs and package performance to be perfectly suited for the system in package (SiP) applications. As a case study, we have designed and fabricated eight layer high density internal passive core and subsequently applied fine geometry 3 buildup layers to form a 3-8-3 structure. The passive core technology is capable of providing up to 6 layers of embedded capacitance and could be extended further. This effort is an integrated approach centering on three interrelated fronts: (1) materials development and characterization; (2) fabrication, and (3) integration at the device level.

Introduction

The ability to shrink electronic systems with packaging size reduction without sacrificing function or performance is a major challenge in today's industry. One way to best achieve this objective is to eliminate active chip packages by directly attaching the bare die to the next level package and also by eliminating the surface area devoted to passives by embedding many of the capacitors and resistors within. The resulting size reduction of the package is seen in all measurable system attributes (diameter, thickness, weight). Embedded capacitors provide the greatest potential benefit for high density, high speed and low voltage IC packaging. Capacitors can be embedded into the interconnect substrate (printed wiring board, flex, MCM-L, interposer) to provide decoupling, bypass, termination, and frequency determining functions **[1]**. In order for embedded capacitors to be useful, the capacitive densities must be high enough to make layout areas reasonable. Available commercial polymer composite technology is not adequate for high capacitance density thin film embedded passives. Several polymer nanocomposite studies so far have been focused on processing of high capacitance density thin films within small substrates/wafers **[2-4]**. One of the important processing issues in thin film polymer nanocomposite based capacitors is to achieve high capacitance density on large coatings.

In the present study, we report novel ferroelectric-epoxy-based polymer nanocomposites that have the potential to surpass conventional composites to produce thin film capacitors over large surface areas, having high capacitance density and low loss. Specifically, novel crack resistant and easy to handle Resin Coated Copper Capacitive (RC3) nanocomposites capable of providing bulk decoupling capacitance for a conventional power-power core, or for a three layer Voltage-Ground-Voltage type power core, is described.

Epoxy dielectric resin has advantages for embedded passives in terms of processibility, thermal stability, low moisture absorption, high Tg, and versatility. However, processing and composition of nanocomposites is critical in order to achieve high quality, handleable, crack resistant RC3 nanocomposites. The RC3 nanocomposite based embedded capacitors offer many advantages over normal capacitor laminate:

1. RC3 reduces processing steps and substrate thickness
2. It can be used for sequential build up (SBU) technology.
3. Provides tailorable capacitance values from composition and thickness tuning
4. The capacitive composition can be provided in multiple carrier metal or organic films
5. RC3 films can be used as stand alone articles

Figure 1 shows a schematic representation of RC3 lamination. As illustrated in Figure 1, a RC3 capacitance

layer deposited on a substrate can reduce processing steps, as well as package thickness. In the present composite, $BaTiO_3$ or other high dielectric constant nano- or micro- particles increase the overall dielectric constant, whereas the polymer matrix provides better processability and mechanical robustness. The effects of particle size and thickness on the observed electrical performance of the embedded capacitors are presented. Uniform mixing of nanoparticles in the epoxy matrix results in highly stable thin film RC3 capacitors. The work was extended to the development of a RC3 based multilayer embedded capacitor construction for a flip-chip plastic ball grid array package with a 200µm core via pitch.

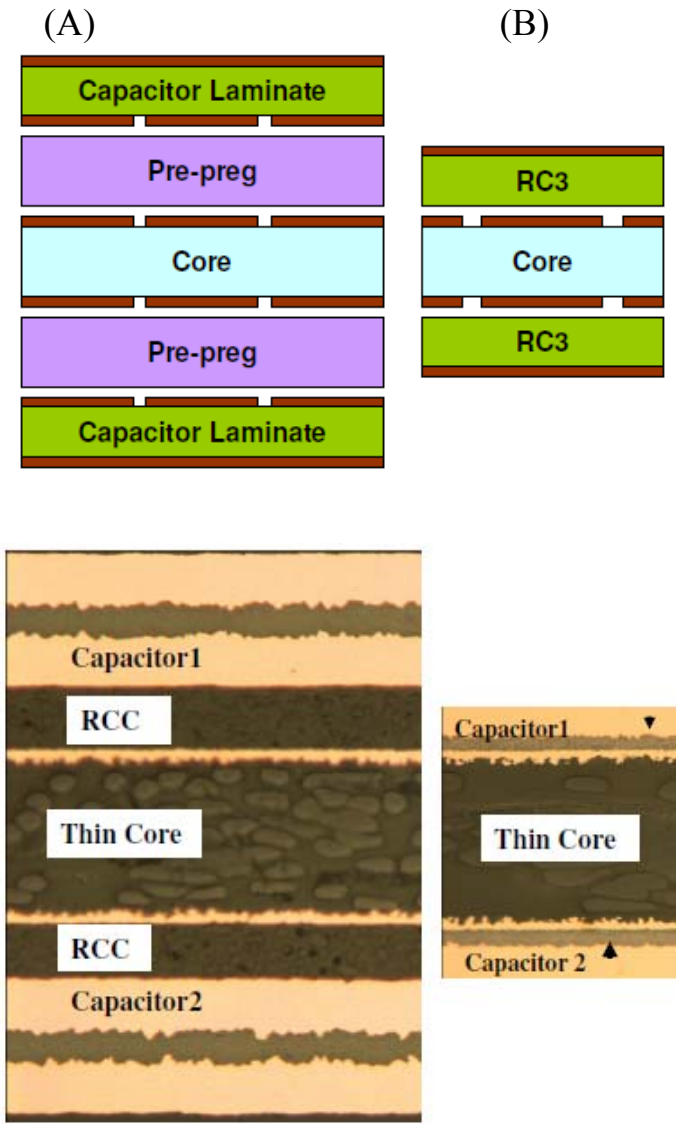

Figure 1: Advantages of Resin Coated Copper Capacitive (RC3) Materials (A) Substrate build with capacitor laminates, and (B) Substrate build with RC3 materials.

A variety of multilayer capacitors have been fabricated using the optimized RC3 nanocomposites. Specifically, RC3 nanocomposites were used to fabricate 35 mm substrates with a two by two array of 15mm square isolated epoxy based regions; each having six RC3 based embedded capacitance layers. The total TV core consists of eight metal layers. In addition, we have designed and fabricated another eight layer high density internal core and subsequently applied 3 buildup layers to form a 3-8-3 structure. A laser drillable, multilayer substrate capable of providing bulk decoupling capacitance and resistance is described. Here multiple capacitance layers with variable capacitance density and multiple resistance layers with variable resistivity will provide a wide range of capacitor and resistor values.

2. Experimental Procedure

A variety of $BaTiO_3$ and other nano- and micro- particles and their dispersion into epoxy resin were investigated in order to achieve a thin uniform film. In a typical procedure, $BaTiO_3$ epoxy nanocomposites were prepared by mixing appropriate amounts of the $BaTiO_3$ nano powders and epoxy resin in organic solvents. A thin film of this nanocomposite was then deposited on a copper substrate, and dried to produce free standing RC3 nanocomposite materials. Free standing RC3 can be directly laminated onto a substrate.

The optimized ferroelectric polymer nanocomposites were used to fabricate thin film multilayer (2,4,6 layers) embedded capacitors. Lamination was used to embed capacitors in multilayer printed circuit boards. The capacitor fabrication is based on a sequential build-up technology employing a first patternable electrode. RC3 nanocomposite can be laminated directly on top of pre-patterned PCB substrate. In the case of laminates, two thin films were prepared, dried and then laminated together at high temperature and pressure. To measure the electrical and dielectric properties of capacitor components, the laminates were patterned by conventional photolithography method. A capacitor core, sandwiched between layers of a dielectric material composed of filled epoxy resin, was used for the fabrication of an embedded capacitor. In a typical process, one side of layer capacitor ($Cu/BaTiO_3$-epoxy/Cu) electrode was selectively etched and then etched side of capacitor core was laminated with a layer of dielectric material. This was followed by etching second capacitor electrode and subsequent lamination with another dielectric. Top and bottom capacitor electrode connected through microvia to make the capacitor operational.

Electrical properties (capacitance, loss) of the nanocomposite thin films were measured at room temperature using an impedance /gain-phase analyzer (Model 4194A, HEWLETT-PACKARD). The dielectric constant/capacitance as a function of temperature was determined using a precision LCZ meter (Model 4277A, HEWLETT-PACKARD) at 1MHz. Surface morphology and particle distributions of nanocomposite films were characterized by a LEO 1550 SEM (scanning electron micrograph). Thicknesses of films were determined by Optical microscope and SEM.

3. Results and Discussion

The demand for high-performance, lightweight, portable computing power is driving the industry toward miniaturization at a rate not seen before. Electronic packaging is evolving to meet the demands of higher functionality in ever smaller packages. To accomplish this, new packaging needs to be able to integrate more dies with greater function, higher I/O counts, smaller pitches, and greater heat densities, while being pushed into smaller and smaller footprints. All these requirements are continuing to move chip packages towards system in a package (SiP) and thinner cross sections. **Figure 2** shows a typical SiP carrier 3-8-3 cross section. The SiP has four features that can significantly reduce the size of the final assembly. The first is to remove the active components from their package and assemble them directly to the SiP. The most efficient approach is to use Flip Chip Assembly (FCA). Many components have not been designed for FCA but if desired they can be converted to make FCA possible. The approaches to achieve this will be described. The second key item is to embed into the PWB as many of the passive components as possible. Resistors with values ranging from 15 ohms to 30,000 ohms can be efficiently embedded. Capacitors that are used for noise suppression (bypass / decoupling) and have values up to 0.1 microfarads (uf) can also be embedded. The SiPs described here will use a Passive Core that incorporates both the resistors and capacitors. The third key item is balancing the component area on both the top and bottom layers. With many passives eliminated and the active components in FCA format, components can be freely placed on top or bottom with little impact on the total height of the SiP assembly. The fourth item is efficiently using connector area. A fine pitch connector that is placed near the edge of the part minimizes the loss of functional area.

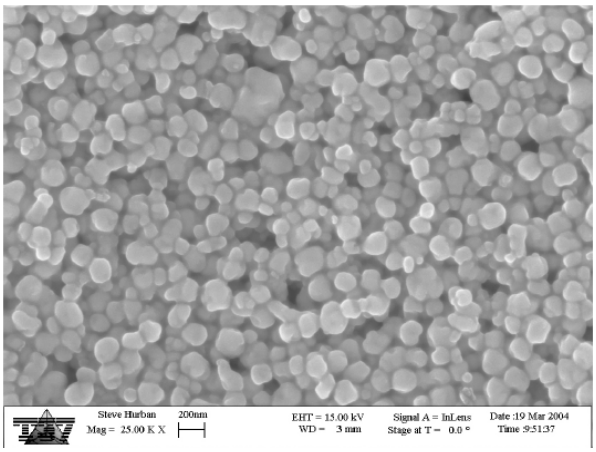

Figure 3: Larger area SEM images of RC3 nanocomposites.

A real challenge in the development of large–area, thin-film nanocomposites is the incompatibility that exists between the typically hydrophilic nanoparticles and hydrophobic polymer matrix, which leads to nanoparticle agglomeration. As a result, inferior coatings with poor performance are obtained. We have identified proper surface treatment that results in excellent dispersability of the nanoparticles and good quality, monolithic coatings. Appropriate surface treatment of ceramics depends on the specific processing routes. For example, Ramesh et al[**4**] reported silane treatment of hydro thermally prepared $BaTiO_3$ nanoparticles. The finer details of the particles and their surface morphologies were investigated using SEM. **Figure 3** shows scanning electron micrographs of RC3 nanocomposite thin film as a typical representative example. Nano particles formed uniform dispersion in the epoxy matrix. A variety of $BaTiO_3$ nanoparticles were used to prepare nanocomposites. For example, we have used hydrothermally processed 65 nm and 120 nm particles, as well as sol-gel processed 500 nm $BaTiO_3$ particles. Thin film (8-25 microns) capacitors fabricated from $BaTiO_3$ epoxy nanocomposites showed a stable capacitance density in the range of 7-25nF/Inch^2 that was stable over a frequency range of 1MHz to 10 MHz.

3.1 Test Vehicle with multilayer embedded capacitors and resistors:

RC3 nanocomposites were used to fabricate multilayer embedded capacitance in the core of a thin-core build-up package substrate **[5-6]**. This particular package technology lends itself well to single-chip and SiP applications, especially in situations where space constraints are critical and miniaturization is a requirement. The capability for embedded capacitance and the associated ability to reduce discrete component counts create significant additional miniaturization leverage.

This multi-layer structure starts with a core that is constructed using a 110 um thick dielectric layer composed of filled epoxy with aramid paper fibers sandwiched between Cu layers. The optimized ferroelectric polymer based RC3 nanocomposites were used to build up thin film multilayer (4,6,8 layers) cores with embedded capacitance. Capacitance values are defined by the feature size, thickness and dielectric constant of the polymer-ceramic compositions.

A test vehicle (TV) was designed with various sizes, thickness, and values of embedded capacitors. Individual 35 mm substrates with a two by two array of 15mm square isolated epoxy based regions were designed; each having six RC3 based embedded capacitance layers. The total TV core consists of eight metal layers. Design features, including antipad diameters, internal plane pickups for vias, and core via pitch were varied within each 15 mm square region. Probe pads were added for testing capability. The design incorporated four core via pitches (200 um, 300 um, 400 um,

500 um) and three possible plane pickups that include external plus one internal, external plus two internals, external plus three internals. Antipads of 162 um and 250 um were used. **Figure 4** shows the embedded capacitor layout.

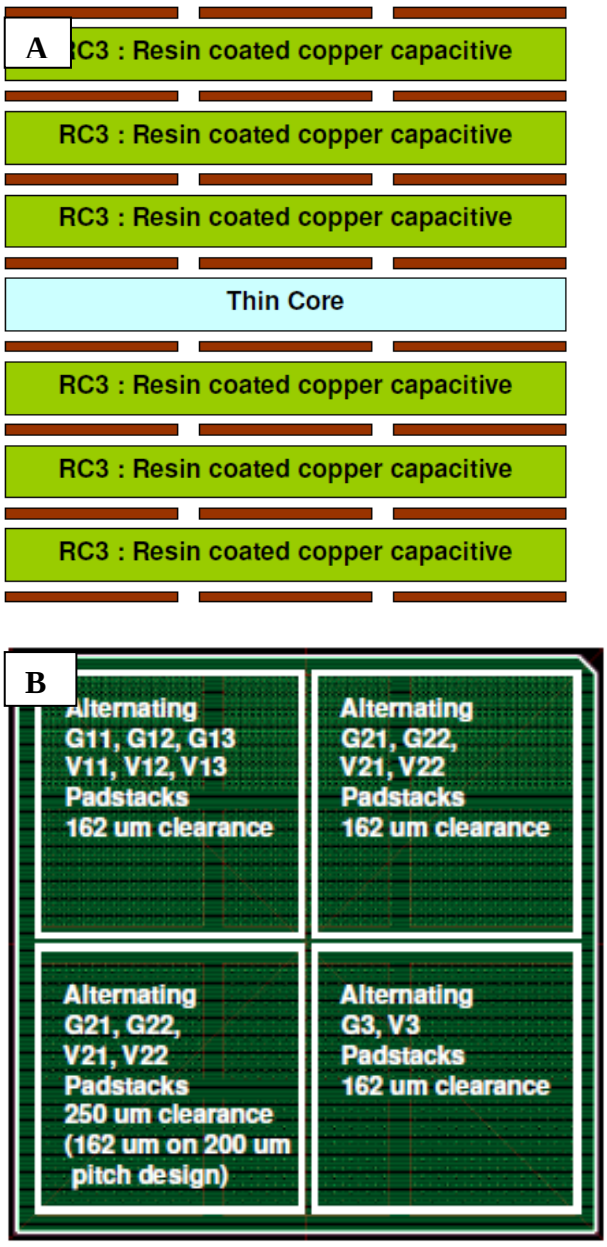

Figure 4: Layout of embedded capacitance test vehicle (A) Eight layer core stackup with six RC3 embedded capacitance layers, and (B) 35 mm body with 2X2 array of 15mm X 15 mm chips.

Figure 5 shows top and cross section views of multilayer embedded capacitors. It is possible to make a wide variety of capacitance layers with different thickness. Desired film thickness of the film can be achieved by controlling the viscosity of the coatings, composition, and the number of layers deposited. In the present process, we can easily laminate thin films from about 8 microns to about 50 microns.

Figure 5 shows a variety of multi-layer embedded capacitors where capacitors were sequentially applied on the surface.

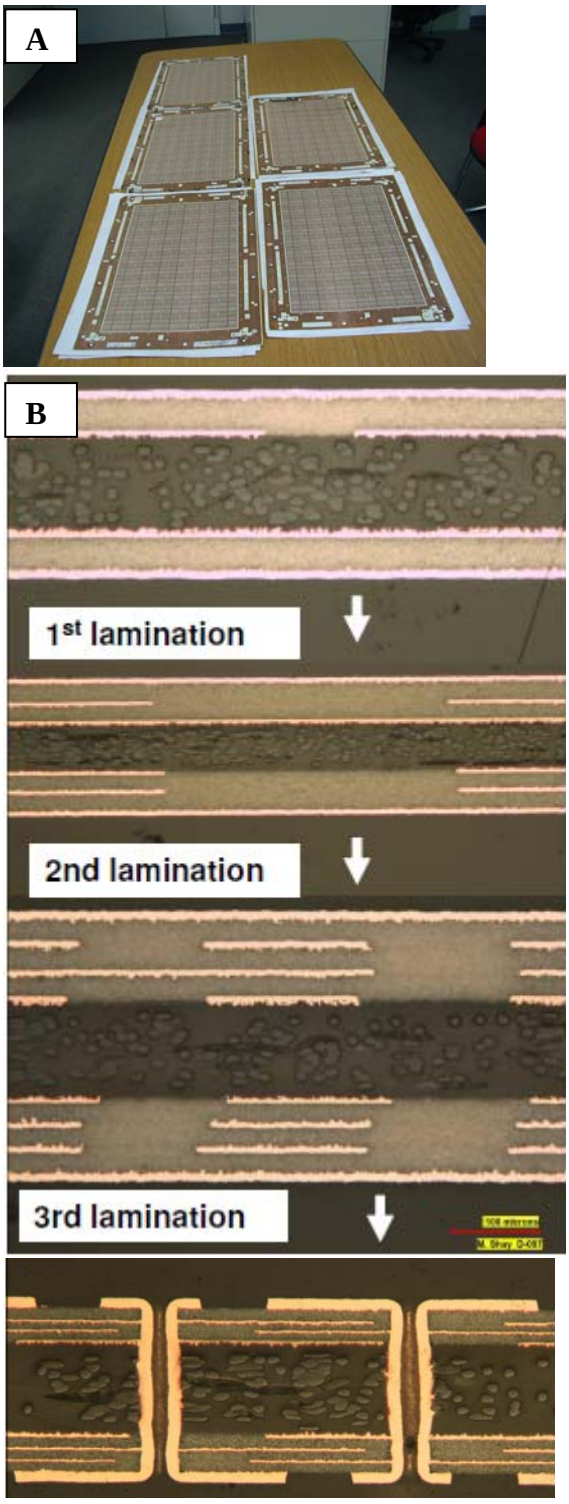

Figure 5 : **(A)** Photograph of RC3 nanocomposite based TVs (13.5 inch X 19 inch). **(B)** Photograph of multilayer (six) embedded capacitor formation shown in cross section.

The optimized RC3 nanocomposites were used to fabricate 35 mm substrates with a two by two array of 15mm

square isolated epoxy based regions; each having six RC3 based embedded capacitance layers. The total TV core consists of eight metal layers. Design features, including antipad diameters, internal plane pickups for vias, and core via pitch were varied within each 15 mm square region. High temperature/pressure lamination was used to embed 6 capacitance layers into the 8 layer internal core. The electrical properties of multilayer embedded capacitors fabricated from RC3 nanocomposite thin films showed high capacitance ranging from 16nF to 28 nF, depending on Cu area, composition and thickness of the capacitors. We have used Network Analyzer for high frequency measurements of printable embedded capacitors. The measurements were carried out from 45 MHz to 26GHz. **Figure 6** shows high frequency capacitance profile of 15 mm square capacitors. The curve fitting indicates that these capacitors are equivalent to 23 nF bulk capacitance. When the capacitor is embedded in the substrate, the impedance from the active device to the supporting capacitor can be much lower than with a discrete SMT capacitor. Embedded capacitance tends to be most effective at higher frequencies. At higher frequencies, the inductive parasitics associated with SMT devices and their termination become limiting. For this reason, large quantities of SMT decaps are often populated to reduce the effective inductance. This is counterproductive to system miniaturization. Due to the distributed nature of embedded capacitance, the inherent impedance and that associated with connection are significantly lower than SMT devices. Therefore, replacing SMT decaps with embedded capacitance at 40:1 or a greater capacitor value ratio improves high frequency performance and miniaturizes the part at the same time. **Figure 7** shows the simulated impact on power distribution impedance when discrete SMT capacitors are replaced with embedded capacitance. Impedance is reduced at frequencies greater than 1.5 GHz and high frequency resonances are dampened.

Upper Left Quad **~ 24 nF**	**Upper Right Quad** **~24 nF**
Lower Left Quad **22-28 nF**	**Lower Right Quad** **~16-19**

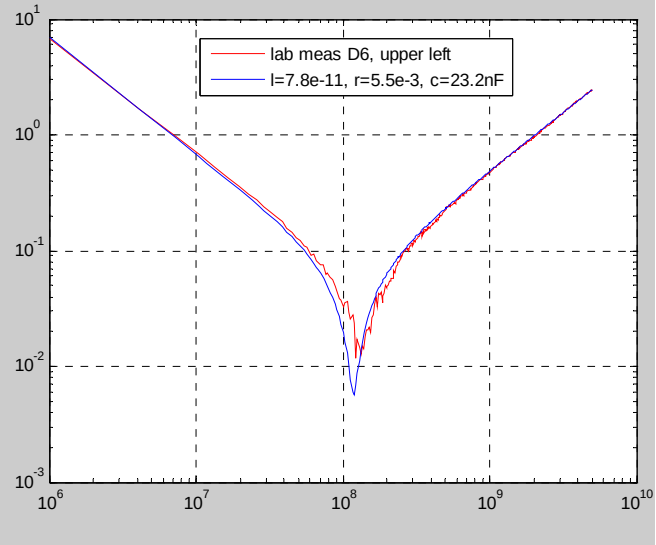

Figure 6: Capacitance and Impedance profile of Capacitors.

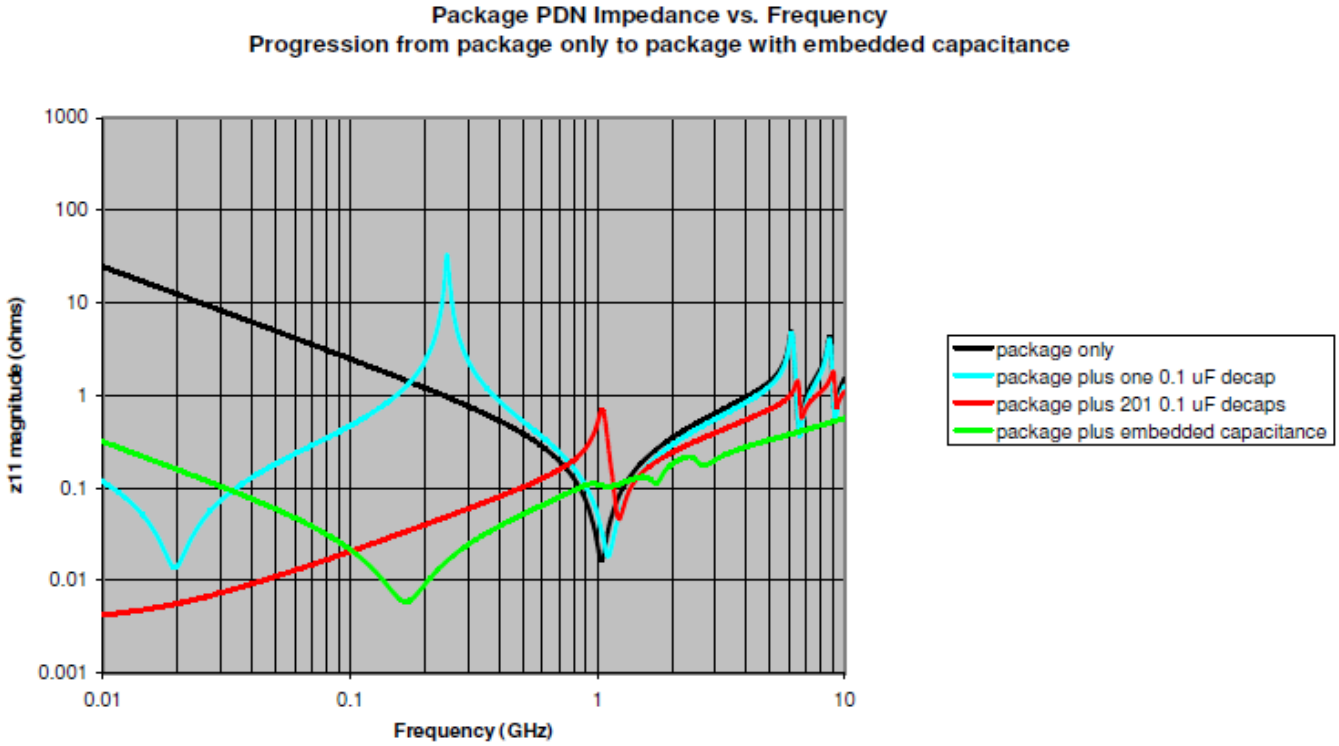

Figure 7 : Power Distribution Impedance Profile showing enhanced performance of embedded capacitance over SMT components.

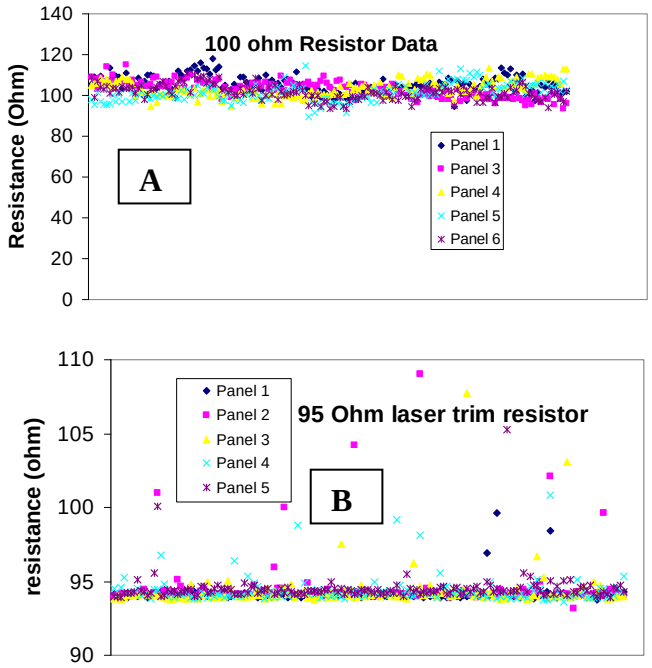

Figure 8 : Resistance profile (A) before laser trim, and (B) after laser trim (Target resistance for laser trimming was 95 ohms. Data above 98 ohms resistance are pre-scrapped, not trimmed).

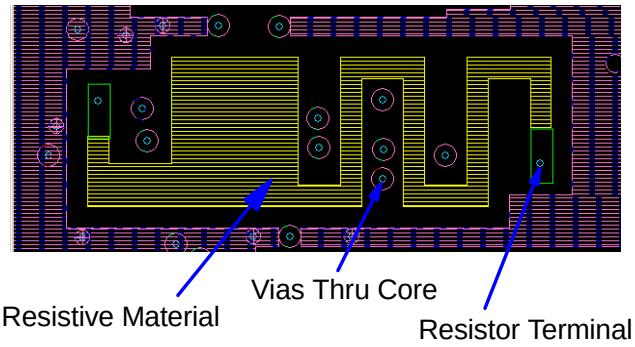

Figure 9: Embedded Serpentine 10,000 Ohm Resistor with Vias in Legs – 1.0 mm x 3.3 mm.

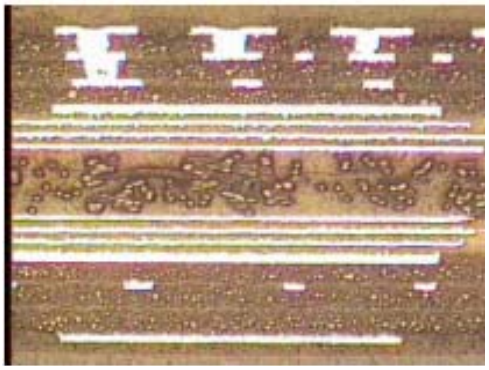

Figure 10: Photographs of 3-8-3 structure shown in cross section.

Additional layers of the test vehicle were populated with various sizes, geometries, and values of embedded resistors covering the range of 15 ohms to 100 kohms. Embedded resistor technology can use either thin film materials that are applied on the copper foil or screened resistor material that can be applied at any level. The approach chosen in these examples is thin film material and it is incorporated into the center layer of the core. The top of the core uses 25 ohm per square material and the bottom of the core uses 250 ohm per square material. This combination enables resistor ranges from 15 ohms through 30,000 ohms with efficient sizes for the embedded resistors. A total of 6 panels worth of foil resistors with 100 ohm target resistance were processed and tested. **Figure 8** summarizes the results. Resistance values within +/- 12% of nominal prior to trim were achieved. The embedded resistors can be laser trimmed to a tolerance of 5% for applications that require tighter tolerance. Power is also a consideration and the embedded resistor area needs to be matched to the power requirement. In these examples, dissipation of 100 mW could be achieved in a small resistor area. **Figure 9** shows a serpentine 10,000 ohm resistor using 250 ohm per square material. One of the features of the passive core is the use of CoreEZ's fine pitch 50 um via diameter on a pitch as small as 200 um. This allows vias to be placed within the legs of the serpentine resistors as shown in **Figure 9**. The ability to provide a high density of vias through the resistor network is critical for both signal wiring density and the effectiveness of the capacitor layers.

3.2 Test Vehicle with multilayer embedded capacitors and resistors: System in a package (3-8-3 structure):

As a case study, we have designed and fabricated an eight layer high density internal core and three subsequent fine geometry buildup layers to form a 3-8-3 structure (**Figure 10**). The eight layer internal core has two resistance layers in the middle and six capacitance layers sequentially applied on the surface. Two basic building blocks are used for this case study. One is an eight layer core. The silica-filled epoxy / aramid paper base substrate with two resistor layers, is sandwiched between six layers of a RC3 nanocomposites. The capacitor fabrication is based on a sequential build-up technology employing a first etched Cu electrode. After patterning of the electrode, the RC3 nanocomposite can be laminated within substrate. The second building block in this case study is the buildup layers used to generate signal layers. The signal (S) layers are comprised of copper features generated using a semi-additive (pattern plating) process. A line thickness of 12 µm was achieved with minimum dimensions for line width and space of 35-45 µm each. A structure with six signal layers, 6 capacitance layers and two resistance layers is shown schematically in **Figure 2**. This allows multiple capacitance layers in a thin total structure. The RC3 nanocomposite layer does not need to supply any structural support; it can be very thin and achieve high values of capacitance per unit area. Also, since it is not structural, the material choices expand significantly. The structure with small vias allows the vias to thread through the legs of the

serpentine resistors and significantly improves z-directional communication. This is especially important when there are multiple voltages that are supported by the capacitor layers. The overall approach lends itself to package miniaturization because capacitance can be increased through multiple layers and reduced thickness to give the desired values in a smaller area. These layers can be accessed because the laser drilled small holes (about 50 um diameter) do not consume large amounts of capacitive area. It has been estimated that this kind of SiP with embedded passives core can reduce package area to ~1 inch^2, which is about 26X area reduction of that of original PWB [7](**Figure 11**). Also, embedding passives within SiP can eliminate 70 0.01uF discrete caps and 150 discrete resistors.

4. Conclusions

A thin film technology was developed to fabricate embedded capacitance in the core of a thin-core build-up package. This technology incorporates a flake-free Resin Coated Copper Capacitive (RC3) nanocomposite based on a ferroelectric-epoxy polymer. An eight layer core with six embedded capacitance layers was constructed with three additional build-up layers to form a 3-8-3 structure. The combination of the thin-core package and multilayer embedded capacitance core technologies lends itself well to single-chip and system-in-package applications, especially in situations where space constraints are critical and miniaturization is a requirement. The capability of embedded capacitance and the associated ability to reduce discrete component counts create significant additional miniaturization leverage.

The structure has the resistors in the middle and the capacitors sequentially applied on the surface. This allows multiple capacitance layers with variable capacitance density and multiple resistance layers with variable resistivity in a thin total structure. The structures with small vias have an ability to communicate efficiently in the z-direction to handle the double sided demands.

Acknowledgments

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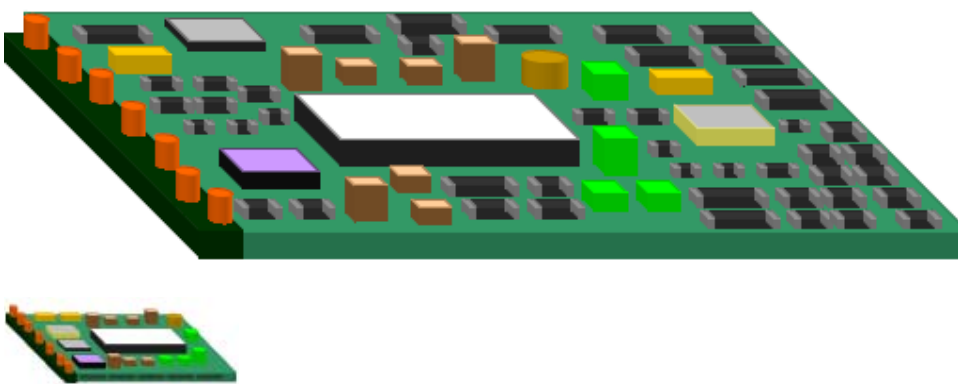

Figure 11: PWB vs SiP