Reliability and Failure Mechanisms of Laminate Substrates in a Pb-free World

Kevin Knadle
Endicott Interconnect Technologies, Inc.
Endicott, NY

Abstract
The plated thru hole has changed considerably in 50 years of electronic packaging, but in its many forms remains the most common interconnection in 1st and 2nd level electronic packaging, and is still one of the most feared in terms of reliability. The transition from the original solder filled holes to BGA wiring vias, subcomposite buried vias, and today's microvias has resulted in many new failure mechanisms, not only in the copper interconnections but also in the surrounding laminate, especially with Pb free reflows.

This presentation surveys the most significant via and via-related laminate failure mechanisms from past to present using data from current induced thermal cycling (CITC) testing, failure analysis, and other sources. The relative life and failure modes of thru vias, buried vias, and microvias (stacked vs. non-stacked) are compared, along with the affect of structure, materials, and peak temperatures on the above. The origin of via-induced laminate failures such as "eyebrow cracks" and Pb free related internal delamination is also explored. Video clips of laminate coupons during Pb free reflows are shown, including examples of failure mechanisms as they occur, to vividly illustrate the challenges involved and to help reveal the root causes. Finally, an extrapolation to future technology trends for laminate substrates is attempted to address the question—what might be the failure modes of tomorrow, and will via/laminate reliability be better or worse?

Introduction
The plated thru hole or via (PTH) has always been the most important element of laminate board and substrate electronic packaging, and in today's world of high density, high speed, and Pb free designs, that importance is only increasing in ways not imagined even a decade ago. For the first solder filled PTH of 40-50 years ago (via 1 in Figure 1), the only challenge was to find a process to drill, condition, and plate a relatively large, short hole such that the copper would adhere to the internal innerplane and side wall, and then survive the required solder passes without excessive copper dissolution in the solder melt. While the plating chemistries were archaic and deposited copper that would never survive the stresses of today's thru vias, fortunately the copper did not have to be strong—once the plated thru hole was filled with solder on the first assembly pass, the solder strengthened copper barrel would never fail in the z-axis. The only significant PTH reliability risk was separation of the barrel to innerplane (IP) connection in the X-Y plane (fail mode a in Figure 1); poorly processed connections could pull apart from the barrel as 360 degree separations during solder assembly and rework. The resulting separations were rarely "open enough" to be detected by in-circuit tests before or after assembly, but would result in latent and/or intermittent opens during product operation, thus starting the PTH's legacy as an element to be feared in terms of reliability. Lacking today's advanced hole clean chemistries, the positive etchback "3-point connection" was born as a way to mechanically enhance the barrel-to-innerplane connection. The challenges of the solder filled PTH peaked with the large ceramic pin grid arrays of the mid-1980's, where the size (>50mm) and mass of these pin in hole (PIH) components stressed the innerplane connection, copper dissolution, and surrounding laminate integrity to the maximum, but otherwise the early PTH offered little constraints on design wiring, manufacturability, choice of laminate material, or electrical performance.
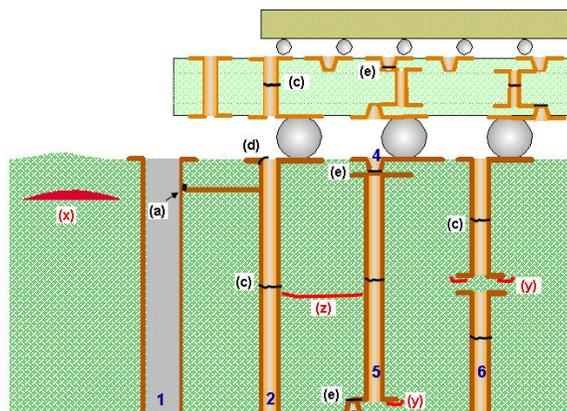

Figure 1—The "PTH" family and related failure mechanisms for today's boards and chip carriers.

The first significant change to the PTH occurred in the 1980-1990's with the advent of surface mount technology (SMT) where plated thru vias shrunk in diameter and were no longer solder filled, resulting in the "wiring via" (Figure 1 via 2). As SMT became ball grid array (BGA) technology, the tight grid and wiring demands of growing array sizes resulted in higher aspect ratio vias until, one by one, suppliers and users crossed the line and faced a new reality— non solder filled wiring vias may not even survive the stresses of board assembly and rework without cracking, especially if the plate is thin or defective in any way. And, as with its predecessor, this new failure mode (c) was often impossible to detect on an assembled board with in-circuit tests. When the author first published about this specific aspect of via failure in 1997[1], the phone rang monthly for years following with confirmations from both users and competitors of such problems with via cracks during assembly and escapes to the field. Of course, the root of this problem is the extreme difference in Z-axis coefficient of thermal expansion (CTE) mismatch between the copper plating and the laminate materials of printed wiring boards (PWB's) and laminate chip carriers (LCC's). This mismatch is especially extreme at assembly temperatures above the glass transition temperature (Tg) where laminate Z-axis CTE approaches 200–400 ppm/C, compared to 15 ppm/C for copper [1-9]. The two mechanisms, z-axis barrel crack and prior X-Y IP separation of solder filled holes, are similar in that they are both activated by assembly processes, difficult to detect with tests, and therefore can present latent or intermittent field risk. But the root causes and stress triggers of the failure mechanisms are entirely different, and required a paradigm shift in both processing and testing— for example, current induced heating replaced solder shock as a quality/reliability test for such unfilled vias, and the processes that produce the "3 point connection" to improve the reliability of a solder filled PTH IP connection can actually reduce the life of today's unfilled wiring vias [10,11].

As revolutionary as the BGA technology change was, the plated thru hole situation today is far more complex. The two main drivers for this complexity are high density interconnect (HDI) designs, and the inevasible demand for Pb free and mixed solder assembly (MSA) reflows. HDI not only adds several new structures to the PTH family as shown in Figure 1 elements 3-6, including microvias and buried vias, but it seems like no two HDI designs are ever alike—the microvias can be 1, 2 or 3 high, stacked or unstacked, filled or unfilled. The subcomposite structures can come with 1,2 or 3 subs per composite, often with mixed laminate materials, with buried vias of any size, and in many different forms: blind, core, or sub; filled or unfilled; capped or non-capped. Of course, these HDI newcomers to the PTH family bring with them at least two new failure mechanisms, which are once again reflow induced and very difficult to screen—base or pad separation (Figure 1 e) of the microvias[12], and eyebrow cracking (y) of the laminate driven near buried vias. Not only are there more failure mechanisms to monitor than ever, but they compete—which of the PTH and/or laminate mechanism dominate is a strong function of each HDI design. And finally, the need to survive Pb free and MSA assembly reflows has arrived, magnifying all the above failure mechanisms significantly, giving new life to former mechanisms, and introducing a unique PTH driven internal delamination mechanism[13,14] referred to as "invisible delamination" (z) in this paper. In short, the PTH has come a long way from the early days of one structure and failure mechanism, and similarly requires another series of significant paradigm shifts in how it is viewed during design, build, and testing phases of PWB development.

The purpose of this paper is to compare the structure and failure mechanisms of today's PTH family, which includes not only fails in copper, but also those induced by the PTH in the surrounding laminate because they all derive from the same root causes: laminate to copper CTE mismatch at assembly reflow temperatures. Moreover, understanding how they interrelate, for today and tomorrow's technology, is key to proper design and evaluation, especially with Pb free reflows.
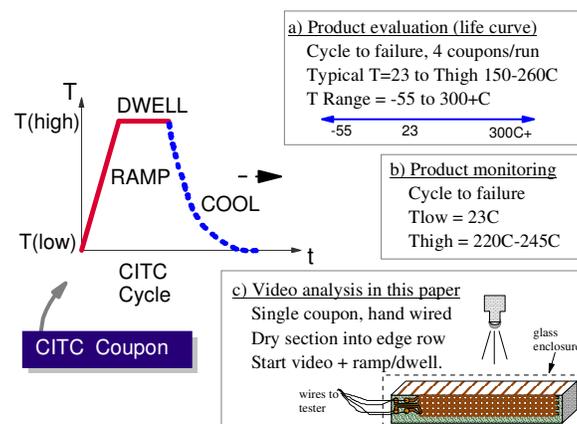

Figure 2--Definition of CITC test including use for videos in this paper.

The CITC Test
The test used in this paper as a means to measure via life as well as to produce videos of PTH deformations and failure mechanisms, and the main PTH test at Endicott Interconnect Technologies (EI) for the past 18 years, is the CITC test, our

version of current induced thermal cycling [1-5,15]. The tester uses proportional control algorithms to continuously adjust the current for each coupon in each cycle in order to achieve a precise and repeatable temperature cycle with a prescribed linear ramp and dwell time. The typical ramp rate, as used for all the data in this paper, is 3 degrees/second. The high temperature dwell time is typically between 30 to 40 seconds, which has been shown by modeling and measurements to be sufficient to achieve thermal equilibrium [5]. Fans are then turned on to start the cooling phase. Figure 2 illustrates the cycle, and also outlines the 3 main uses for the test as presented in this paper, including PTH life curves, rapid product monitoring or evaluations, and real time video recording of PTH failure mechanisms during a coupon heat cycle.

The PTH that started it all—high aspect ratio wiring vias revisited

The place to start a discussion of today's PTH and laminate problems is with a review of the standard wiring thru via— barrel life as a function of temperature, and video clips of barrel and laminate deformed state at reflow temperatures. The "PTH life curve" has been used by the author for over 15 years to characterize new materials or PTH structures, and to calculate via life for any combination of temperatures[1-4]. Figure 3 depicts some select recent and vintage life curves to review the problem that is behind all others—the CTE mismatch between copper barrel and the surrounding laminate at reflow temperatures can produce deformation of such magnitude that even well plated vias can survive only a handful of assembly passes without cracking. The 1998 red curve FR/4 (10mil vias/130mil thick PWB) is from a mixed resin system (note the 2 Tg deflection points in the curve) that is no longer commercially available, and which was the cause of several cases of PTH cracking based on industry discussions. The reason for such fails is clear from the curve at the "assembly" life end of the curve— well constructed coupons lasted less than 8 reflow cycles. Since 1-2 reflow cycles are required for SMT attach, and an additional 2 reflows for each rework (remove & replace), 8 reflow cycles to 220C could be envisioned during assembly. But more importantly there is no "safety factor" in 8 reflows—any increase in thermal exposure, or any form of thin plate or defect in the vias could easily account for assembly driven cracks, as was confirmed by industry experience. Failure analysis of the 8 cycle 23-220C CITC fails showed significant laminate and copper deformation. Note that if the same product could be shipped to the field without any reflow, it would survive (by extrapolation) over a million cycles of 23 to 75C!
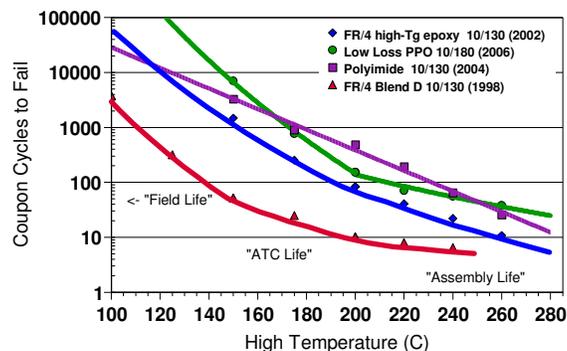

Figure 3-- Select CITC PTH life curves to illustrate challenge of unfilled wiring vias.

While Figure 3 shows the reason for assembly driven failed vias, Figure 4 illustrates why they can be a serious reliability concern as latent opens in the field. At reflow temperatures above the Tg of the laminate material, the z-axis expansion of the laminate is an order of magnitude much greater than that of the copper, which forces the copper in tension where it plastically deforms—i.e., the copper barrel becomes permanently longer than it was. Similarly, the laminate sees significant compressive forces in the zone around the PTH barrel because the barrel acts as a rivet to constrain it from expanding as it would away from the PTH. These considerable compressive forces create a pressure gradient that causes the laminate, now well above Tg, to "flow" away from the barrels. "Flow" is used in quotes because cross-linked thermoset polymers are not supposed to flow as other polymers, but some form of movement or reshaping is indicated by the permanent deformation seen in laminate x-sections after reflow or solder shock—the laminate is now longer between vias than in the zone directly next to them (Figure 4c). The combination of these permanent deformations (longer barrel, shorter laminate) means that any crack formed at the peak temperature will be forced in slight compression on return to room temperature. In addition to the illustration, figure 4 includes 1) ESEM photos of a barrel crack open at 230C and the same crack closed tightly again after cooling to ambient, and 2) electrical measurements of 8 coupons (left axis) with intentionally very weak barrels through a single simulated reflow cycle in a convection oven showing them open completely during heating (temperature, red line and right axis) between T = 140-185C, and close solidly to original resistance value starting between T=175-110C.

As further illustration and verification of the CITC data in Figure 3, since the red curve predicted failure within a reasonable number of experimental reflow cycles, a non tested block of 8 CITC coupons from the build was used to generate failure data with actual reflow passes. Because reflow induced barrel cracks are completely undetectable after cooling to room temperature as discussed above, this experiment required removal of a top panel in the first cooling zone of the reflow oven
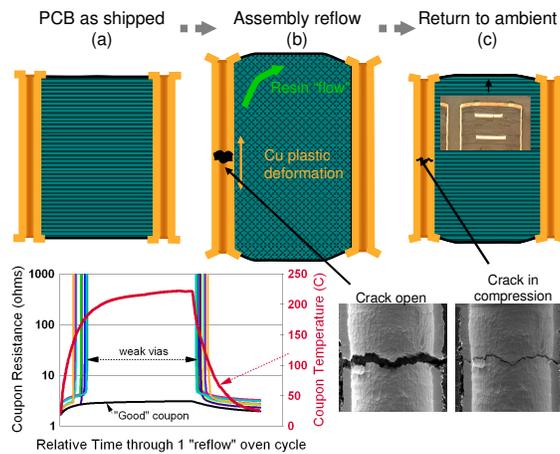
Figure 4-- Illustration, electrical data, and ESEM photos of deformations on a wiring via during assembly cycle.

to allow hand probing of the coupons right after the heating peak. That is, at the correct point (by timing) of each pass, the panel was removed and the part quickly measured with 4 wire resistance while still hot. Before pass 1, the oven was profiled with an identical block to 220C peak using the same timing and panel removal. The part was cooled to room temperature, and this process repeated up to 10 passes. Figure 5a plots the hot resistance by coupon and reflow cycle. A 3% failure criterion was used in this case, instead of 5 or 10%, because of the difficulty of reading all the coupons simultaneously while still hot, and because it appears to best fit the sharp slope change of the data. The final results are plotted in Figure 5b— the curve for cycles to fail from actual 220 reflow passes is almost identical to the 220C CITC cycles to fail curve.
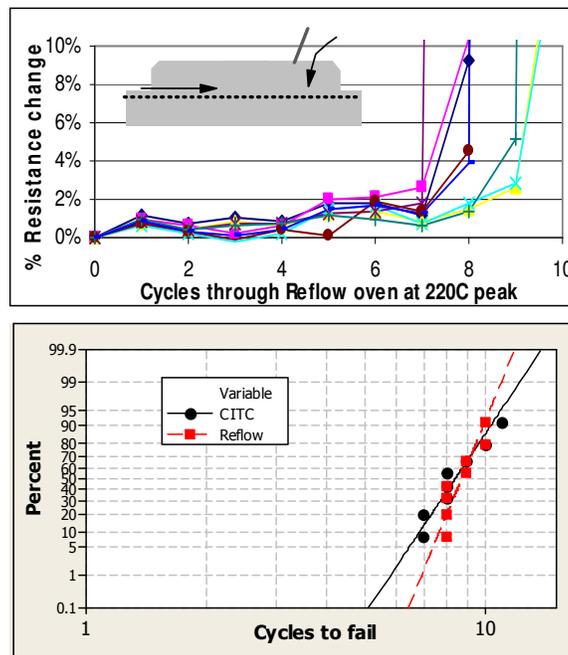
Figure 5-- -- Reflow verification for CITC data of Figure 3; (a) Coupon resistance vs. cycle measured inside reflow oven. (b) Probability plot showing identical cycles to failure between CITC and reflow.

Additionally, note the other material curves in Figure 3. The purple curve shows why polyimide, though expensive and a challenge to process at high aspect ratios, is a popular choice with the military for assembly robustness. The green curve is a high performance low loss PPO filled resin that consistently passes all Pb free testing, and has the overall best PTH performance of any laminate tested, but is still not a universal solution because its price-performance space is also likely outside most applications. Note that the blue curve is a cost effective high Tg phenolic epoxy with excellent PTH life in all regions including 220C assembly (40 cycles), and but at Pb free 260C it lasts only 10 cycles. That is, it can work for Pb free, but each 260C assembly or rework cycle consumes 10% of the PWB's PTH life, compared to only 1/40 of the life per cycle at 220C or 1/20 at 245C. This steep slope of PTH life reduction vs. reflow temperature introduces another point that will be made again in this paper—the key to a cost effective Pb free PWB product is not necessarily to find a material that survives a predefined number of cycles to exactly 260C, but to find a material that survives whatever that specific product requires after

| a) T=Ambient (start) | b) T=175C | c) T=220C | d) T=260C |
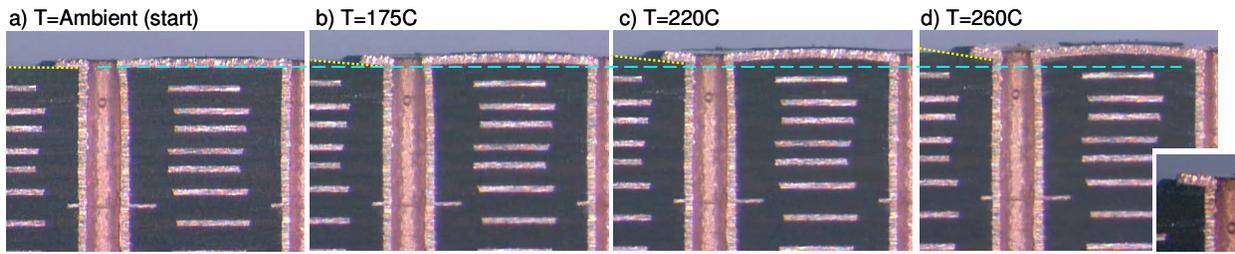
Figure 6-- Select frames from video of CITC coupon cycled ambient to 260C, 10mil via/180mil thick PWB.

aggressive optimization of the assembly process , because 5 or 10 degrees (and 1 or 2 cycles) can make a significant difference.

The magnitude and slope of the PTH curve at Pb free temperatures, as well as the challenge of Pb free assembly in general, is further portrayed by real time video of a coupon cross-section during a Pb free reflow. Figure 6 shows four select frame captures from the video of a high Tg epoxy coupon similar to that of the blue curve (this one was 10mil via on 180mil thick board) in a simulated single cycle from room temperature to 260C. Sample preparation and procedure was as shown earlier in Figure 2: sample was dry-sectioned to row 1, wired, and placed PTH-up in a glass frame under the camera. For this video, N_2 gas was leaked into the glass enclosure to limit oxidation of the copper during heating. The first observation from the figure is the significant deformation of the laminate, barrel, and lands at 260C. The difference in the two center frames between Pb free 260 and conventional 220C is staggering, but is consistent with the slope of the Figure 3 blue curve as discussed above, let alone general industry experience with Pb free assembly. The yellow dotted lines indicate measurements of the angle of deflection for the external lands: the lands deflected about 10 degrees at 260, 6.5 degrees at 220C and 5 degrees at 175C. The inset photo shows the permanent deflection of that same land (no longer adhered to the laminate) after on return to ambient after only a single 260C cycle, measured at 7.7 degrees, suggestion significant plastic deformation of the rim copper. Additional cycles at 260C are known to exaggerate the angle and/or protrusion of the land even further.

Finally, as if the Pb free situation was not complex enough, the magnitude of deformations at Pb free temperatures are so significant that they often trigger different and competing failure mechanisms along the life curve. While this fact does not invalidate the curves, it could have design implications, and it certainly sheds further light on the Pb free challenge. For example, Figure 7 is a life curve for a high Tg epoxy (more recent build than in Figure 3, though same aspect ratio) constructed with 2 different and independent CITC coupons—one with the daisy chain stitch external (top and bottom surfaces) and one with the stitch on the nearest 2 internal planes, top and bottom. The two coupon types yield exactly the same cycles to failure at 150C and 175C, and the same failure mode (center barrel crack), but they diverge slightly at higher temperatures—the external coupon with lower life in this case, fails at the external rim, while the internal coupon lasts a little longer but fails at the inner plane connection, at least at 260C. Note that inner plane fails observed at 260C are not related to poor barrel to innerplane connection, but rather appear to be ripped apart in a bending mode due to the same laminate deformation that bends the lands (only a few mils above where the first innerplane connection is located) as seen in Figure 6. Of course, the rim crack mechanism that activates on the external coupon at 260C in Figure 7 is similarly related to the same observations of Figure 6.
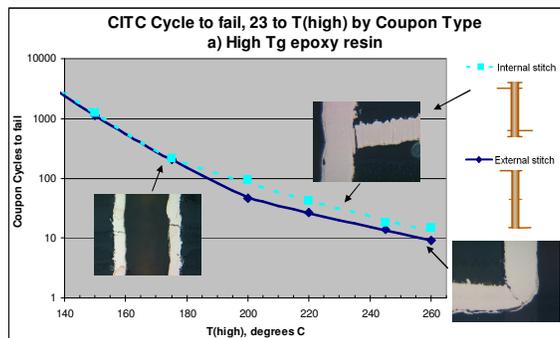
Figure 7—Failure mode shift vs. temperature for a High Tg epoxy resin, 10mil drill on 130mil thick board.

As a second example, Figure 8 compiles the results of the same experiment for a High Tg filled resin. The same 3 failure mechanisms "compete" again, this time with the inner plane failing slightly earlier than the rim at 260C, but both different than the center barrel crack than at conventional reflow temperatures. Note that none of the curves differ significantly, and a repeat of either test could yield a different result by material depending on plating thicknesses, etc, but these examples are otherwise provided as one more case for the complexity of assuring laminate boards for Pb free assembly.
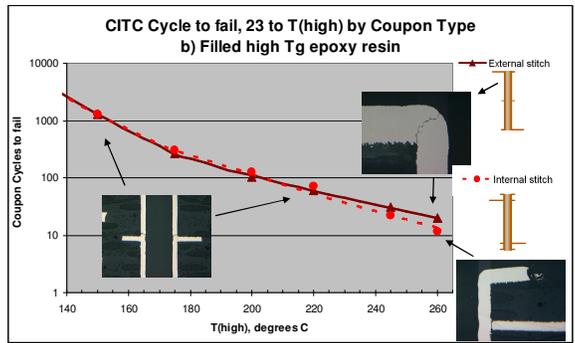
Figure 8—Failure mode shift vs. temperature for a High Tg filled epoxy, 10mil drill on 130mil thick board.

The enemy below—Visible and Invisible Delamination in Pb free assembly

Thermally induced internal delamination is one of the original and ever-present failure mechanisms for laminate substrates and boards. The root cause is generally linked to the "explosive" vaporization of entrapped moisture at high temperatures, especially reflow. The alternate names of blistering or popcorning not only reflect the mechanism but also hint at another fortunate attribute— when they occur within laminates of any thickness they create a measureable opening within the substrate that is almost always visible at the surface as a raised and/or discolored area. "Visible delamination" as such is typically observed in open areas with few vias, and/or in regions surrounding vias such as is shown in Figure 9c for a 130mil thick 10"x7" test vehicle (TV); cases of visible delamination on the TV are circled and numbered during reflow passes at 260C. The number is the pass after which it was observed (i.e., "2" = delamination was observed by inspection immediately upon removing card from reflow pass 2 at 260C). Note how the delamination rarely encroaches on via grids. The (a) and (b) insets show dry-section examples of visible delamination, typically cohesive within laminate material at glass to resin interfaces, near but not into vias seen further back in the section.
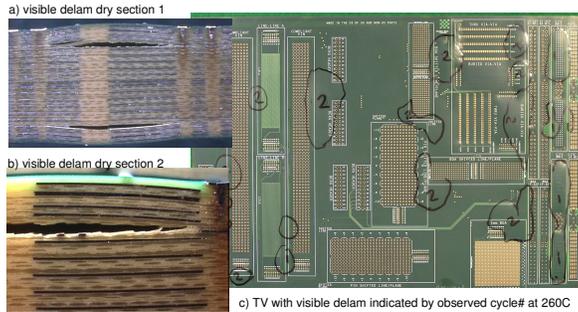

**Figure 9-- "Visible Delamination" during Pb free reflows on a high Tg resin board.**

Table 1 compiles the results of testing 9 different laminate standard and low loss materials using the same TV and approach at 3 different peak temperatures ; tabulated is the last successful reflow completed without visible delamination for 2 cards by temperature, up to 10 maximum. These test results were compiled in 2003-2005, with boards manufactured according to suppliers' recommendations at the time, but does not necessarily account for material and process improvements since then, nor any strict bake and bagging practices before reflow, which may improve the results incrementally. But any way that it is viewed, the results were shocking at the time.

Table 1-- Reflow passes without visible delamination by material and reflow peak temperature.

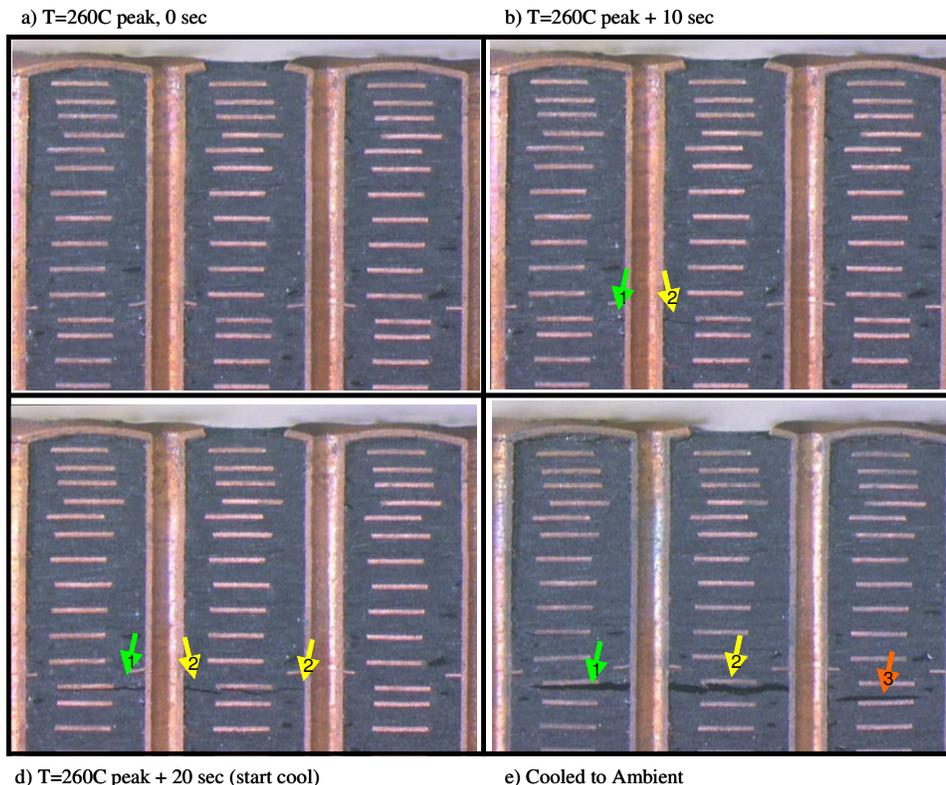| Material	220C	245C	260C
A	10+	10+	10+
B	10+	2	0
C	10+	1-3	0
D	10+	10+	10+
E	10+	3	0
F	10+	4	0
G	10+	4	0-2
H	10+	10+	10+

However, as Pb free evaluations continued, users and suppliers began to discover another form of delamination with clear distinctions from this classic visible form— the new type appears only between vias, not open areas; it occurs within resin

not at glass interfaces, and is highly dependent on the aspect ratio and grid of those vias. That is, for any given board thickness the mechanism would trigger above a certain hole density (below a certain grid), and usually near the center of the board[13]. The author prefers to call this new form after its most pragmatic difference and challenge— the significant void or hole it creates in the board, often spanning entire vias, is completely invisible from the surfaces. And except in a specially designed coupon where it can be detected as a capacitance change, it can only be found by x-sectioning. That is, there is no visible difference between a board module site that has this delamination versus one that does not. While most believe that at the very root both mechanisms are due to expansion/vaporization of trapped moisture with temperature, the unique nature of "invisible delamination" is so striking as to demand a greater understanding. Figure 10 shows a unique photo of invisible delamination found by x-section (in this case induced by solder shock, but otherwise the same as that found with oven reflows, and not a time-0 condition) that vividly answers why this mechanism is invisible— despite the large rupture between the two vias, there is otherwise little or no change to the surrounding material, planes, or dimensions. But this answer only raises new questions—how does the material within the rupture disappear as if to violate "conservation of mass", and how does this happen with little affect to surrounding laminate?
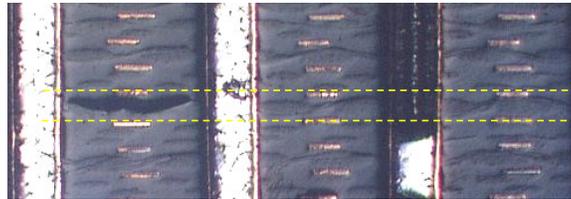
Figure 10—"Conservation of mass" dilemma with Invisible delamination—where does the material go?

To help answer these questions and further explore the root mechanism, the CITC video technique (Figures 2 and 6) was again employed in an attempt to record the formation of invisible delamination. The same type of coupon and setup was used except that the camera view must include the center of sample and more than a single cycle from 23 to 260C was required to activate the mechanism. During the peak dwell of the 7th cycle delamination was observed about 10 seconds after stable dwell at 260C, as shown by some frame captures in Figure 11. At point "2" in the figure, a sharp crack grew more than half way across the span quickly, within a second. At the same time a small crack grew on the other side at point "1". By 20 seconds, just before cooling was started, both cracks had grown, especially "2" which now spanned the distance between PTH's. As cooling started (fans), the cracks progressively opened until they appeared as the typical wide ruptures at ambient,

a) T=260C peak, 0 sec   b) T=260C peak + 10 sec

d) T=260C peak + 20 sec (start cool)   e) Cooled to Ambient

Figure 11--Frame capture from video showing formation of Invisible delamination.

as shown in the 4th frame of Figure 11. At the same time, a new rupture at point 3 appeared during cooling; apparently it also was created during the dwell, but not visible until cooling. The other randomly shaped small black spots in the laminate are artifacts of the dry section polishing, and should be ignored except that it is interesting to note that they shrink somewhat with cooling, as expected, unlike the cracks formed by this mechanism. Also note the significant permanent deformation of the copper and laminate even after cooling, as discussed in the previous section.

It is acknowledged that the "open face" of this sample is not the same 3D boundary condition as found in a whole board, but with the assumption that the basic formation and path of the mechanism is the same for this otherwise symmetric approximation, the most significant results of the video relative to understanding root cause are as follows: a) invisible delamination viewed at room temperature as a wide rupture is formed at high temperature as a fine and fast propagating crack, and b) the cracks start in the laminate closest to the barrel walls, where the laminate is under the greatest compressive stress. While initially striking, these observations are completely consistent with a possible failure scenario involving moisture induced rupture if one allows that:

1. The pressure of expanding vaporized internal moisture and pressure from the compressive forces from the via are "additive", creating an extremely high pressure on the polymer matrix of the resin, or otherwise "complementary"— the compressive pressure accelerates both microcracking of the resin and the diffusion of moisture into the microcracks.
2. the "explosive" rupture that results when this pressure exceeds some level for that resin will locally deform (crush) the polymer above and below the rupture, especially given its highly softened, rubbery state at such high temperatures,

While a crack formed under tension will contract when the tension is removed, a crack formed under compression will open when the compression is removed—thus, at room temperature these cracks appear as large voids of missing material with little change to the surrounding structure or geometry outside a very local area.

The above failure scenario not only explains the visual observations, but also accounts for the grid and aspect ratio dependence in at least one of two ways. Some have conjectured that thicker boards and tighter grids will have more entrapped moisture at the point of PTH plating, and therefore proportionally greater chance for invisible delamination. But the difference might also be seen in terms of stress—thinking of thru vias as rivets that work together to constrain the surrounding resin, higher aspect ratios and tighter grids will result in greater compressive forces in the zone surrounding the center of wiring vias. But if the moisture and compressive pressures are additive or complementary in some way, as proposed, then either or both explanations may apply.

Whatever the root cause, the most important question is how to control by design, evaluate with testing, and otherwise mitigate this unique Pb free failure mechanism given that its occurrence and severity is a strong function of: material, peak reflow temperature, board thickness, hole size, hole grid, process history including moisture content, and board construction (power vs. signal connections). Clearly, such a multi-dimensional problem demands an evaluation approach that is also multi-dimensional. That is, classifying a material as Pb free compatible or not based on a single coupon at 5x 260C reflow test is no longer viable as it may have been with solder shock of PIH technology. The author recommends a coupon approach such as is shown in Figure 12; at 1" wide by 5" long, the EI delam coupon is small enough to fit on the kerf of most production boards, and therefore reflect the design features of that board, but can also include enough design space variations to better answer the "Pb free or not" question for a particular material and construction. The coupon version shown has 7 different grids including 8mil vias on 0.8mm grid, 10mil vias on 0.8mm grid, 10mil vias on 1mm grid, 12mil vias on 50mil grid, etc. The coupon also includes nets for measurement of internal capacitance and 4-wire resistance of IP connections.
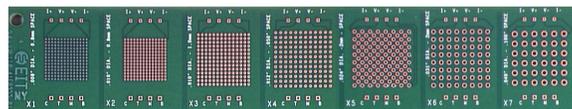
Figure 12-- Example of EI delam coupon, 1"x5" to fit on panel kerf; grids range start from 8mil drill on 0.8mm.

In addition to a coupon that extends the design space, the most useful results are obtained when the multiple temperatures and number of passes are evaluated. Table 2 shows results of EI delam coupons from 3 different boards at 2 reflow temperatures, illustrating the affect of grid, temperature, and material on this mechanism. But Table 2 is only a start. The space in between the "No" (i.e., no delamination) and the "Yes" is very important for the successful packaging user in 2009 and beyond, at least for those willing to accept that comfortably high margins on qualification test requirements will not always apply with today's packaging challenges. That is, as with the PTH life discussion earlier where the a few degrees lower peak temperature adds 50% or more to PTH life, setting the bar at "<5" passes at "<260C" can make a significant different in terms of activating invisible delamination, when combined with other best practices; so take advantage where possible! For example, our company has successfully manufactured both the boards and Pb free assemblies with more than one material, including the high Tg epoxy in line 1 of Table 2, in the last several years-- it simply requires the diligent combination of

design considerations, appropriate raw board processing and handling practices, aggressive dialing in and control of the Pb free assembly profile, and careful testing with the right coupons and approach.

Table 2-- Presence of invisible delamination on EI delam coupon by material and reflow pass

	5x 245C		5x 260C	
Material	1mm	0.8mm	1mm	0.8mm
High Tg epoxy 130mil board	No	No	Yes	Yes
High Tg filled epoxy 130mil	No	No	No	Yes
Filled PPO resin 180mil	No	No	No	No

**Now for something totally different: Eyebrow cracks**

As discussed earlier around Figure 1, HDI technology has introduced several new via structures and via-induced failure mechanisms to laminate packaging. One of the most interesting though elusive HDI failure mechanisms is the eyebrow crack, as shown by a couple examples in Figure 13. Though the origin of the name is unknown, the name becomes self evident to all who observe them. Eyebrows cracks form above, below, and between buried vias of sufficient size whether they are filled, capped, or not. The cause of eyebrows cracks is best understood by referring (once again) to the significant deformations involving and surrounding wiring vias, as illustrated in Figure 4 and video captured by Figures 6 and 11. If such thru-via related deformations can cause so many problems— PTH life reduction, lifted lands, IP cracks, and invisible delamination— then placing such structures inside a PWB is an example of how one cannot simply "bury his problems". At least in Figures 4, 6, and 11 the only stress on the surrounding laminate is compressive. But when thru vias become buried vias, laminated inside a composite structure, the same deformations result and can lead to tensile zones in the resin directly above and below the vias.
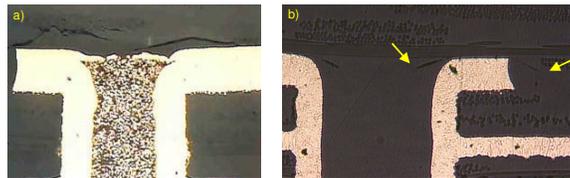

Figure 13-- Classic examples of eyebrow cracks after assembly

To illustrate, the CITC test is again used to capture with video the formation of eyebrow cracks in a worst case double subcomposite structure with a full grid of top and bottom buried vias. Figure 14 shows a macro view of 4 frame captures starting and ending with ambient; note that N_2 was not used in the glass enclosure, therefore copper will appear oxidized after the peak temperature exposure. Figure 14 includes a frame at 195C when the eyebrow cracks (4 total, above and below yellow center line) were fully formed, and a frame at 260C peak where they are more evident, somewhat longer, and more numerous (note 2 more at the top of the vias). But here, the difference between 260C and 195C is not as striking as with the prior mechanisms, which is consistent with industry experience that eyebrow cracks are by no means exclusively a Pb free problem, but can happen with any reflow. In fact, they may be as much a function of time as of temperature—the author has delaminated an entire module site due to interconnected eyebrow cracks simply by baking for several hours at 195C.

To better depict the formation of these cracks, additional frames focusing on the critical zone are shown in Figure 15. The first hint of the cracks or at least their eventual path is seen at T=175C (b). At T=189C, note the small eyebrow shaped start of cracks at points 1 and 2. Within a few seconds, by T=195C, these have propagated fully across the land diameters. Cracks

| a) Ambient 0 sec	b) T=195 62 sec	c) T=260C 85 sec	d) Cooled to Ambient
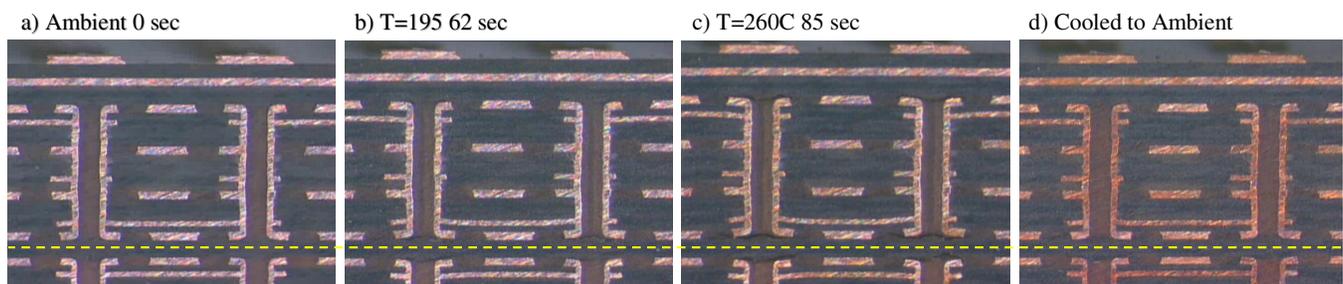
Figure 14-- Frame captures from video of eyebrow crack formation in a double subcomposite board.
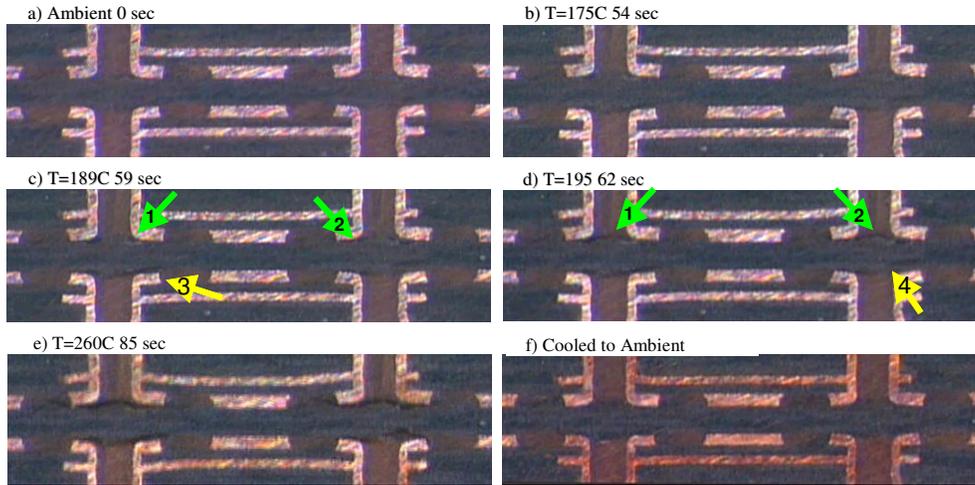
Figure 15-- Close-up of eyebrow crack formation in previous figure.

3 and 4 show a somewhat different formation path and look. Crack 3 simply becomes more visible with temperature, without the propagation of 1 and 2. Crack 4 starts as two separate cracks which apparently start far enough apart that, though they grow toward the center, they never join together. All the cracks close back up on return to ambient and are no longer visible, at least at this magnification.

Note the thermal induced deformation of the vias, lands, traces, and laminate in the middle 2 frames of Figure 14, compared to the ambient frames— the magnitude of the deformation is scaled down with aspect ratio, but the same shape as is observed as with thru-vias of Figure 6. But in the case of buried vias observe how the deformed shape, especially the land deflection, would create a tensile zone in the joining resin just above the lands and vias. Resins can withstand reasonable tensile forces below Tg, but above their Tg they tear easily when pulled in tension. This root cause of the eyebrow crack is further illustrated in Figure 16, which is a close-up of the left most via pair in the above Figures at ambient, and at a peak of 245C. To better compare relative shape and deformation, the 245C image is shown flipped 180 degrees vertically. Dotted reference lines are drawn at the indicated locations a, b, and c for both temperatures. Note the distinct tensile zone visible in the region of the via rims (at arrows), exactly where the eyebrow cracks were seen to start and grow in the above Figures.
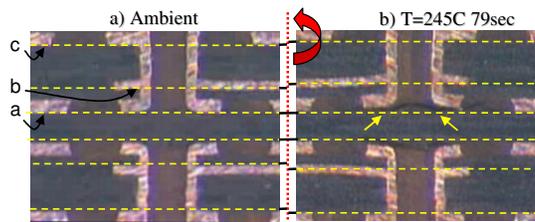
Figure 16— Comparison of T=245C versus ambient frames to illustrate tensile zone that causes eyebrow cracks.

As discussed previously, these videos are intended to be illustrative of the particular failure mechanisms, not representative in every way of the real case since one half of the board had to be removed in order to see the fail occur. In this case, the open face must be somewhat worst case because actual pieces of this product x-sectioned after reflow (220C peak) did show eyebrow cracks, but they were not the full span as seen here (see right side of Figure 13 for a worst case example on this actual board after 5x simulated reflow). Of course this point raises the next question—what is the reliability impact if any of these cracks, and how far do they need to grow to be a problem? Ignoring them is not an option, as they are almost universally present in HDI boards, though usually as the small and benign "baby eyebrow" variety. But the author has heard from others of cases where they become large enough to be a potential serious problem. As with everything else in this paper, success will not come by accident with today's complexity, but requires balanced design, expert and quality build, and rigorous evaluation based on the best available knowledge of today's failure mechanisms. Table 3 attempts to compare the above three laminate mechanisms, particularly to highlight their differences. All three mechanisms are dependent in some way on choice of laminate material, reflow peak temperature, PWB processing, and total cycles, but otherwise they are significantly different in key ways, which affects how and where they need to be considered in design and evaluation.

**Table 3-- Comparison of today's laminate failure mechanisms**

Attribute	Visible delamination	Invisible delamination	Eyebrow cracks
Geometry vs. temperature	Open at peak as formed, open at ambient	<u>Closed</u> at peak as formed, open at ambient	Open at peak as formed, <u>closed</u> at ambient
Locations where mechanism is active	Open areas (no vias) or loose grids	Dense, tight grids of thru vias	Above, below, or between buried vias.
State of stress during formation	Neutral	Compressive	Tensile
Aspect ratio and/or thickness dependence	None	Yes, both.	Yes, likely function of via dia & length.
Moisture/bake influence	Yes, to a point	Yes, to a point	No
Non-destructive inspection/screen	Yes, almost always.	No	No
Typical interface fractured	Resin to glass	Resin to resin	Resin to resin

HDI—Design vs. Reliability

The real surprise and complexity of HDI is not only how many different via structures and combinations that it adds to the design mix today, but also how strongly dependent is the link between specific designs and reliability. In BGA technology of the 1980-1990's, two different products may have a different number of wiring vias on a different thickness board, but the failure modes and overall reliability were quite predictable, even if challenging at high aspect ratios. And once a "design space" was qualified, specific products did not have to be requalified with testing to know they would work. But the large number of via types and constructions available to the HDI designer, let alone combinations thereof, often with mixed materials within the composite, lead to a complexity not known before especially when combined with the narrow margins of Pb free assembly. The key to quality and reliability assurance is to know the "weakest link" for any specific product, but for HDI designs that is often difficult to predict: will it be the microvias or thru vias, or for that matter, a laminate failure mode induced by the vias. Fortunately, there are at least some "rules of thumb" that apply to this design vs. reliability question.

Figure 17 compiles relative via life for 2 different HDI products, one PWB and one dense LCC substrate. Each product had individual CITC coupons covering the 4 different via constructions shown. Relative life is calculated by testing all coupons to fail at CITC 23-220C, and then comparing N50's with a lognormal probability plot. The coupon with the lowest N50 is listed first and defined as with base life =1. In both cases, the first coupon is that structure which most closely resembles a "thru via", which becomes the first rule of thumb—thru vias or any facsimile see the full force of the Z-axis CTE mismatch as demonstrated by data and photos earlier. That is, the full stack of example <u>a</u> is expected to have about the same via life, and the same propensity for thru via related laminate failure mechanisms if present (e.g. invisible delamination), as would be the equivalent thru via. Therefore in the first example, the full stack structure had the same failure location (indicated with arrows based on failure analysis x-sections) as the next 2 structures, but with cycles to fail 1/3 and 1/4 the values, respectively.

In example <u>b</u>, the first structure is a modified full stack, most similar to a thru via of the four coupons but lacking the full "rivet" nature of a thru via or full stack. Note that though this modified stack is still the first to fail and with the same failure mode as the second coupon, the margin is much closer attributed to the fact that structurally they are more similar than in the first example.
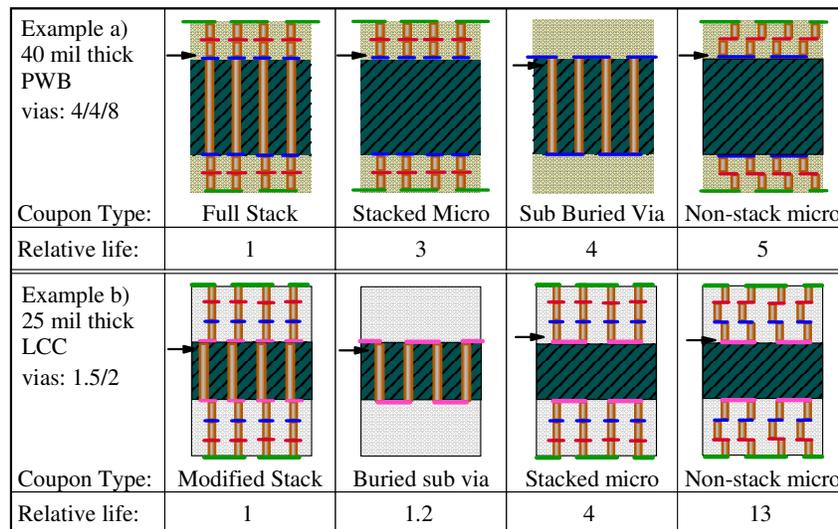
Figure 17-- Relative life by structure for two HDI examples, PWB and LCC.

a) ambient   b) T=220C end of dwell   c) cooled back to ambient


Figure 18-- Frame captures from HDI reflow cycle video

Interestingly, this first rule of thumb also applies similarly on a small scale to microvias.   In both examples of Figure 17 the microvias had excellent life, but stacked microvias fail before unstacked microvias, with all else held constant—this is because they are locally more "thru-via" like in geometry and stress state, while the unstacked microvias have an additional degree of freedom in which to flex, reducing the stress on the copper. This situation is illustrated by a final video in Figure 18 for a substrate with 3+3 microvias on a buried via subcomposite. The substrate is cycled from ambient to 220C and back again (no N_2). The yellow dotted lines are drawn from the build-up layers at ambient to help show both the Z-axis expansion, and more importantly, the flexing of the non-stacked microvias that occurs at 220C (red arrows). It is clear how this flexing can reduce the stress on the microvia itself, and explains how unstacked microvias last longer than the stacked microvias, which like small "thru vias" are not able to flex.   Note however that an eyebrow crack was formed at the green arrow during dwell at 220C, which becomes a "reality check" reminder that at least one more rule of thumb is needed: the reduced stress on copper via interconnections in a "less thru-via-like" design comes with a price— possibility of tensile stresses in the resin, and therefore greater risk of eyebrow cracks.   Or stated in more general terms, different HDI structures may trade one failure mechanism for another, once again reiterating the need for smart design and evaluations.

Future technology and a look ahead—smaller is better
If the past couple decades have seen such an increase in complexity and failure mechanisms, both laminate and copper related, what will be the expectation for future technology—does it stand a chance? While this question is impossible to answer now, the good news is that all the via structures of future technology will be forced to get smaller and less thru-via like. Interestingly, for all the failure mechanisms reviewed in this paper, smaller is better! For example, Figure 19 shows an example of a leading edge board constructed with Z-interconnect, which is the only means to meet electrical requirements (no via "stubs") and/or wiring demands in some cases, especially in the future. While the Z-interconnect itself is of course a challenge, the product shown so far appears to be resistant to the mechanisms discussed here-in. There are no thru vias, and the "thru-via" like nature of what is small and non-dense enough to escape both invisible delamination and eyebrow cracks, at least with the materials and parameters evaluated so far.   Readers are encouraged to employ similar analysis in looking at other examples of future technology, as well as those in design today.
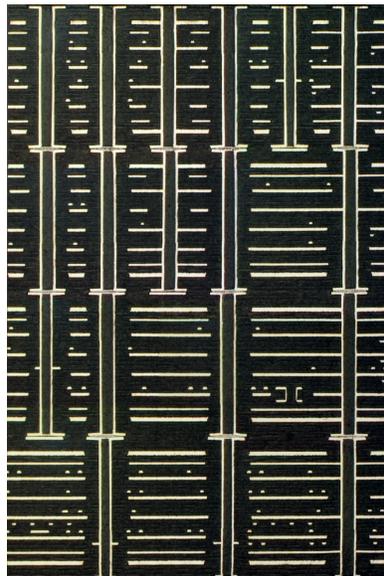
Figure 19-- Example of emerging technology-- HPC-Z_{ei} 390mil thick Z interconnect PWB with 8mil vias in 4 subs.

Conclusion

The complexity of laminate electronic packaging in terms of design, build, and reliability evaluation has reached a level today never imagined when the first PTH was filled with solder over 50 years ago. Today the design and process engineers have to deal with thru vias, microvias, buried vias, and Z-interconnect, each of which can be used blind or buried, composite or subcomposite, filled or unfilled, capped or uncapped, stacked or unstacked, and assembled with either SnPb, MSA , or Pb free solders. Then quality and reliability has to be assured with a seemingly infinite mix of potential failure mechanisms that can occur either in the vias or induced by the vias in the surrounding laminate depending on the above design mix, process choices, and even last digit of the optimized peak assembly temperature.   The successful user of this technology, today and tomorrow, will be those that neither over-react nor under-react, but recognize that:

1. The comfortable qualification margins of past product may longer be possible with today's HDI designs and Pb free reflows— reflow and via life requirements may need to be tailored for a specific product with the smart and innovative use of coupon tests.

2. Thorough evaluation and rigorous monitoring of products will become even more important given these margins.

3. "Design for reliability" is now as important as design for electrical and wiring needs, balancing the potential risks of via failure versus laminate failure based on material choice, via size and grid, and mix of thru vias versus compliant HDI structures.

Acknowledgments

References

1. Knadle, K.T, Ferrill, M.G., "Failure of Thick Board Plated Through Vias with Multiple Assembly Cycles—The Hidden BGA Reliability Threat", SMTA Journal of Surface Mount Technology, Vol 10, Issue 4, October 1997, www.smta.org.

2. Knadle, K, "Proof is in the PTH – The Critical Link between PTH processes and PCB Reliability", Endicott Interconnect Technical Symposiuma July 2003- October 2003.

3. Knadle, K.T., Jadhav, V.R., "Proof is in the PTH-- Assuring Via Reliability from Chip Carriers to Thick Printed Wiring Boards**,** ECTC Confereence proceedings, 2005.

4. Knadle, K.T. "Analysis of Transient Thermal Strains in a Plated Through Hole using Current Induced Heating and Transient Moire Interferometry" Master's Thesis, Binghamton University, 1995.

5. Ramakrishna, K., Sammakia, B., "Analysis of Strains in Plated Through Holes During Current Induced Thermal Cycling of a Printed Wiring Board", 7th Symposium on Mechanis of Surface Mount Assemblies, 1995.

6. Iannuzelli, R. "Predicting Plated-Through-Hole Reliability in High Temperature Manufacturing Process" ASME Conference Proceedings, November 1994.

7. Gross, T., "Deformation of Plated Holes: The First Soldering Thermal Cycle, EEP-Vol-4-1, Advances in Electronic Packaging, ASME 1993.

8. IPC-TR-579, "Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards".

9. Estes, T.A. "The effect of Lead-free Reflow Profiles on Through Via Reliability", IPC D-36 Subcommittee report from IPC PCQR2 database, February 2005.

10. Trakas, G., Hoeppel, G., Cai J., "Etchback and its Effect on PWB Reliability", www.coretec-inc.com.

11. Unpublished internal and customer related CITC testing by the author.

12. Andrews, P., Parry, G., Reid, P., "Learning from Microvia Failure in Lead-Free Assembly", PCD&M, June & July 2006

13. Rothschild,W., Kuczynski, J., "Lessons Learned about Laminates during Migration to Lead-Free Soldering", Proceedings of IPC APEX 2007.

14. Ehrler, S., "The Compatibility of Epoxy-based Printed Circuit Boards with Lead-free Assembly", Circuitree, June 2005, pp. 30-42.

15. IPC-TM-650 2.6.26 DC Current Induced Thermal Cycling Test.

16. Engelmaier, W., "Printed Circuit Board Reliability: Needed PCB Design Changes for Lead-Free Soldering", Global SMT&Packaging, September 2005, pp. 41-44.

17. Kelly, E., Bergum, E., "Laminate Material Selection for RoHS Assembly", PCD&M, November & December 2006.