Package on Package (PoP)
Stacking and Board Level Reliability, Results of Joint Industry Study

Moody Dreiza, Lee Smith - Amkor Technology
Gene Dunn - Panasonic Factory Solutions
Niranjan Vijayaragavan, Jeremy Werner - Spansion

ABSTRACT / SCOPE OF WORK

This paper presents the results of a joint - three way study between Amkor Technology, Panasonic Factory Solutions and Spansion in the area of package on package (PoP) board level reliability (BLR). [BLR is also referred to as second level or solder joint reliability within the industry]. While PoP is experiencing exponential growth in hand held portable electronics applications, as reported by iSuppli [1] and others, to date PoP BLR data has been customer specific and not available for industry publication. Significant company internal and industry data exists to help optimize designs for BLR performance in 0.5mm pitch, Pb free fine pitch BGA (FBGA) or chip scale packages (CSP). In addition new work has emerged in 0.4mm pitch CSP as reported by Scanlan, Syed, Sethuraman**,** et al [2]. However, industry data specific to the reliability of the top to bottom PoP - BGA interface has been critical to designers in planning for new PoP applications or configurations. In addition, data was needed to validate whether current best practices for Pb free reliability performance of bottom 0.5mm pitch BGA to mother board interface still applies in PoP stacked structures.

The goals of this collaborative study were to:

- Compare popular Pb free ball alloys and BGA substrate pad finishes to determine, which solder joint and BGA pad finish structures show the best BLR cost / performance balance for the BGA interfaces.
- Establish collaborative PoP supply-chain relationships in order to generate applicable BLR data and make it broadly available to the industry.
- Ensure that PoP BLR data generated is comprehensive – based on the high volume design and manufacturability considerations for top, bottom packages and final PWB assembly.

This joint work is part of an ongoing project Amkor has planned to cover multiple package sizes, and stacking interface structures in support of aggressive PoP roadmaps. This paper is the first in a series of planned data releases to help facilitate PoP advancements, infrastructure development and industry standardization. The scope of this paper is to cover the already popular 14 x 14mm PoP package size that provides a 152 pin stacked interface which supports a high level of flexibility in the memory architecture for multimedia requirements.

This paper will summarize:

- The structure and reliability monitoring benefits of a three net PoP daisy chain design.
- Process flow, conditions and benefits with the single pass reflow SMT stacking process applied in the PoP stacking build.
- BLR test conditions and report reliability results measured.
- Concludes with suggestions for optimum BGA pad surface finish and Pb free solder ball material selection.
- Indicate areas planned for study in future PoP projects.

KEY WORDS and ACRONYMS

3D packaging, Stacked package, Package on package, PoP, PSvfBGA, multi-chip package, MCP, stacked CSP, Board Level Reliability, BLR, Solder Joint Integrity, Solder Joint Reliability, SJR, second level reliability.

INTRODUCTION / MARKET DRIVERS

Integration of popular “convergence” features and functions is key to meeting mobile consumer’s demands in hand held electronic equipment designs. Products that achieve high levels of integrated communications, computing and entertainment-multimedia features in small, stylish and robust new form factors are winning in the market place. Even in

markets with high levels of penetration for mobile phones, digital still cameras, PDAs and MP3 players; consumers are showing a strong willingness to upgrade to smaller and more function filled hand held devices.

Hand held system designers have to increase the semiconductor content to provide the seamless connectivity / interoperability, multimedia processing and memory capacities required in these function filled devices. To integrate higher levels of semiconductor content without limiting size and form factor flexibility, designers increasingly look to 3D packaging technologies. Historically, higher levels of silicon integration in 3D packaging has been the domain of semiconductor suppliers through the use of stacked die packaging technologies. This history from FBGA to 3D stacked CSP memory device packaging, to enable higher levels of functional integration in mobile handsets has been widely reported including the well publicized paper by Kada and Smith[3]. However, today's system designers demand a new class of 3D packaging technology to address the following set of technical, business and logistic requirements:

- Ability to cost effectively stack logic based digital signal and multimedia processor devices with high capacity and or combination memory devices - without limitations from wafer supply, KGD, test, supplier cooperation or time to market.
- Ability to multi-source devices to be integrated, to achieve lowest total cost and flexible, responsive sources of supply.
- Ability to maintain flexibility in the memory architecture to customize the memory content to the specific product requirements.
- Ability to finalize the memory content and supplier selection late in the product launch to readily adjust to changing market requirements.
- A 3D packaging technology platform supported by industry standards with a broad infrastructure for reliable adoption, ready reuse of technology and dependable sources of supply.

Today PoP is seen by system designers and semiconductor suppliers as the leading 3D packaging platform to address this challenging set of requirements. The structure and design rules for PoP, has been reported by Dreiza et al [4]. Currently the dominant use of PoP packages is to integrate a high density digital logic device in the bottom (base) package with high capacity or combination memory devices (i.e. DRAM and flash) in the top (stacked) package. New PoP designs typically include 2 to 4 stacked memory die in the top package and 1 to 2 stacked logic devices in the bottom package. The 2 package layer, 3 die, package stackable very thin FBGA (PSvfBGA) based structure shown in the top of Figure 1 was used in the BLR studies reported here. The low profile substrate cavity based PSetCSP structure was first reported by Smith and Zoba [5] . PSetCSP stacking and board level reliability was reported by Yoshida and Ishibashi [6], [7]. Yoshida et al. will also be reporting a detailed study concerning stacking yield vs. warpage impact for this same 14x14mm PoP configuration [8].

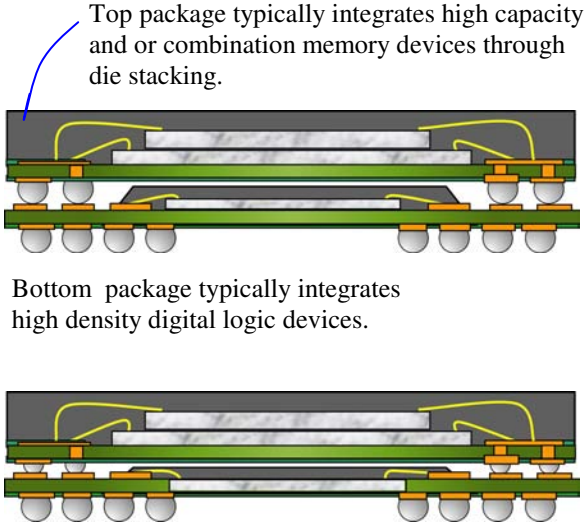


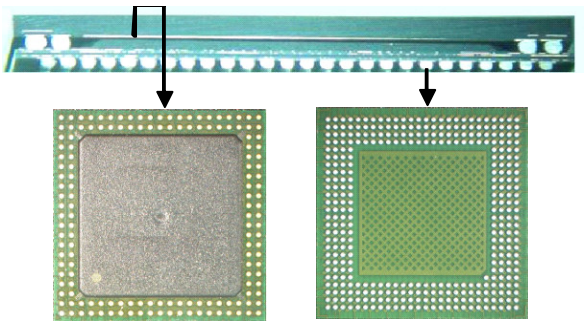
Figure 1. Typical Package on Package (PoP) cross sections:

Include higher density PSvfBGA base structure, top figure and lower profile cavity type PSetCSP structure, bottom figure.

TEST VEHICLE AND DEFINITION OF EXPERIMENTAL LEGS

The test vehicle used on this study complies with JEDEC Publication 95, Design Guide 4.22A for PoP, consisting of a 14 x 14 x 1.5mm PoP 3 net daisy chain stack up. The bottom package is based on Amkor's multiple award winning [9] PSvfBGA platform, with 353 bottom perimeter Pb free 0.3mm diameter solder balls in 26 x 26 BGA matrix at 0.5mm pitch, solder to the test boards. And 152 perimeter top lands in 2 row 21 x 21 matrix at 0.65mm pitch to receive the top stacked daisy chain package as shown in Figure 2.

Figure 2. PoP test vehicle cross section



PSvfBGA top side 152 lands around the mold cap.

PSvfBGA bottom side 353 perimeter balls.

A total of 5 legs, as shown in Table 1, were studied for this 14mm PoP stack to determine optimum Pb free material set for the interfaces.

The top package across all legs was consistent, using NiAu BGA pad finish for interface A, with Pb free SAC405 (95.5 % Sn, 4.0 % Ag, 0.5% Cu) 0.42mm diameter solder balls. Also for all legs, standard JEDEC test boards were used (interface D) with Cu OSP pads with non solder mask defined (NSMD) pad design.

The BLR study variations occurred for interfaces B and C as well as the Pb free ball alloys for bottom 0.3mm diameter balls attached to interfaces C and D as shown in Table 1.

The die sizes and resulting package warpage profiles for the test vehicle parts were engineered to minimize warpage both at room and the critical solder liquidus - reflow temperature, per Yoshida et al's findings [8]. This was done in order to minimize the impact from variability due to poor joint wetting and resultant poor solder joint integrity which can result when PoP stacks have not been characterized or optimized for warpage control and high stacking yields. In fact, the one pass reflow SMT stacking process at Panasonic, using conventional top package tacky flux dip, resulted in nearly 100% stacking yield.

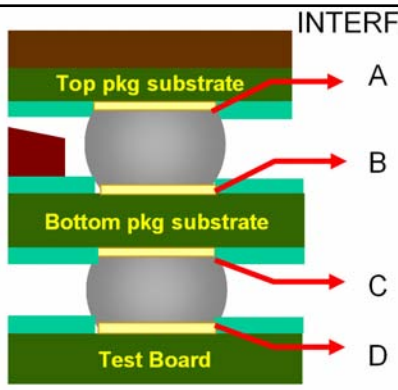


Table 1. 5 Leg BLR matrix and critical solder joint interfaces evaluated.

Leg #	Pad finish	Solder ball	Pad finish of bottom package		Solder ball	Additional Comment
	Top pkg (A)	Top pkg	Top side (B)	Bottom side (C)	Bottom pkg	
Leg 1	NiAu	SAC405	NiAu	NiAu	SAC3.0	
Leg 2	NiAu	SAC405	CuOSP	CuOSP	SAC3.0	
Leg 3	NiAu	SAC405	CuOSP	CuOSP	SAC3.0	Multiple reflow passes by to simulate prestack
Leg 4	NiAu	SAC405	NiAu	CuOSP	SAC3.0	
Leg 5	NiAu	SAC405	NiAu	CuOSP	LFA3	

Figure 3 illustrates the 3 net PoP daisy chain design of the test vehicle. The first net (i) monitors the joints on the bottom side of the bottom package. The second net (ii) monitors the majority of joints in the critical stacked "memory" interface between the packages. Finally net (iii) monitors the 12 top corner joints in the interface which is considered to be the highest risk net, typically used as no connects and only committed to I/O in highest density designs.

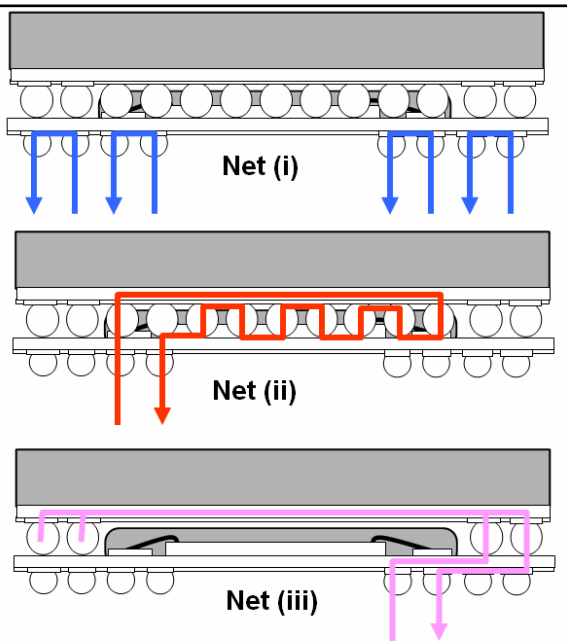


Figure 3. Three net monitoring PoP test vehicle design.

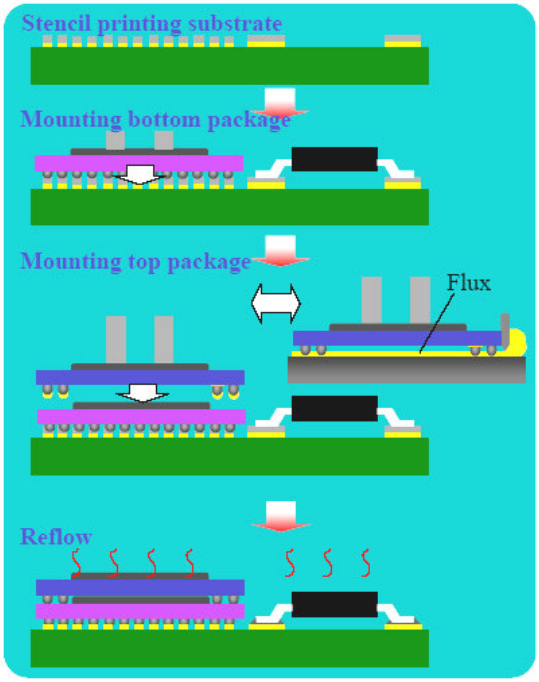


Figure 4. Flow chart showing single pass SMT Stacking applied by Panasonic.

ONE PASS REFLOW SMT STACKING PROCESS

The Panasonic process and flux dip material selection was applied in order to emulate standard factory SMT stacking setups. Thus, air (non-nitrogen) reflow, standard tacky flux (not solder paste loaded flux) dipping was used.

The flowchart shown in figure 4 describes the PoP stacking steps for a one pass reflow process. First, the PCB substrate is paste printed utilizing a metal stencil. The PCB is passed to the SMT placement machine and all the bottom packages are picked and placed onto the paste. (The SMT placement machine is configured with a flux dipping station). Next the top package is picked, dipped into the flux station, top component vision recognition is performed, and the part is stacked on the bottom package.

After all top packages are picked and stacked, the tacky flux holds the PoP stack in place as the assemble board is passed through the reflow oven.

The equipment used for POP stacking is similar to SMT machines found in factories doing advanced BGA/CSP assembly. Starting with the stencil printer, we used a Panasonic SP60 model with +-25 micron accuracy, metal squeegees, and bottom side stencil cleaning. For package stacking, a Panasonic DT401 model with JEDEC tray feeding and flux dipping station was used as shown in Figure 5. This machine is capable of +-35 microns placement accuracy and all ball recognition of the CSP packages. Reflow was performed on a Heller 1800EXL nine zone convection reflow oven.

DT401 Flux Transfer Unit

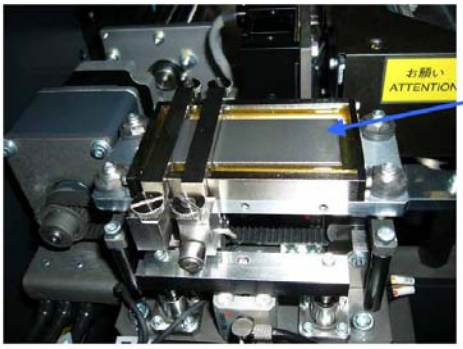


Figure 5. Panasonic DT401 with close up view of the flux transfer unit.

STACKING RESULTS BEFORE BLR TESTING

The stacking results were carefully analyzed to ensure that the good joint formation had been achieved and that warpage did not play any factor in skewing the BLR data. As shown in Table 2, the process and packages achieved excellent stacking yields with only one defect reported across all legs.

Table 2: Stacking Yield Summary

Leg	Net Yield After Stacking (Before BLR)		
	i	ii	iii
	Bottom	Top Middle	Top Corner
1	90/90	90/90	90/90
2	90/90	90/90	90/90
3	90/90	90/90	89/90
4	90/90	90/90	90/90
5	90/90	90/90	90/90

JEDEC TEST CONDITIONS

Each leg was subjected to JEDEC drop testing per JESD22-B111 and IPC-9701 temp cycle condition 1 as described in Table 3 below.

Table 3: BLR test quantities

PoP BLR Testing 14x14mm Program					
	Number of units per leg	Number of nets per unit	Mounted Packages per Board	Number of channel per board	Number of boards per leg
Temp Cycle	30	3	10	30	3
Drop	60	3	15	45	4

IPC Temperature Cycle 1 Test:
-40 to 125 °C, Slow Ramp, 1 Cycle/Hour, 15 minutes ramps and dwells

JEDEC Drop Test:
1500G peak acceleration, 0.5ms duration time

BLR DROP TEST RESULTS

The drop results are summarized in Table 4 and plotted in Figure 6. Failure analysis (FA) was in process at abstract due date, so additional data by net and component location, will be presented at the conference. To expand on figure 3, we can state that:

- Leg 1 had the highest number of total and early failures reported across all 3 nets.
- Legs 2, 3 and 5 saw no failures up to 200 drops for nets (ii) and (iii). That is, there were no failures between packages.
- Leg 4 had only 2 failures between packages, nets (ii) and (iii), but these were at 171 and 172 drops well exceeding pass criteria.

Table 4. Drop test results

Drop Test Failures - 14mm PoP					
Failure Order	Leg 1	Leg 2	Leg 3	Leg 4	Leg 5
1st	1	29	43	16	
2nd	2	32	51	25	
3rd	2	42	57	93	
4th	4	42	63	95	
5th	4	51	73	134	
6th	5	62	121		
7th	11	82	124		
8th	17	126	148		
9th	61				
10th	112				
11th	128				
12th					
13th					
14th					
15th					
16th					

	: suspended data
	: no failure until 200 drops
#	: 1st failure

From drop results we draw the following conclusions:

- Achieving a solid foundation is the most critical mechanical interface to optimize in PoP. The use of CuOSP with LFA3 ball (Sn with 1.2% Ag, 0.5% Cu + 0.05% Ni) shows the best performance. (This combination is validated in other Pb free drop work).
- While interface B (bottom package top land finish) did show some improvement with CuOSP finish versus NiAu, these slight improvements are considered outweighed by additional costs in substrate and assembly fabrication, and are not recommended for volume production at this stage.
- Further studies are planned to look at impacts when the top package uses CuOSP BGA pad finish with LFA3 solder balls.

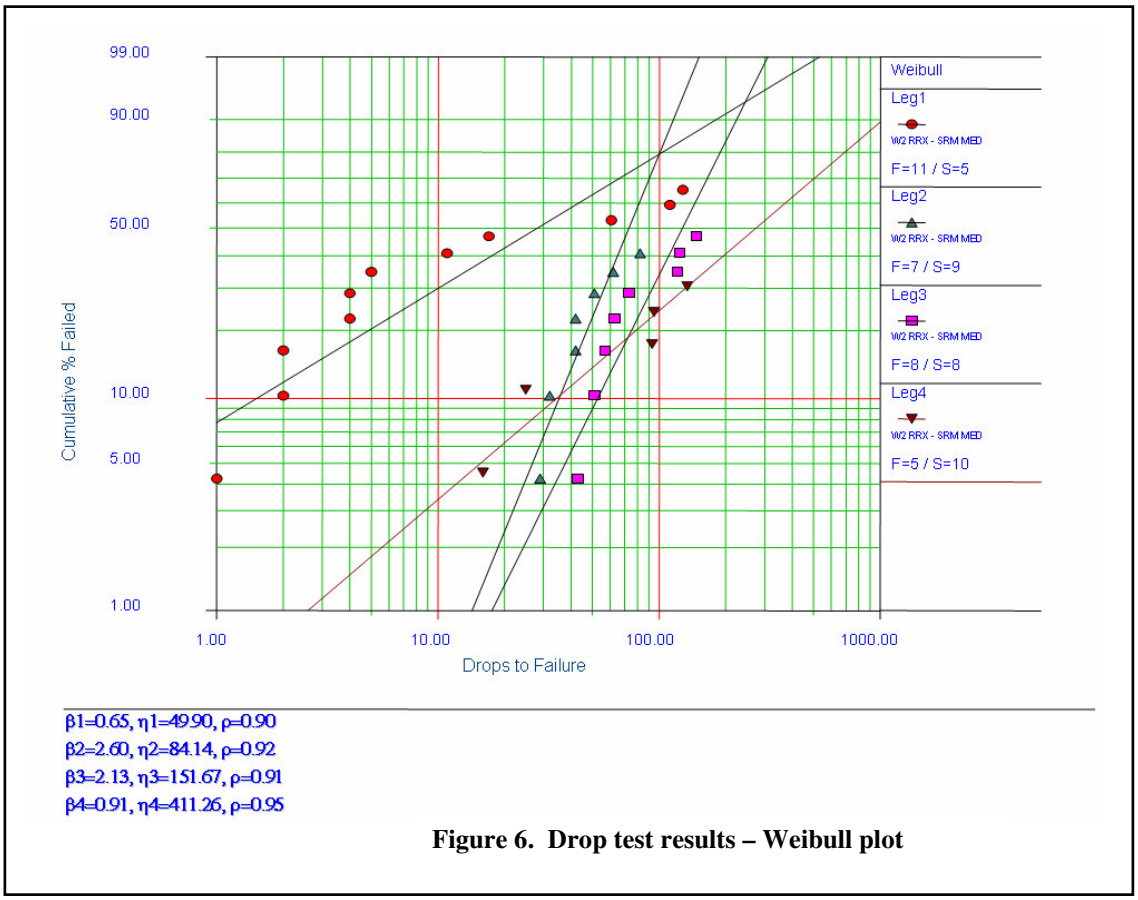


Figure 6. Drop test results – Weibull plot

BLR TEMPERATURE CYCLE TEST RESULTS

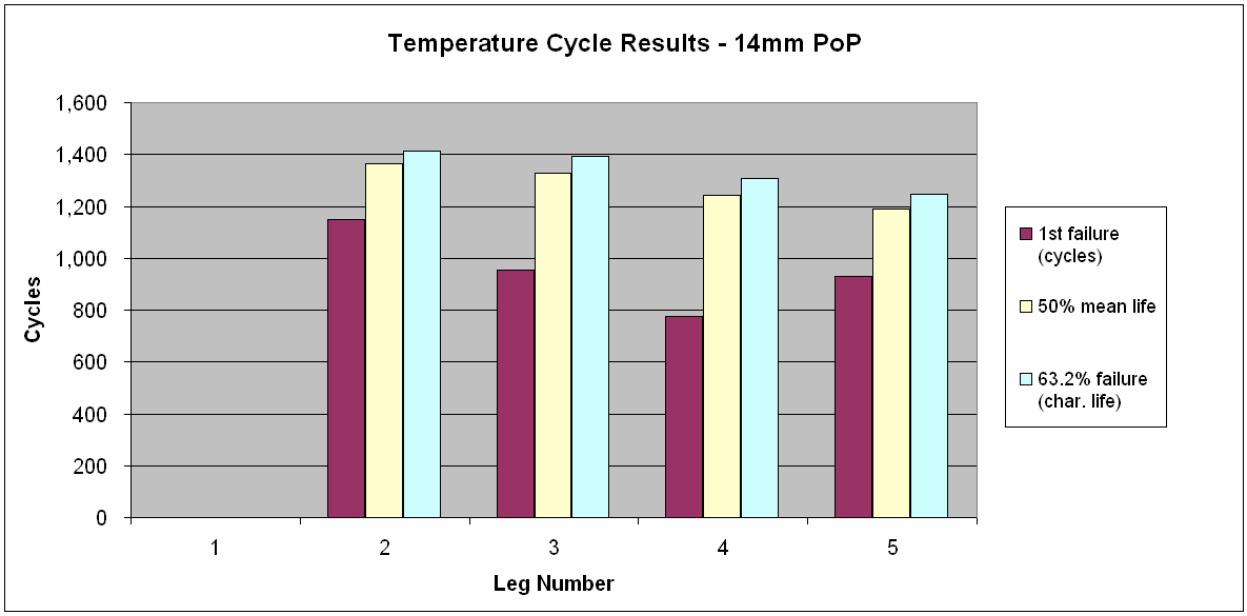
The temp cycle test results are shown in Table 5 and Figure 7. These results are reported after 1900 cycles. As expected the leg with NiAu interface (Leg 1, with no failures) showed better TC results than those with CuOSP (Legs 2-5). Since Leg 1 showed no failures at 1900 cycles, and since the top side nets (ii and iii) are monitored through the bottom BGA, it may be inferred that all of the TC failures are at the CuOSP interfaces C and D (refer to Table 1). This is being evaluated in the FA work.

However, a balance must be struck with the improved drop test results obtained with CuOSP as shown previously, since leg 5 does pass market temp cycling requirements for handheld applications.

Table 5. Temperature Cycle test results

	14mm Temperature Cycle Results					
	Leg #s	1	2	3	4	5
First Fail (50% mean life)	Minimum	0	1149 (1364)	954 (1329)	777 (1242)	928 (1191)
	Bottom net (i)	0	1221 (1485)	954 (1511)	1025 (1370)	993 (1349)
	Top middle (ii)	0	1149 (1509)	1253 (1449)	1060 (1406)	975 (1305)
	Top corner (iii)	0	1183 (1494)	1165 (1410)	777 (1416)	928 (1388)

Figure7. Temperature Cycle test results



CONCLUSIONS

Based on the results of the drop and temperature cycle experiments, it can be deduced that a good overall combination of ball composition and surface finish that also keeps in focus parameters for mass production in no underfill applications are represented by legs 4 and 5. Since the bottom package is typically shipped with an exposed top pad interface B, legs 4 and 5 have an added advantage of avoiding oxidation risks on surface B which may occur with CuOSP finish (as with legs 2 and 3).

Further study is planned for top packages with a CuOSP finish at interface A and LFA3 balls. Stacked on bottom packages with CuOSP and NiAu finishes for top pad interface B.

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