Pin in paste stencil design for notebook mainboard

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This paper examines the construction of a notebook mainboard with more than 2000 components and no wave soldering required.

The board contains standard SMD, chipset BGAs, connectors, through hole components and odd forms placed using full automation and soldered after two reflow cycles under critical process parameters. However, state of the art technology does not help if the process parameters are not set carefully. Can all complex BGAs, THTs and even screws be soldered on a single stencil? What will help us overcome bridging, insufficient solder and thombstoning issues?

This paper will demonstrate the placement of all odd shape components using pin-in-paste stencil design and full completion of the motherboard after two reflow cycles.

Keywords: Screen Printing, Stencil, Multilayer, Fine Pitch, Electroform

Everyday laptops we use are a little bit more than a keyboard and an LCD screen. If we take our time to take a look under the hood, we'll find a complex notebook mainboard together with many additional components. Less space, more functionality is what a laptop stands for, and a notebook mainboard is probably one of the most dense, compact and complex electronic assemblies in use today.

Traditional SMT process calls for screen printing, component placement and reflow phases, respectively for each side. The exception would be adding THTs and processing them together with SMDs in a single operation. However, when we go deeper into the process, we see it is not that simple.

As the surface mount components get smaller, and the component density increases as a result, soldering becomes a challenging task. Soldered joints are not always accessible for some components like QFNs and BGAs, since they are covered by the component body itself. These SMDs for sure require extra care, but what if we like to solder all THTs on a single pass together with them?

A notebook mainboard is a 1,2 mm thick 6 to 8 layer board with more than 2000 components on it. Our aim is to complete the soldering process after two reflow cycles and send the board immediately to ICT. In order to make this happen, first we should define all process parameters. On the first pass we will have only SMDs in place, but on the second pass THTs will come into stage.

In this article, we focus on the bottom side stencil and will define the stencil construction and aperture design requirements. There are strict procedures that govern the manufacture of stencils in any SMT production environment but I will try to keep our vision as wide as possible.

If we consider a seamless placement process where no placement issues are apparent–

- All SMDs are placed with high accuracy.
- THT devices are either manually placed of placed in automation with required accuracy and pressure. (In Vestel Digital all devices are placed in automation by the help of special nozzles and gripper arms.)

–then the key parameters left will be stencil design and reflow profile.

Pin in hole reflow technique

How to incorporate through hole components into the reflow soldering process? This question is the rally point for a simple to understand but hard to follow task. The pin in hole or pin in paste method lets the PCB go through the reflow oven once it is completely placed and, as a result, everything becomes 'soldered' right after the oven. In this process, paste is applied to all SMD pads, and holes are filled with solder for THT components.The difference from the SMD screen printing process is that the amount of solder pushed into the holes is more than the amount applied for regular pads–overprinting.

Multilayer stencil requirement

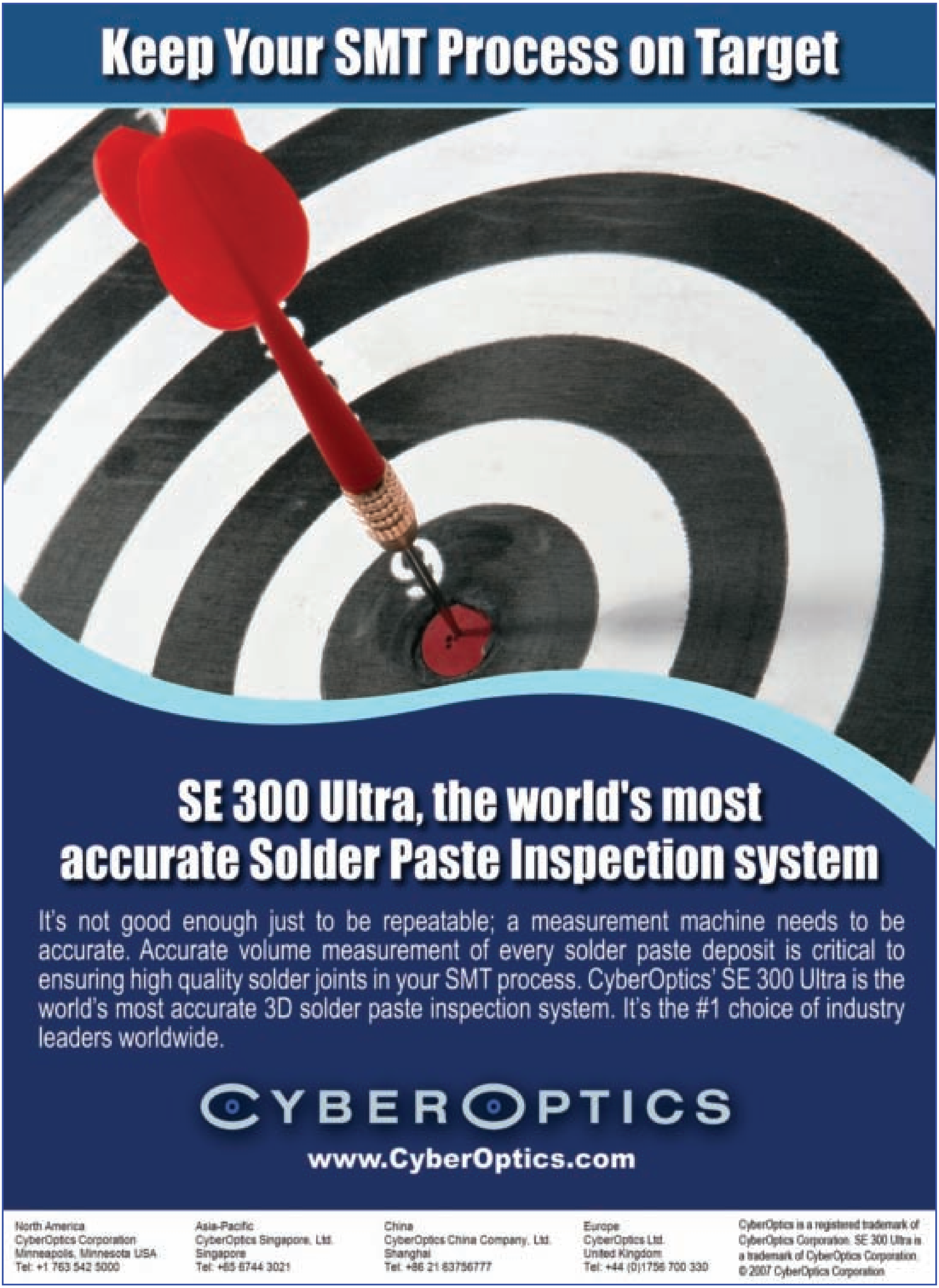
Consistent stencil design requires a clear definition of aperture parameters for each and every special component. Special components are the ones that need to be validated when a new process parameter is conducted or modified. On a typical notebook mainboard, 0.8 mm pitch and 1,27 mm pitch BGAs, 0.4 mm fine pitch QFPs, 0.5 pitch QFNs, 0.5 pitch connectors and all leaded peripherals–the so called THTs–sit on the same surface. Since our aim is to solder them all on a single pass, we will exercise extra care on each of them in order to optimize the stencil design for a repeatable process.

Let us consider the bottom side of a notebook mainboard and identify the stencil design parameters for each special SMD.

Chipset BGA

Ball Pitch : 0.8 mm
Ball Diameter : 0.358 mm

Rule 1: The ratio of the round aperture's surface area divided by the surface area of the side walls of the hole should be greater



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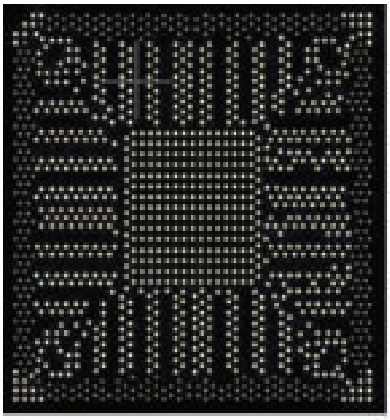
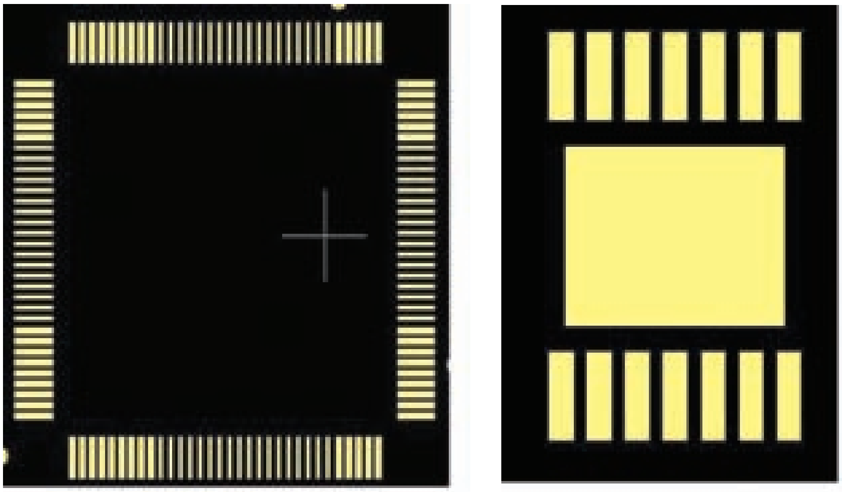


Figure 1. Chipset BGA with an 0.8 mm ball pitch and 0.358 mm ball diameter.



Figures 3a and 3b. A fine pitch QFP with 0.4 mm lead pitch and a small outline package.

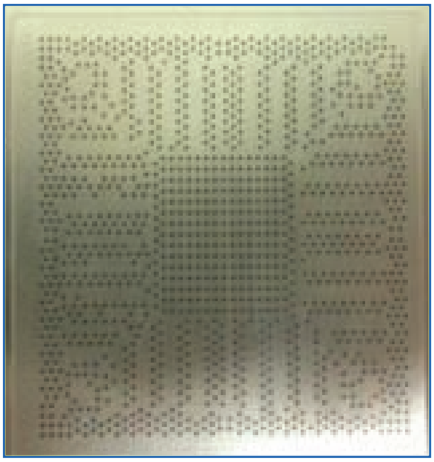
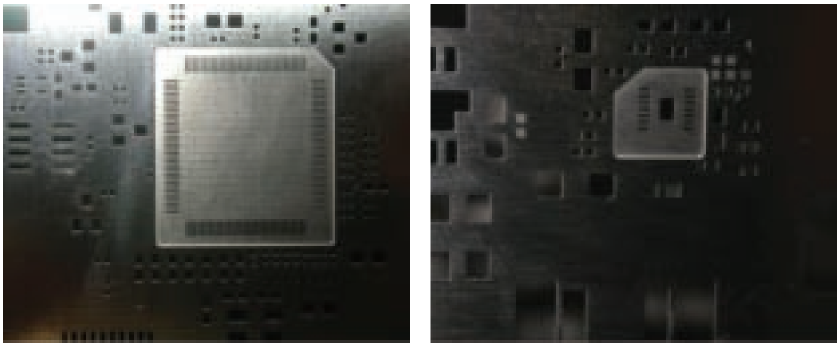


Figure 2. Chipset BGA stepped down to 125 microns (5 mils)



Figures 4a and 4b. A stepped down fine pitch connector (pitch : 0.5 mm) and stepped down small outline package.

than 0.66. If $D^2/4DT>0.66$, then Rule 1 is satisfied.

By applying this formula we get an optimum stencil thickness of 125 microns (5 mils).

Fine pitch QFP and 0.4 fine pitch smalloutline package

Lead Pitch : 0.4 mm
Lead width : 0.2 mm

Square aperture Rule 1: Aperature width and length divided by stencil thickness should give a ratio greater than 1,5. W/T andL/T must each be greater than 1,5.

Square aperture Rule 2: Aperture area divided by surface area of interior side walls of the aperture LxW/[2x(L+W)xT]–the ratio should be greater than 0.66.

According to the calculations for a 0.4 fine pitch QFP and SO, optimum stencil thickness will be 100 microns (4 mils), since for electroform stencils 125 microns (5 mils) is also acceptable and gives better results if apertures will have trapezoidal openings and are electro-polished for improved solder paste release to PCB pads.

Fine pitch connectors (pitch : 0.5 mm) Rules 1 and 2 apply. 125 microns (5 mils) stencil thickness is recommended.

THT devices

THT components are robust and reliable in placement process. Once they are placed a misalignment issue is rarely evident; however, they have a strong tendency to resist heat transfer in the reflow oven.This puts us at risk of having insufficient solder in holes after reflow. Solder balls are likely to complete their run in the hole before the reflow cycle ends, but what if not? The lead hole will not be filled with solder as expected. Then a few questions pop up:

- Insufficient solder?
- Reflow profile?
- Pcb hole design?
- Environmental conditions?
- More questions

Since our topic is limited to stencil design, we will only try to answer the first question. Solder paste will flow inside the hole when it becomes liquid somewhere around 200°C. A brick of solder must be applied over the hole entrance. The amount of solder we need to apply to the hole, most of the time by overprinting the pad, is calculated as in *Equation 1*.

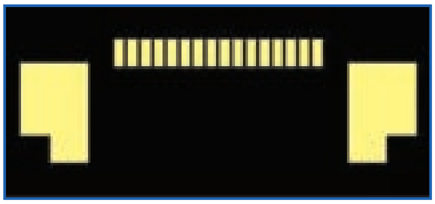


Figure 5. 0.5 mm fine pitch connector

Solder paste volume is two times the difference between hole volume and lead volume. We differentiate between the volume before and after reflow since solder paste is %50 metal by weight and almost

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$$\text{Volume of Solder Paste} = 2 \times \left(\pi \frac{D_{Hole}^2 - D_{Lead}^2}{4} h \right)$$

Equation 1

half of it shrinks. The multiplier '2' is the shrinkage factor and compensates for any shrinkage of solder paste.

According to IPC A 610 D , a %75 filling level for solder paste is acceptable.

Inserting leaded components in a solder filled hole requires fine tuning for THT aperture parameters. The amount of solder is calculated in *Equation 1* should be used to define volume requirements for the solder brick. Since we are printing over the hole, some amount of solder will be pushed into the hole by squeegee pressure. This amount is neglected in volume calculations although it is beneficial. The angle of squegee blade is a factor that defines the amount of solder trapped in the hole after printing. The solder volume to be printed can be extended in two dimensions–length and width of the aperture–since height is mainly defined by stencil thickness.

Process parameters like printing pressure and speed, separation distance and separation speed affect the overall printing quality, and deviating from this will cause introduction of unknown and multiple factors that will be challenging to solve due to the number of variables induced as a result of deviating from optimal flow. THTs must be considered as unique elements and be worked out seperately.

Let us define the overall stencil thickness by taking various component types into consideration.We have a 358 mm BGA with 0.8 mm pitch, 0.5 mm pine pitch connectors that require 125 micron (5 mils) thickness, a 0.4 mm fine pitch QFP that requires 100 microns (4 mils) thickness and finally THT components that require a stencil as thick as possible in order to form thinner and higher solder bricks.

The limitation is that we are not in a position to allow more than 50 microns difference between two layers of the stencil. On a multilayer stencil this will have a negative impact on the process since residual paste left on sharp corners of stepped down areas will tend to harden over time. Another concern is that stepped down components will feel the disadvantage of high corners by receiving more paste around corners. It is crucial also to have some control over edge corners, since sharp edges are not preferred in any process.

Overall thickness of the stencil will be

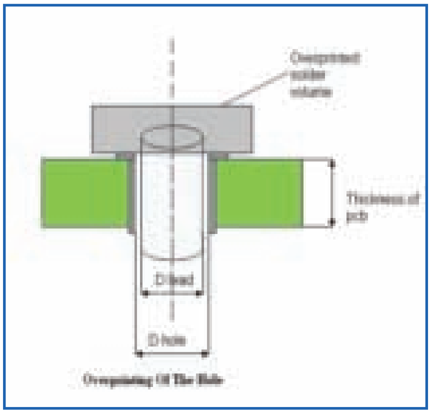


Figure 6. Overprinting for the hole.

150 microns (6 mils) and the maximum layer thickness difference will be kept around 50 microns (2 mils) to maintain a consistent and repeatable process.

Overprinting

We have determined a constant stencil thickness for THTs – 150 microns (6 mils)–and our intention is to expand the area of the aperture in order to meet the volume requirement for leaded components.

THTs leads–in line formation –up to 2 rows

These components have room for expansion in two directions. The aperture can be stretched opposite directions in order to increase the printing area, consequently the volume.

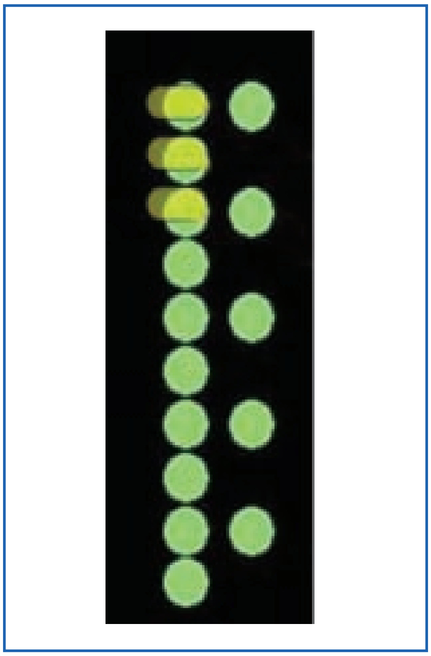


Figure 7. Recommended shape for increasing the printing area

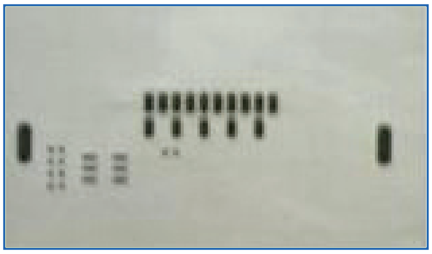
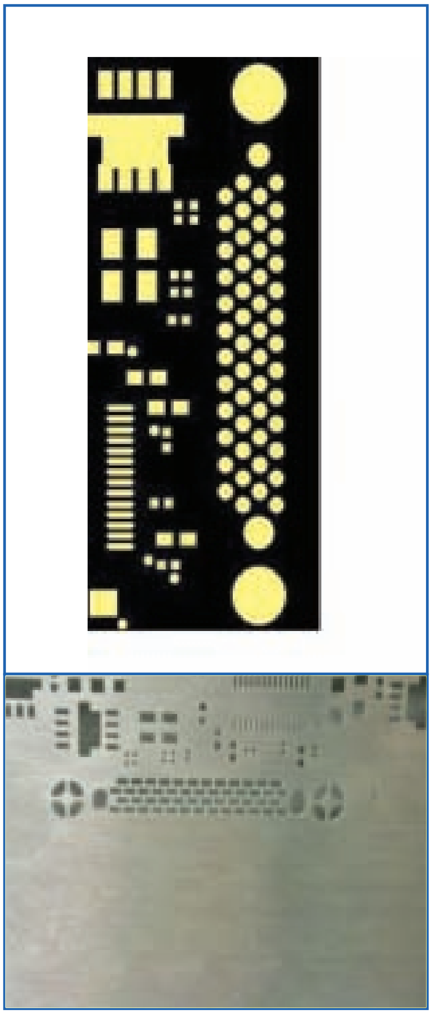


Figure 8. Typical application of a pad modification to a VGA connector

THTs leads–inline formation – more than 2 rows

The ODD connector has four rows adjacent to each other, and there is almost no room for expansion except the exterior rows. The solution is to modify the aperture shape to square.

If more solder paste is required on a square shape and there is a limitation for space, process solution will be finding ways of pushing more solder into the holes most probably by adapting an inclined squegee blade to the process. Continued on page 39



Figures 9a and 9b. THTs with a four-row lead formation. Figure 9b shows square aperatures.

difficult designs. During normal automatic dispense programs, a dot may be placed between two terminations that always short, and it only takes a few seconds to put into a glue program.

It makes a nice change to see glue solving rather than causing problems, but remember that there are many good products in the industry, so work with suppliers. When you have selected your adhesive, control the application process so it does not become a problem in your factory.

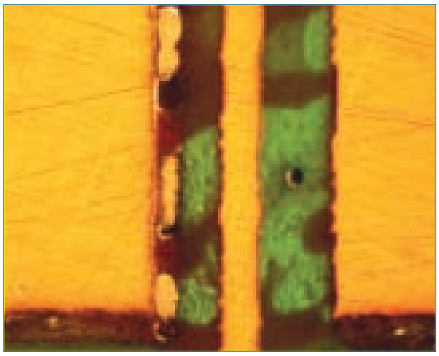


Figure 4. Microsection through the board under chip component. This shows the pads, adhesive and the solder shorting between the two pads and the track between pads. Root cause: the curing process.

Bob Willis is a process engineer working in the electronics industry, providing training, consultancy and process failure analysis on site for companies. Bob offers on site workshops world wide. He will be running lead-free workshops for IPC and SMTA in the US this year. For further information on lead-free training workshops, training materials and lead-free process support visit www.ASKbobwillis.com

Alstom Transport Information Solutions.

Vectron International received Core Partnership award from Huawei Technologies.

Vishay received the Active Component Manufacturer of the Year and the Interconnect, Passive, and Electromechanical Component Manufacturer of the Year awards from NEDA.

Walt Custer is an independent consultant who monitors and offers a daily news service and market reports on the PCB and assembly automation and semiconductor industries. He can be contacted at: walt@custerconsulting.com or visit www.custerconsulting.com

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TDK developed a new embedded chip process for both semiconductors and passive components which has a total thickness is only 0.3 mm.

Teledyne acquired:

- cable and interconnect manufacturer and assembler Storm Products.
- infrared product designer and manufacturer Judson Technologies.
- Nextest Systems Corporation.

Tyco Electronics is closing its Hillington, UK, factory in March, 2008.

Valor:

- and Digitaltest GmbH established a technology partnership to deliver best-in-class NPI solutions for assembly and test.
- design for manufacturability software was selected by Sercomm Taiwan and

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Conclusion

Stencil technologies available today offer a wide range of choices in determining aperture designs. If pin in hole reflow process requirements are met for a particular board–component material temperature withstand capability, limited component lead protrusions, pcb hole tolerances, placement accuracy requirements, etc.–then another factor to consider will be stencil design improvements that are essential to tailor the process needs.

Notebook mainboard screen printing processes require multilevel stencils for pin in hole reflow, since the assembly contains various odd shape and SMD components to be soldered together with THTs. Nickel electroform stencils give the best results when compared to laser cut stencils, since they are free of rough edges and aperture tolerances can be kept around + 0.0005.

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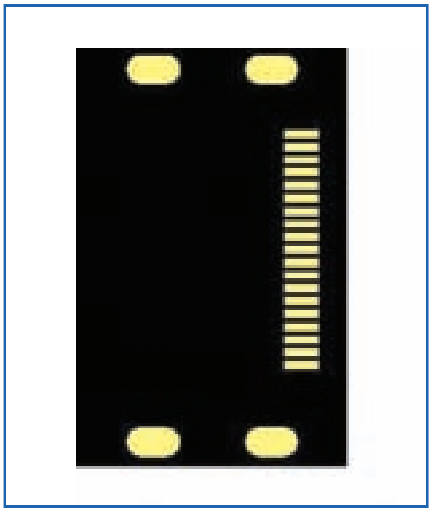

Figure 10. THT connector with SMD leads.