White Paper by Subrat Prajapati

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Design Guidelines for Stencil Design using Regression.

***Abstract*- The complexity of Printed Circuit Assembly process is increasing day by day and causing productivity issues in the industry, introducing ultra fine pitch components (pitch less than 15mil) in PCA is a challenge to minimize risk of defects as solder short, dry solder. This paper is focusing on minimizing these defects.**

To optimize process to reduce these defects, major contribution is from screen-printing process where stencil design plays major role if considered other screen-printing parameters are optimized, on which this paper is focused on. During the initial Stage of Stencil design it is imperative to arrest these problems. Design of Stencil should comply with "IPC-7525A: Stencil Design Guidelines". This paper is set on guidelines to minimize the process complexities and issues in production using above standard.

I. INTRODUCTION

Industries are focusing on reducing the overhead cost where in-house soldering defects and rework cost in surface mount device (SMD) assembly plays a major contribution. Goal is to address the solder short, dry solder joint defects from the initial stage of pilot lot planned to achieve required yield in production lot.

Root cause of these defects are mainly attributed to Screen Printing Process mainly categorized in following Processes-

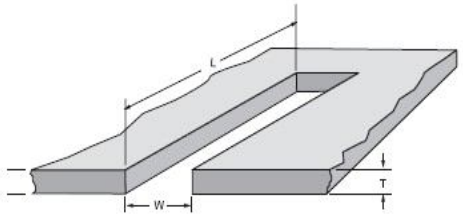
- Stencil Design
  - *A.* Stencil Thickness
  - *B.* Stencil Aperture Width/Length
- Solder Paste Thickness

As technologies changes, Electronics manufacturing services (EMS) is bound to shift to ultra fine pitch Integrated Circuit (IC) assembly having pitch less than or equal to 15 mil, in this scenario it's become critical that stencil design should give us first time pass PCA after reflow machine & to minimize stencil revisions.
IPC-7525A standard calls for stencil design, which is converted here in easier way to know how accurately we should get right stencil fabricated first time.

B. Knowledge Intensification

As stated in IPC-7525, Stencil aperture design should be reduced aperture with respect to PCB pad size in order to avoid excess solder paste deposition on Pads and leading to solder short issues. Due to excess paste deposition, operator will remove solder shorts that may create dry solder joints especially in component of pitch below15mil.

The three parameters of Stencil Aperture are Stencil Thickness (T), Aperture Width (W) and Aperture Length (L) as below Pic.



Taking IPC-7525A as base for Stencil Design, divide SMD component in categories as follows-
1st: Leaded SMD (J-leaded, Gull-wing, resistor array, smd Connector): Referred in IPC7525: 3.2.2.1,
2nd: QFP devices: Referred in IPC7525: Table-1,

As Length and Width of Aperture is dependent on Pitch of component, design of Aperture should be made as per Linear ***Regression equation*** derived from IPC7525A, which gives the user freedom to easily calculate stencil Aperture opening and required stencil thickness.
A Linear Regression equation is expressed as **y = mx + c**, where y is dependent variable, x is independent variable, m is the slope of regression line and c is intercept point of regression line and y-axis.It has been used to derive IPC-7525A given range of component pitch taken as 'x' variable and Aperture opening as 'y' variable.
Applicable for Leaded SMD (Pitch=15.7-51.2 mil): Ref.IPC7525: 3.2.2.1 states "For leaded SMD with 51.2-15.7 mil pitch, the reduction is typically 1.2-3.1 mil in width and 2.0-5.1 mil in length", derived as per below regression equation –

Aperture Width Reduction = 0.360 + 0.0535 * Pitch of Component
Aperture Length Reduction = 0.6294 + 0.0873 * Pitch of Component

Applicable for QFP: Ref.IPC7525: Table-1 states " Pitch from 11.8-25.6 mil, aperture Width should be from 5.91-11.8 mil & aperture length should be from 37.4-57.1 mil derived as per below regression equation –

Aperture Width = 0.8736 + 0.4268 * Pitch of Component
Aperture Length = 20.5551 + 1.4275 * Pitch of Component

Stencil thickness desirable need to be derived from below equation, which is common for all type of SMD components-

Stencil Thickness = 2.64 + 0.0831 * Pitch of component

Keeping below conditions to be met so as not to get undesirable solder paste volume on pad & maintain good transfer efficiency-

Aspect Ratio = Width of stencil aperture/Thickness of stencil (W/T) >1.5
Area ratio = Area of aperture opening/ Area of aperture walls (L*W)/2*(L+W)*T >0.66

Above equation has arrived with R-Sq = 100.0%, where R-Sq values represent the proportion of variation in the response data explained by the predictors (the independent variable that is used to predict values of the dependent, or response, variable in a regression analysis).

While calculating stencil thickness stencil calculated thickness should be averaged out from all list of IC on board to get one value of stencil thickness applicable for all components on PCB.

If the stencil thickness comes with minimum to maximum difference more than 2mil, call should be taken to step-up, step-down type stencil with stencil manufacturer.

One should ensure the paste thickness on PCB after screen-printing should be as per below specification-

Paste Thickness on PCB = Stencil Thickness + 1.5/-0.5mil
(Specification made for 5mil stencil thickness)

If components are less than 15 mil pitch, one should seek to deploy type-4 solder paste having granule size of 20-38 µm than using type-3 having granule size of 25-45 µm.

C. Implementation Result:

Derived Regression equation has been implemented in new Stencil and run on line with all other process variables constant/monitoring phase for 150 number of PCA.
It has clocked DPMO of 6510 from 22000
(Opportunity of defects =999, considered 58 number of IC, resistor arrays and SMD connectors taking 2 pin as one opportunity of defect).

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