Method for Automated Nondestructive Analysis of Flip Chip Underfill

Steven R. Martell, Ameya Mandlik and Kieren Mercer
Sonoscan, Inc.
2149 E. Pratt Blvd.
Elk Grove Village, IL 60007
T: 847.437.6400

Abstract
For many years Acoustic Micro Imaging (AMI) techniques have been utilized to evaluate the quality of the underfill used to support the solder bump interconnections of Flip Chip type devices. AMI has been established as one of the few techniques that can provide reliability and quality control data, but little has been done to automate the evaluation process for Flip Chip underfill until now.

An automated analysis method has been developed and tested on a variety of Flip Chip structures that provides more consistent and accurate analysis than manual, visual examination by operators. The automated analysis provides unbiased, repeatable evaluation data for part-to-part and lot-to-lot comparisons to ensure that the process is within its control limits, providing a more reliable product.

This new method of analysis incorporates techniques that provide data on how well individual solder bumps are being supported by the underfill or an overall percentage void measurement, depending on the level of detail required for the process. The analysis functions also have built-in capabilities to automatically account for process variations.

Example acoustic microscope images and automated data analysis results for a set of Flip Chip devices will be presented to help explain the methods utilized to obtain consistent and accurate information for process evaluation.

Keywords
Acoustic Microscope, Acoustic Micro Imaging, AMI, Flip Chip, underfill, automated analysis, quality assurance and reliability.

Introduction
Acoustic imaging techniques have been an accepted nondestructive method for evaluating the attachment between a die and a substrate with either eutectic, solder or organic adhesives since the establishment of MIL-STD-883, Method 2030. [1] Simple criteria were established within Method 2030 to provide accept/reject guidance of typical die attach applications for military use. The criteria were established to provide adequate reliability of the die attachment strength for rigorous military and aerospace applications. As shown in Figure 1, the criteria were very basic since the image analysis power and techniques were rather limited, so a simple percentage of area or visual analysis of the ultrasonic/acoustic images was relied upon at that time.

The die attach area was evaluated in two ways: as a single region and divided into four (4) quadrants. In the case of the single region, any single void larger than 15% or a corner void greater than 10% of the total area were grounds for rejection. If the die attach passed these criteria, then it was divided into four quadrants for further evaluation. It was rejected if any of the quadrants was not bonded more than 70%. These criteria were fairly easy to calculate with simple image processing techniques or visual measurement and calculations, if needed.

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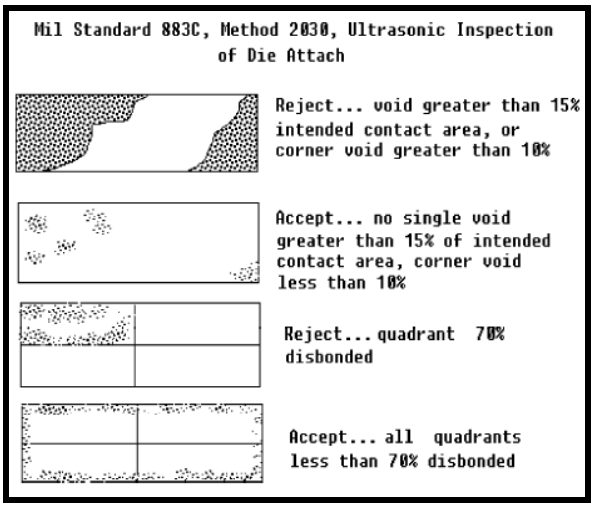

Figure 1: Accept and reject criteria from MIL-STD-883, Method 2030, for die attach.

While a die attach is a simple structure consisting of a die, adhesive material and substrate, a Flip Chip device adds several levels of complication. The die is flipped over, with the active side facing the underfill material, and all of the interconnections between the die and the substrate are dispersed throughout the underfill. Based on industry standards and guidelines, there are reliability issues associated with a lack of bond at the active side of the die and the underfill and voids in the underfill next to solder bump interconnects.[2,3,4,5] A small isolated void in the underfill material is not a reliability issue, as shown in Figure 2.

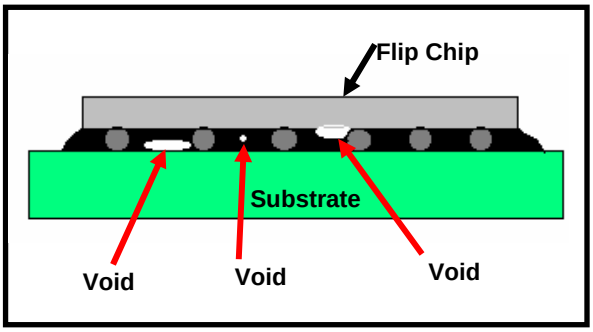

Figure 2: Typical types and location of voids in the underfill material of a Flip Chip device. The small isolated void, as shown in the center, is not a reliability issue. Voids located at the interfaces or close to a solder interconnection can be a reliability issue.

In the case of the void/delamination at the active side of the die to underfill interface, it is fairly simple to obtain an acoustic image at that interface to look for any delaminations or voids. This interface image will also include the die to solder bump interface, which is of interest for reliability analysis, also. Therefore, a simple percentage measurement of voids within a region could be used, if the criteria are the same, such as no void/delamination allowed at that interface. However, any percentage (%) area criteria greater than the region of a single solder bump interconnection would be an issue. The acceptance criteria would have to limit a single void area to an area smaller than a single solder bump area.

Voids within the underfill and voids/delaminations at the underfill to substrate interface have no standard accept/reject criteria to reference for the analysis. In addition, the criteria can be based on the application use and/or level of reliability required. The main concern for reliability has been unsupported solder bump interconnections. This is due to the fact that solder can creep into the cavity within the underfill material, when located adjacent to the solder interconnection, causing an open connection and leading to the failure of the device.

Adding to the problem is the complexity of the interconnections layout for the Flip Chip device. Older forms of Flip Chips had a uniformly spaced, grid like pattern for the interconnections. Newer types of Flip Chip devices have much more complicated interconnection layouts that include multiple regions of various grid patterns and transition zones. This level of complexity also complicates the visual and traditional percentage of region analysis techniques to the point where manual analysis becomes very inaccurate and non-repeatable on a statistical basis. Therefore, there is a need for a more sophisticated and robust method for evaluating Flip Chip underfill for critical defects with an automated analysis method.

Discussion on Methodology Used

Statistically speaking, a percentage void calculation could be used if the same type of Flip Chip device was being evaluated on a regular basis and a correlation between the percentage of void and reliability data was done with satisfactory results.

Unfortunately, this cannot be typically done for most products going through rapid process development or it is just too costly to do for every variation of the device being manufactured. Therefore, ground rules need to be developed based on what is considered to be acceptable and rejectable defects based on failure analysis and computer modeling results. The challenge was to develop a method that can screen devices based on these ground rules with accurate and repeatable results even when there are process variations.

The basic methodology divides the underfill region into "cells" that are defined by the position of four (4) solder interconnect locations, see Figure 3. Each cell is sub-divided by the chosen AMI scan resolution into a number of pixels per cell. A cell is considered "good" or "bad" based on a percentage of pixels with a void within a cell, such as 50%. The number is user selectable to any percentage preferred for that device design and application use.

Upon determining if a cell is bad or good, the total number of bad cells can be counted to provide data for accepting or rejecting the whole Flip Chip device. In addition, since the support of a solder interconnection is very important, the cells surrounding a solder interconnection are evaluated to determine if it is supported on all four (4) sides, completely enclosed, or if one or more of the cells are bad. A Flip Chip device can then be rejected if 1, 2, 3 or 4 of the surrounding cells are bad, depending on the level of reliability desired.

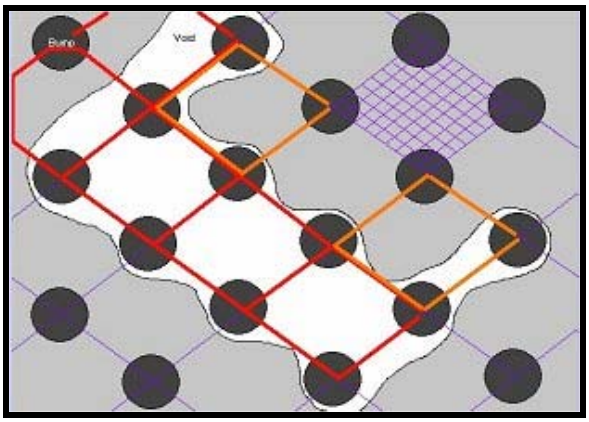

Figure 3: A "cell" is outlined by four (4) solder interconnections and sub-divided into pixels of data. The red lines outline bad cells, the orange lines for possibly bad cells and the purple lines for good cells.

This methodology works well for a uniform grid pattern of solder interconnections, but cannot be utilized directly when different interconnection patterns or vacant areas are used over the region of the Flip Chip device. To adjust for this, the total region can be divided into sub-regions with the same grid pattern, as shown for the device in Figure 4. Within each sub-region the interconnection pattern can be treated the same to obtain consistent automated image analysis.

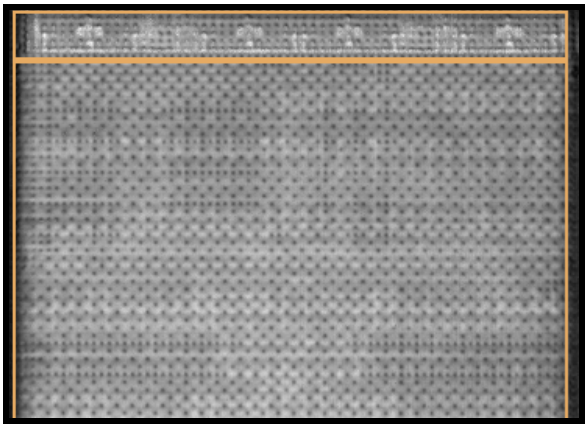

Figure 4: The upper half of a Flip Chip device that has been divided into two visible sub-regions, as indicted by the orange boxes. A third sub-region along the bottom edge is not shown here.

Within each of these regions the interconnection pattern is automatically located by the software to form the cell network that will be utilized for the analysis. The analysis for each device is done on a sub-region and total region basis to help identify assembly process issues associated with a particular sub-region due to underfill dispense, flow, outgassing, etc.

A recipe for the analysis of a particular device type can be stored and recalled for the consistent analysis of each device imaged with AMI today, tomorrow or at a much later date. These recipes can be locked by an administrator so that an operator level technician cannot modify the recipe or results during the analysis of a batch of devices.

Even with the recipe locked, there will be some part-to-part variation and image analysis issues that will distort the data if they are not accounted for during the automated analysis of the acoustic images obtained for each device.

One such issue is the level of the acoustic image brightness that may change due to the underfill material density, distribution of filler particles or other batch-to-batch variations. Over the full range of image brightness levels, the very bright images could be rejected even if no defects are present and very dark images could be accepted even if they contain defects when the automated analysis function is just setup for an average brightness level. To compensate for this a dynamic threshold function was developed. This function automatically adjusts the threshold range based on the brightness variations that may occur from device to device.

Results and Data Obtained

A set of four (4) Flip Chip devices were provided for this paper that had not been previously examined with the automated analysis function, but had been acoustically imaged. Two of the devices were known to have voids in the underfill and two were void free.

All four parts were scanned by Sonoscan's applications lab to obtain the typical type of acoustic images used for evaluating the underfill for voids and delaminations at the die or substrate interfaces. Figure 5 shows the acoustic images of the four devices scanned. Looking closely, you will notice that there is some variation in the overall level of brightness between one device and another. There is also a difference in the interconnection pattern along the top and bottom edges of the devices in comparison to the central region of the devices.

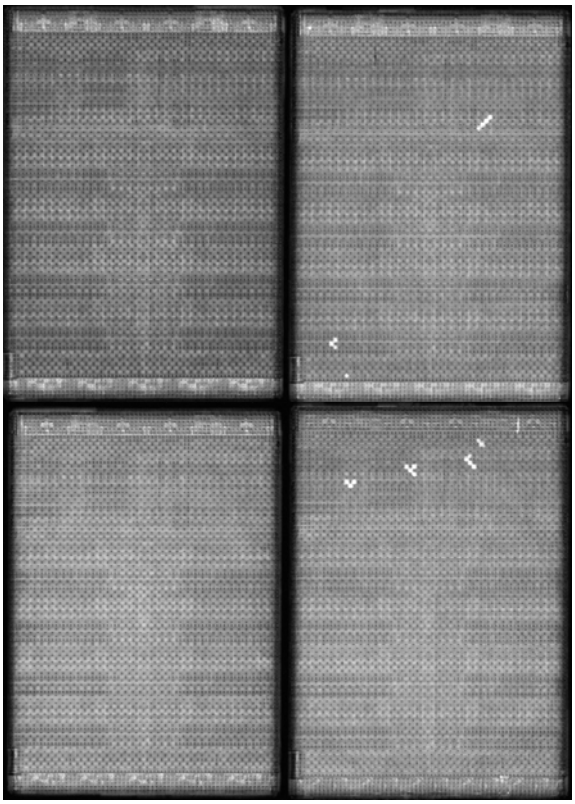

Figure 5: Acoustic images of the four Flip Chip devices prior to any automated analysis. Devices 1 and 3 (top & bottom left) appear fairly clean, but image 1 appears to be slightly darker than the others. Devices 2 and 4 (top & bottom right) both have voids in the underfill, indicated by the white areas.

The next step in the process was to determine the number of sub-regions needed per device image. As previously mentioned and shown in Figure 4, the top and bottom edges show a different interconnect pattern than the central region of the device. Therefore the device was divided into three (3) sub-regions of interest, with the large central sub-region #1, the top #2 and the bottom edge #3.

The accept/reject criteria starts with establishing a threshold for the seed defects for each sub-region and/or a group of sub-regions that have the same dynamic range, such as sub-regions #2 and 3 for these devices. All the defect areas grow from these baseline defects to their maximum size without introducing any artifacts.

The criterion for a "bad" cell is selected next based on a maximum percentage of "bad" pixels within a cell. Normally, a percentage between 10% and 50% is chosen and is typically close to 20% for most applications for good reliability.

To count unsupported interconnections, called embedded bumps, the number of allowable "bad" adjacent cells is selected. Depending on the application, 1 to 4 "bad" cells could be selected, with 1 providing the highest reliability. Typically, 2 "bad" cells are chosen for normal applications.

With all of the analysis conditions selected and the recipe saved, the results of the automated analysis of the acoustic images were obtained and are provided in Figures 6 and 7, which show the analyzed images and analysis results, respectively.

Device 1 (upper left of Figure 6) had no "bad" cells or embedded bumps, indicating it is completely free of any underfill defects. For device 3 (lower left of Figure 6), it is also defect free in sub-regions 1 and 2, but there was a single "bad" cell in sub-region 3, which is the bottom region.

Both devices, 2 (upper right of Figure 6) and 4 (lower right), had two embedded bump interconnections each that were not adequately supported by the underfill. For device 2 there were 13 "bad" cells in sub-region 1 and the other was in sub-region 2, for a total of 14 "bad" cells. Device 4 had "bad" cells in all three sub-regions, with 17, 3 and 1 in sub-regions 1, 2 and 3, respectively.

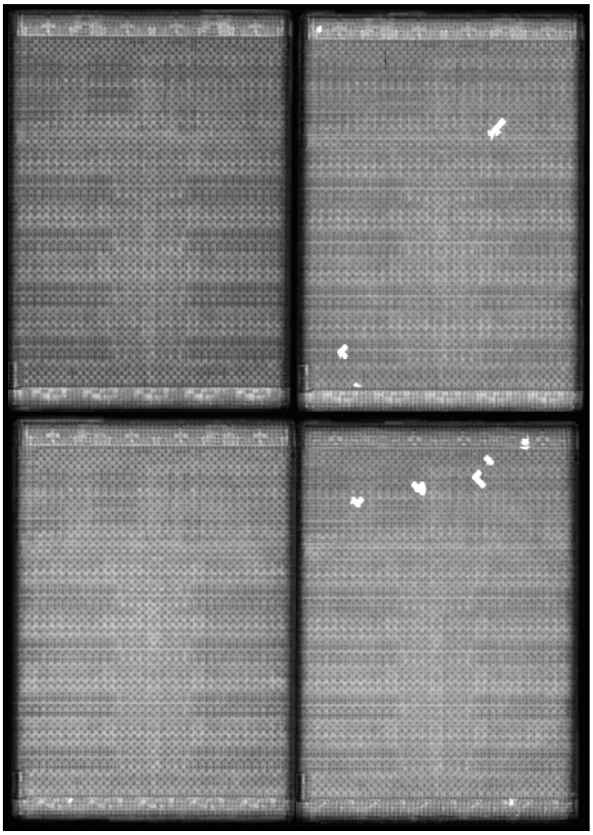

Figure 6: Cell analysis images for devices 1 to 4. Devices 2 and 4 have multiple bad cells, as indicated by the white areas in the images.

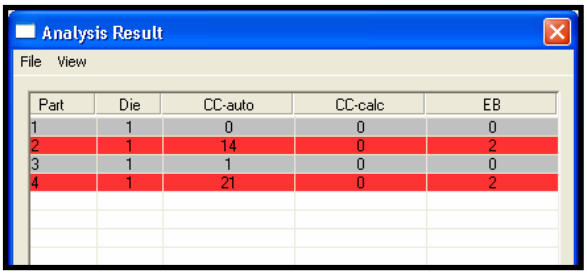

Figure 7: Final results for devices 1 to 4. Both devices 2 and 4 have 14 and 21 bad cells, respectively, and 2 embedded bumps each. The other devices have no embedded bumps.

Conclusions

This set of devices provides a simple example of how this new methodology can be used to identify Flip Chip devices that have a reliability risk due to inadequate underfill and/or underfill that failed to provide the required support to the interconnections, such solder bumps. This methodology also removes any analysis variance due to human error, turns the analysis into a quantitative from qualitative process and does it repetitively with repeatable results.

This same methodology can and has been applied to a single device with 9 or more sub-regions and two or more Flip Chips within a package. It has developed over the last two years into a robust and precise method for counting and categorizing underfill defects for a variety of Flip Chip type devices.

In comparison to total percent void measurements for an entire device this new method can distinguish between a small total void region that is a threat to reliability and a large total void region that does not have any reliability issues due to the pattern of the voids throughout the cells analyzed.

As shown in Figure 8, the analysis function does include percentage void, largest void diameter and largest void length results for each of the sub-regions per device. Using this data alone to accept or reject a device would be inadequate and unreliable.

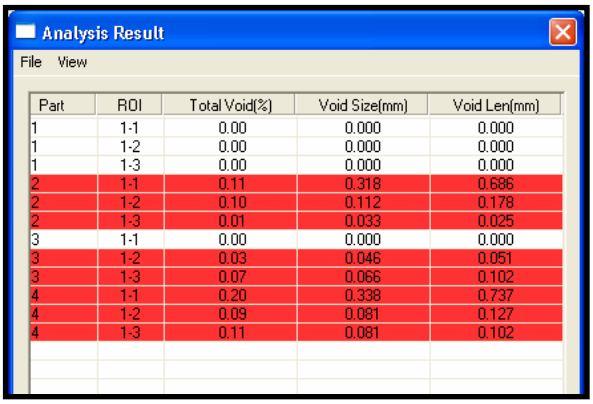

Figure 8: Percentage total void, void size and void length data given for each sub-region for each device.

Output from the analysis can be provided in several ways, but the most common is a digital data file format that allows traceability of each device and the analysis results. The digital file can be uploaded to the server for process and quality control review to ensure that the process is still within the control limits.

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[1] MIL-STD-883, Method 2030: Ultrasonic Inspection of Die Attach., GEIA Standard.
[2] J-STD-020: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices., Joint Industry Standard
[3] J-STD-030: Guideline for Selection and Application of Underfill Material for Flip Chip and Other Micropackages., Joint Industry Standard
[4] NASA/TP – 2003 – 212242; EEE-INST-002: Instructions for EEE Parts Selection, Screening, Qualification and Derating., NASA Standard
[5] NASA/TP – 2003 -212244; PEM-INST-001: Instructions for Plastic Encapsulated Microcircuit (PEM) Selection, Screening, and Qualification., NASA Standard