MECHANICAL FAILURES IN PB-FREE PROCESSING: EVALUATING THE EFFECT OF PAD CRATER DEFECTS ON PROCESS STRAIN LIMITS FOR BGA DEVICES

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ABSTRACT

The increased temperatures associated with Pb-free processes have produced significant challenges for PWB laminates. Newly developed laminates have different curing processes, are commonly filled with ceramic particles or micro-clays and can have higher T_g values. These changes which are aimed at improving the materials resistance to thermal excursions and maintaining electrical integrity through primary attach and rework operations have also had the effect of producing harder resin systems with lower fracture toughness.

Industry guidelines for mechanical stress limits were developed for materials processed using eutectic SnPb solders. A series of design and material implementations have gained wide acceptance by the industry to address mechanical failures at the corners of area array packages. Current accepted levels of process strain were established when the dominant and limiting failure mode was interfacial fracture (IFF) in complex intermetallic compound (IMC) layers at the solder / package interface. Changes in packaging processes, conversion to Lead (Pb) free solders and the subsequent compensation by laminate suppliers have produced significant shifts in failure mode occurrence and the "Pad-crater" failure mode has become far more common than IFF. By conducting a testing program that focuses on materials and geometries consistent with high complexity "Enterprise Computing and Telecomm" electronic assemblies, and evaluating the results against the current industry guidelines it is possible to determine whether the dominance of the "Pad-crater" defect mode will require revision of process strain guidelines. Test methods, test results, failure analysis and likely mitigation techniques are discussed.

Key words: Pad crater, spherical bend test, mechanical failure mode, process strain.

INTRODUCTION

The transition to lead free assembly of medium and low complexity products is essentially complete. Products designed for sale directly into the retail marketplace such as handsets, smart phones, gaming systems, PCs and Net books, are all routinely built with lead free solder alloys required to comply with widely enacted environmental legislation. The vast majority of these products are built with alloys in the Tin Copper (Sn-Cu) and Tin Silver Copper (Sn-Cu-Ag) alloy systems. There are a wide variety of choices available but the common impact is that the minimum solder joint temperature for proper re-melting of solder spheres and powders is in the 230 to 240C range. The industry struggled initially. While there have been some very extensive field failure issues related to material selection, in general the materials required for robust assemblies in these less critical reliability, high replacement rate product categories are now readily available. Proper analysis and material qualification and product design will result in "wear out" failure mechanisms and warranty exposures that are in line with those experienced with eutectic tin lead (SnPb) assembly processes.

Less is known about the mechanical robustness of lead free systems. Considerable effort has expended on drop shock improvements for handheld devices and there are a plethora of new additions to low silver alloys attempting to enhance the energy absorption of these alloys, but comparatively little work has been documented on mechanical failures of larger assemblies. Laminate suppliers have over time implemented changes to reduce the Z-axis expansion and raise decomposition temperatures to make their materials robust in extended thermal excursions. Unfortunately these implementations have had a detrimental effect on some mechanical properties of laminates, particularly toughness.

Roggerman et al.[1] and others have published "cold ball pull" and "hot pin pull" testing results which identify that filled phenolic cured FR4 epoxy laminate systems fail at lower loads and absorb less energy to failure than unfilled resins from the same group. These micro particle fillers have been introduced to reduce Z-axis expansion and are widely implemented. We believe that this category of resin system represents the limiting case for mechanical integrity.

Mechanical failures in BGA solder joint systems have been categorized into ten modes to simplify cross company discussion and acceptance of standardized testing. There is wide industry agreement that Mode 3, failure at the package NiP/SnNi IMC layer was the limiting case when current procedures were designed. There has been some movement in the industry to convert to Cu-Sn based interfaces at the package side and this has reduced the number of maverick lot incidents considerably. This change combined with conversion to lead free processing has produced a new dominant failure mode. Anecdotally mechanical failures in lead free systems are almost always reported as Mode 10, pad lift/pad crater unless some significant process defect is present in the solder.

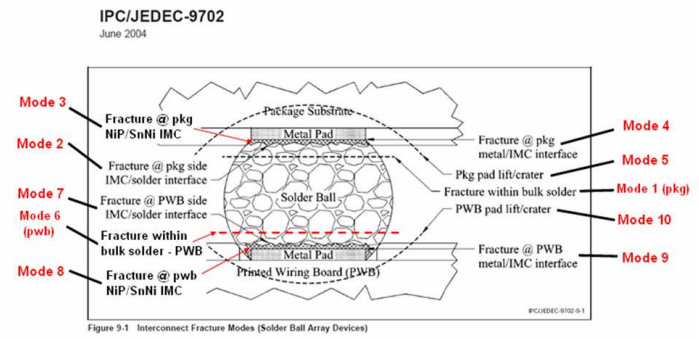

Figure 9-1 Interconnect Fracture Modes (Solder Ball Array Devices)

NOTE: SEM/EDX is required to distinguish between Failure Modes 2 & 3 as well as between Modes 7 & 8.

Figure 1: Failure modes in BGA solder joint systems [2]

However, the conversion to Lead free assembly is not complete, The challenges facing the electronics industry over the next few years are more formidable than those that have been recently overcome. With the expiry of the "lead in solder" exemption now targeted at 2014, Enterprise computing and Telecommunications equipment must convert to lead free assembly processes. These server room and backbone type products are designed to the maximum area that can be processed through standard SMT, wave solder and test equipment. Outline dimensions of 16 x 20 inches (40 x 50 cm) are typical. Current products typically have 20 to 30 Cu layers and thicknesses of 0.100 to 0.130 inches (2.5 to 3.5 mm) but certainly higher layer counts and thicknesses of 0.25 inches (6 mm) are on the roadmaps for these products. The high thermal mass associated with this type of assembly can drive a 5X to 10X increase in the heat energy requirements when compared to PC and consumer products. These increased energy requirements translate into longer thermal profiles and extended exposure times at high temperatures for all processing steps.

(ASICs) that usually exist as high I/O BGA packages. Power and I/O characteristics usually require that these are flip chip devices based on built up substrates with metal heat spreaders. The combination of thick laminate structure and large stiff package design almost certainly defines the maximum stress condition and therefore the lower boundary condition for mechanical integrity under flexure in high complexity assembly.

Thermal analysis of a typical high complexity product processed through standard 10 zone and 12 zone SMT ovens (Figure 1.) clearly indicates that proper reflow of large BGA devices on this type of product will expose the laminate to temperatures near the 260°C limit.

Evaluations intended to optimize process parameters and materials targeted for high complexity assembly must be performed on representative laminate stacks, package types and must be based on extended thermal profiles.

The intent of the current work is to validate that the current material sets defined for lead free solder processing can with stand equivalent mechanical stress excursions relative to those defined for Eutectic tin lead systems. This work will be conducted on test vehicles constructed and processed to be consistent with high complexity assembly.

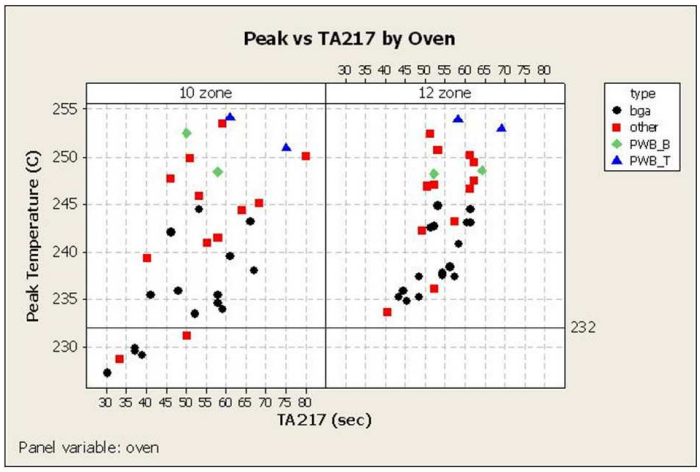

Figure 2: Thermal Analysis of High Complexity Reflow

EXPERIMENTAL DESIGN

The experiment was designed to assess the mechanical strain limits for lead free high complexity assembly and characterize the effect of lead free alloys and extended thermal requirements on safe working limits for board flexure in terms of peak strain and rising strain rate.

Surface strain analysis in PCBAs is the method by which we normalize a whole group of sub-parameters. Surface strain in uniform slabs is a function of deflection or curvature and board thickness (distance from the neutral axis of the slab). In electronic assembly it is complicated by non uniform reinforcement of the system by soldered components. Our interest is actually in the stress/strain concentrations that are inherent in the soldered connections. Specifically the stresses that are imposed on the solder, the interfaces of the solder joint and the resin systems that are directly in contact with the solder pads. In this work we have introduced two factors which are "designed" to generate variation in the results. These are board thickness and strain rate. The other three factors: sphere alloy, laminate and pad plating are under study. The expectation is that each combination of strain rate and board thickness will generate a separate distribution of failures. The experimental design is actually to produce six separate evaluations of the reduced factor list outlined in Table 1.

Factor	Levels
Sphere alloy	SnPb / SAC105 SAC305 / SAC405
Laminate	Standard Filled Phenolic / Toughened Filled Phenolic
Pad Plating	OSP / ENIG

Table 1: Material Factors

Strain Rate

The strain rate dependence of fracture in epoxy resin systems is well documented in basic materials research, and has been widely incorporated into existing industry specifications and guidelines, such as IPC/JEDEC-9702 - Monotonic Bend Characterization of Board-Level Interconnects[2] and IPC/JEDEC-9704 - Printed Wiring Board Strain Gage Test Publication [3]. A proper treatment of this topic is beyond the scope of the current paper, but testing for this experiment was targeted at three specific Principal Strain rates intended to cover the acceptable ranges of all major assembly processes. Those three targeted Principal strain rates are 1000, 3500, 7000 micro strain per second (με/s).

Materials

Eight sub-lot variations of a mechanical test vehicle were procured. Solderable surfaces were plated in both OSP and ENIG to generate interfaces based on both Cu6Sn5 IMC and Ni4Sn3 IMC systems. The PWBs were obtained in two laminates provided by Isola. The first was a standard filled phenolic cured FR4 and the second was a non-commercial variant of the first which had been modified to reduce room temperature Young's modulus by approximately 40% in an attempt to toughen the resin system.

Two versions of physical design were generated, each with identical footprints and outlines but with two distinct laminate stacks to represent incremental levels of assembly complexity. The first version was made up of 20 copper layers and had a nominal thickness of 0.100 inches (2.54 mm), the second contained 26 copper layers and had a nominal thickness of 0.130 inches (3.3 mm). The 185 x 185 mm test vehicles have a single BGA footprint for a 40 x 40 mm – 1.0 mm pitch device.

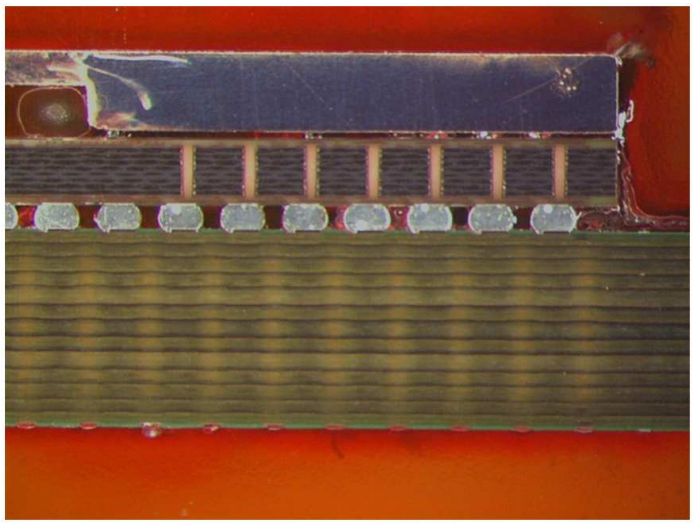

Figure 3: Package / board construction - 20 layer stack

The 40 mm 1517 I/O built up flip chip packages were daisy chain devices provided by LSI. The package substrates were all plated with SAC305 over copper before spheres of the various alloys were attached. The BGA spheres were provided in Sn37Pb, SAC105, SAC305 and SAC405.

SAMPLE PREPARATION

Thermal profiles were prepared for each of the sphere alloys in the testing program. The SnPb devices were attached with SnPb paste while all of the Lead free devices were processed with SAC387 paste. This induces minor modifications to all of the SAC alloys in the final solder joints but it is typical of production assembly.

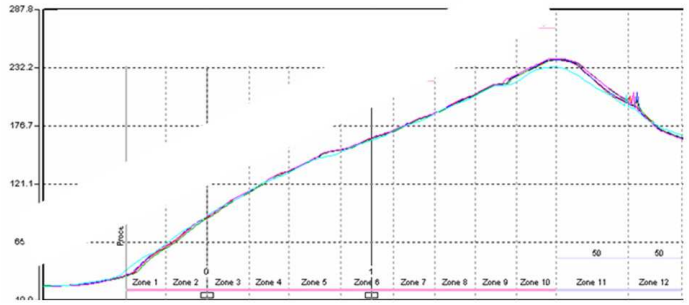

Figure 4: Typical SMT profile - 10 zone - SAC alloy

Assemblies were preconditioned by one pass through the SMT oven prior to BGA attachment to account for the fact that these large devices usually exist on the top side of double sided assemblies. Where forced rework was required assemblies were processed through two further hot gas cycles to simulate removal and replacement of the BGA device. Solder joints from these processes were properly formed with acceptable voiding and typical microstructure.

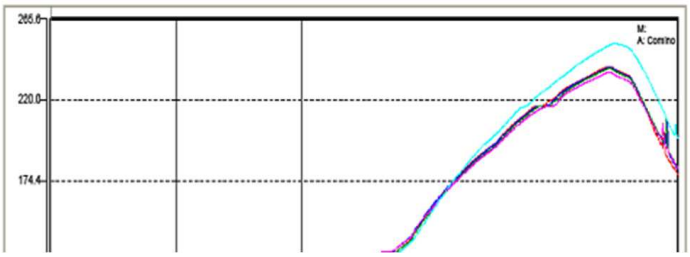

Figure 5: Typical Rework profile - SAC alloy

METTALURGY

XRF examination of the as received BGA devices with spheres attached indicates that silver levels are near the low end of the specification for all of the SAC alloy lots.

Element	Alloy	N	Mean (ppm)	SE
Ag	SAC105	50	8,411	64
	SAC305	50	25,458	80
	SAC405	50	36,374	95
	SnPb	50	491	41

Table 2: Silver content in attached solder spheres

Optical microscopy was performed on cross sections from all of the process lots. There were no remarkable results from primary attach. Solder conformation was normal, very little voiding was evident and the all of the standard phase compositions were measured. Packages are pre-plated with SAC305 directly over Cu so OSP boards produce Cu6Sn5 interfaces at both top and bottom interfaces. ENIG boards produce Cu6Sn5 at the top interface and a much more complicated Ni3Sn / Ni4Sn3 / (Cu-Ni)4Sn3 interface at the board side pad.

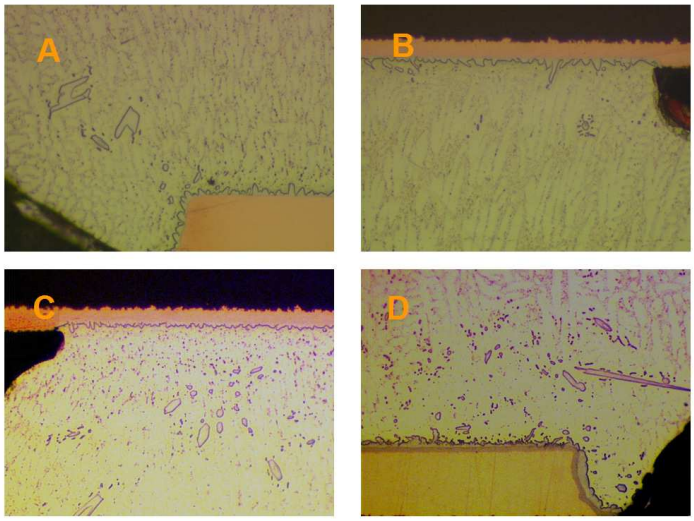

Figure 6: Forced Rework: A & B - OSP; C&D - ENIG

As expected, the extended thermal exposures generated by forced rework produce a fine dendritic network and distributions of primary Cu6Sn5 near the interfaces and thicker boundary IMC layers. There is significant consumption of the Cu pad on the package side. We also noted a significant portion of Cu containing IMC over the Ni layer at the board side of the ENIG assemblies.

FLEXURAL TEST BENDING MODE

Various flexural test bending modes have been employed in the electronics industry. IPC-9702 is based on four-point bend with the package aligned parallel to the bending direction. This mode reduces scatter in the results primarily because individual solder joints are reinforced by near neighbors at the same stress level. IPC-9702 was intended to reduce repetitive package qualification testing by standardizing methods. The results are easily compared between packages, but they do not represent the extreme condition and therefore are difficult to translate into safe working limits for tool qualifications and process characterizations. Orienting the package at 45 degrees to the bending direction increases the stress in the corner solder joints and provides a more conservative estimate of flexural limit. Hsieh & McAllister [4] have published an excellent comparative study of the various flexural options and identify spherical bend testing as the mode that generates the highest tensile stress in the corner solder joint for a given displacement from the as built condition. Celestica has selected the spherical bend test setup for this work for three primary reasons.

- It represents the most conservative estimate of Flexural limit.
- It most closely mimics the conditions imposed by "bed of nails" test equipment which is a standard process step for all most product and primary source for board deflection.
- It generates data at all four corners of the package because they are loaded equally.

TEST SETUP AND DATA COLLECTION

The spherical bend test fixture is based on a support plate with eight spherically ground pins evenly spaced on a 120 mm circle. The sample under test is centered on the circle and the load is applied from the back side in the center of the package footprint by another spherically ground pin.

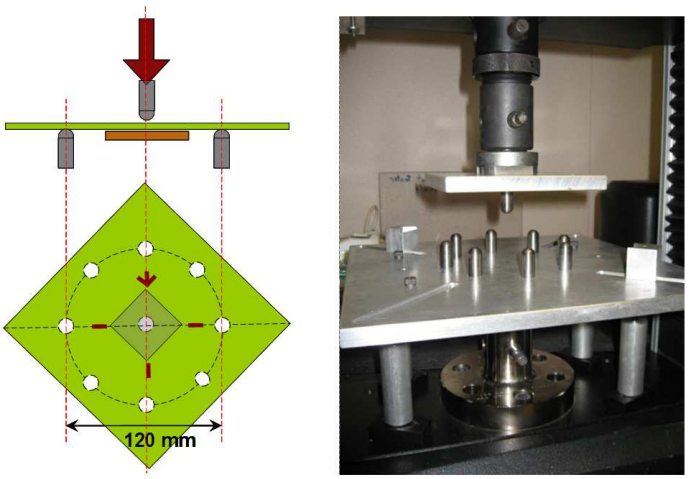

Figure 7: Spherical Bend Test Stand

The effect is to force the flat assembly into an area segment of a sphere whose radius is directly related to the displacement of the loading pin. The attached package acts as a stiffener in the center of the slab and stress is imposed in a manner directly related to the diagonal distance from the center of the package. The effect is to load the corner solder joints to failure. In fracture mechanics engineering terms the loading is mixed mode I & II.

Mode I: A tensile component of the load as the stiffener (package) resists being deformed by flexure imposed on the board. Mode 1 is opening mode when describing a horizontal crack in the solder joint.

Mode II: An in-plane shear stress component as the package resists being stretched as curvature is imposed on the system.

The loading system is described by arrows in Figure 8(A).

The principal strain on the board surface is by design coincident with the diagonal of the package and strain gauges are located on the board at the corners of the package. Where the assembled test unit is relatively compliant, gauges attached to the package corner in the same orientation also provide information. However the heavy metal heat spreader and its attachment to the package substrate make that information undecipherable for this sample set.

Data collection is setup to simultaneously record resistance in

the daisy chain, strain in the six gauges attached to the sample, displacement of the test head and the load induced by that displacement. The six strain gauges record diagonal strain and rising strain rate at each corner and the additional two at a single corner allow calculation of the principal strain and principal strain rate.

RESULTS

Previous work with more compliant systems has allowed us to record either the change in resistance that signifies failure at one of the solder interfaces or a localized minimum in the strain profile that indicates a laminate failure in either the board or the package substrate. Preliminary trials on this sample set demonstrated that these very stiff "high complexity typical" systems do not store enough energy to create these very small events at low strain levels. Strain events do occur at higher levels of displacement but they are related to catastrophic failures and do not represent the first damage to the system. Alternatively events may occur at low strain levels but the systems produce enough signal noise from vibration effects to make the events undetectable.

These preliminary results also determined that Mode 10, "Pad crater" was not only the dominant failure mode under this test method, it was the only failure mode detected in assemblies from standard "Primary Attach" processes.

A more intensive destructive evaluation of samples subjected to increasing levels of displacement (flexure) determined that for this test setup three distinct displacement zones can be defined.

- Zone 1: A safe zone where no damage occurs
- Zone 2: A mixed zone where package corners both fail and survive.
- Zone 3: A zone where all package corners fail.

The intent of further testing was to define the boundary conditions for Zone 2 and generate distributions that would allow extrapolation to safe working limits. We defined a "step stress" procedure to test groups of samples to progressively higher peak strains at fixed displacement rates. For each data point peak strain, rising strain rate and outcome were recorded. The distributions of these estimates of survivable strain were used to generate working limits.

This work also required that we redefine our criteria for failure. In compliant systems where "strain events" are recorded, failed samples inspected after penetrating dye has been applied exhibit complete separation of the BGA structure from the board. The crack path is very consistent; it involves a cone shaped failure in the "butter coat" of the laminate and follows the top surface of the glass bundles in the first reinforcing layer. We have yet to see any work in the literature that investigates the crack path. We normally assume that cracks initiate at the surface but it has been postulated that there could be considerable internal separation and coalescence of micro cracks below the surface before this catastrophic failure occurs.

As result of our analysis we have defined two distinct portions of the Pad crater crack, which represent two different levels of failure categorized as cohesive and adhesive separation.

- Cohesive Separation: The crack initiates at the surface of the laminate in close proximity to the solder pad and travels at approximately 45 degrees to the first level of reinforcement.
- Adhesive Separation: The crack subsequently follows the top surface of the first reinforcement layer until it finds a short path back to the surface inboard of the solder pad.

We understand now that in these stiffer systems the cohesive portion of the crack occurs without generating any discernable disturbance in the strain profile, but we believe that it represents a significant risk to product shipping into service environments.

If we conceptualize a crack tip as an infinitely small radius then it represents an infinitely high stress concentration. We should accept that once the crack has initiated it will require much less energy for that crack to grow. Even benign service environments have significant amounts of thermal or vibration energy present which could over time grow these cracks. There are also the issues with moisture migration and condensation when the internal glass bundles are in contact with atmosphere.

To summarize, any damage to the laminate resin system discernable by dye penetration and optical microscopy is considered to be a failure.

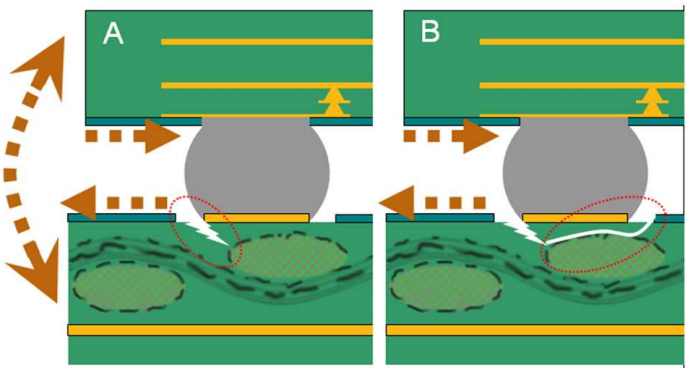

Figure 8: Pad Crater A- cohesive separation, B – Adhesive separation

Failure distributions were best modeled using Weibull distributions for two reasons.

- The failure rate is expected to be constantly increasing as the stressing factor is increased. In fact, there is a point at which no further survivors will be detected. This is the boundary between Zone 2 and Zone 3.
- The data includes both failures and survivors. In statistical terms the data is right censored.

As expected the scatter in the results increases as the testing strain rate is increased. In general the distributions of all data at the various strain rates are consistent with the behavior currently accepted by the industry. The survivable peak strain decreases as rising strain rate increases.

Distributions are combined for individual board thicknesses. Data and calculations of safe limits were plotted in the common strain / strain rate format on log linear graphs. Basic regression techniques were used to generate safe working limits over the range strain rates associated with manufacturing processes. Figure 9 is a typical output from this process and displays individual data points,

and the two limit curves based on diagonal and principal strains respectively. This process was repeated for all board thicknesses under study. This data was compared against the current estimate of the board thickness relationship and seems to correlate well. There is some evidence that the strain rate dependency for this fracture mode is different than the relationship currently accepted by the industry for SnPb assembly.

The significant additional thermal exposure of laminates and solder pads caused by forced rework of large BGA devices produces changes in the board side solder interfaces and where ENIG pad plating is present introduces a second failure mode. Mode 8 – Fracture at the NiP / NiSn IMC layer at the board side was identified as a second failure mechanism but Mode 10 remains dominant. The occurrence of two failure modes did not significantly affect the distribution of the data or the calculated limits.

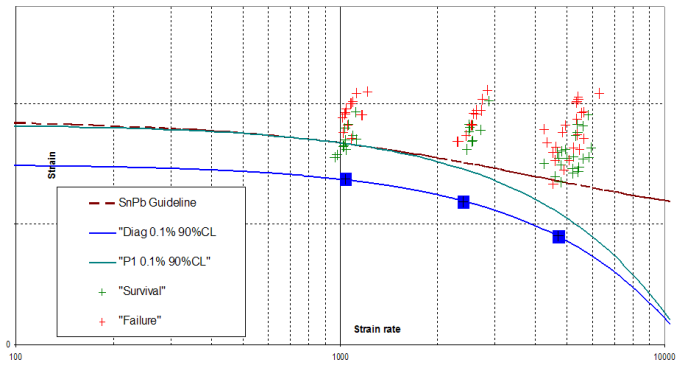

Figure 9: Typical Strain / strain rate behavior in FCBGA devices for a single board thickness

CONCLUSIONS

1. Mode 10 – "Pad Crater" is the dominant fracture mode for solder ball array devices when assemblies are fabricated using common Lead free process capable materials.

2. The Pad crater failure mechanism follows the strain rate dependent nature well established for brittle materials.

3. Safe working limits for monotonic failure in solder ball array devices can be established by board thickness for these materials.

4. Secondary fracture modes can be introduced by extended thermal exposures typical for hot gas rework of BGA devices.

FUTURE WORK

There are three additional test phases currently planned.

• We are continuing the test program to include more sub-lots that have been processed though extended thermal exposures to validate that automated rework processes do not produce a separate population across the range of strain rates associated with assembly processes.

• We are pursuing a cyclic test program to determine if multiple stress/strain excursions at what we now classify as safe levels can initiate Pad Crater type cracks.

• We are evaluating design modifications to mitigate this fracture mode.

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BIOGRAPHY

Brian Gray holds a Mechanical Engineering Degree from the University of Western Ontario. He worked as a Tooling Design Engineer for a Tier II automotive supplier until 2000, when he joined Celestica as an SMT Process Engineer. Brian held various positions in Celestica operational groups until 2008. Since that time he has been a member of the Corporate Advanced Process Development team. In this role, he is researching laminate toughness and mechanical failures in assemblies as part of Celestica's High Complexity Initiative. Brian is also the primary liason to Ryerson University for multiple joint collaborative research projects, and is currently completing his Masters degree.