Innovative Electroplating Processes for IC Substrates - Via Fill, Through Hole Fill, and Embedded Trench Fill

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ABSTRACT

In this era of electronics miniaturization, high yield and low-cost integrated circuit (IC) substrates play a crucial role by providing a reliable method of high density interconnection of chip to board. In order to maximize substrate real-estate, the distance between Cu traces also known as line and space (L/S) should be minimized. Typical PCB technology consists of L/S larger than 40 μ whereas more advanced wafer level technology currently sits at or around 2 μm L/S. In the past decade, the chip size has decreased significantly along with the L/S on the substrate. The decreasing chip scales and smaller L/S distances has created unique challenges for both printed circuit board (PCB) industry and the semiconductor industry. Fan-out panel-level packaging (FOPLP) is a new manufacturing technology that seeks to bring the PCB world and IC/semiconductor world even closer. While FOPLP is still an emerging technology, the amount of high-volume production in this market space provide a financial incentive to develop innovative solutions in order to enable its ramp up. The most important performance aspect of the fine line plating in this market space is plating uniformity or planarity. Plating uniformity, trace/via top planarity, which measures how flat the top of the traces and vias are a few major features. This is especially important in multilayer processing, as nonuniformity on a lower layer can be transferred to successive layers, disrupting the device design with catastrophic consequences such as short circuits. Additionally, a non-planar surface could also result in signal transmission loss by distortion of the connecting points, like vias and traces. Therefore, plating solutions that provide a uniform, planar profile without any special post treatment are quite desirable.

Here we discuss innovative additive packages for direct-current copper electroplating specifically for IC substrates with capabilities such as embedded trench fill and simultaneous through hole plating and via filling with enhanced pattern plate.

These new solutions not only offer better trace profile, but also deliver via fill and through hole plating. Here we describe two electrolytic copper plating processes, the selection of which could be based on the via size and the dimple requirements of the application. Process I offers great via fill for deeper vias up to

80 – 120 μm diameter and 50 – 100 μm deep. Process II is more suitable for shallow smaller vias 50 – 75 μm diameter and 30 – 50 μm deep. In this paper we show that these two processes provide excellent surface uniformity and trace profile while also providing via filling and through hole plating capabilities when controlled within given parameters. Process optimization and thermal and physical characterization of the metallization is also presented.
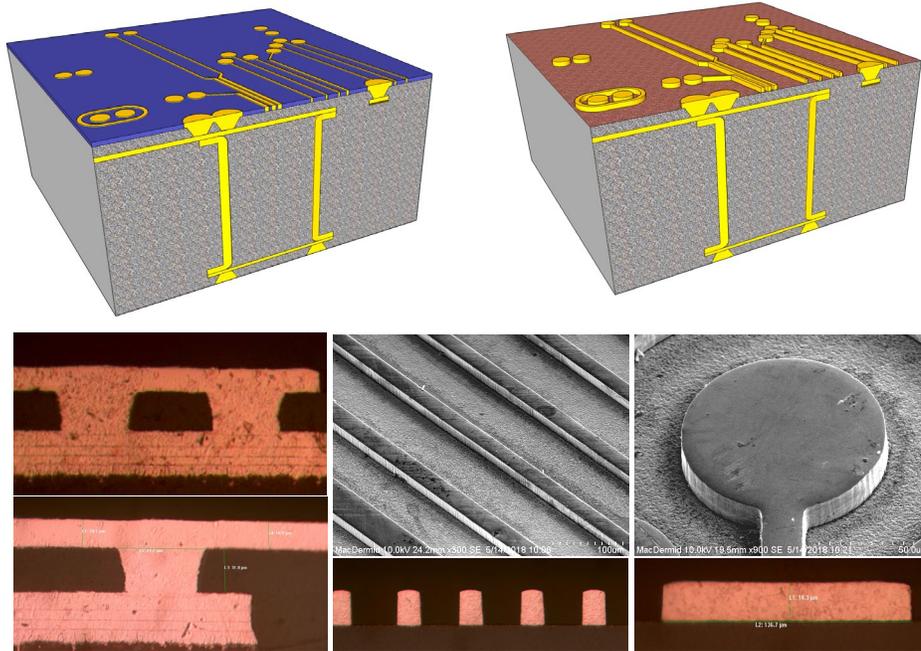

Figure 1. Capability of the processes for simultaneous via fill and through hole plating with enhanced pattern plating.
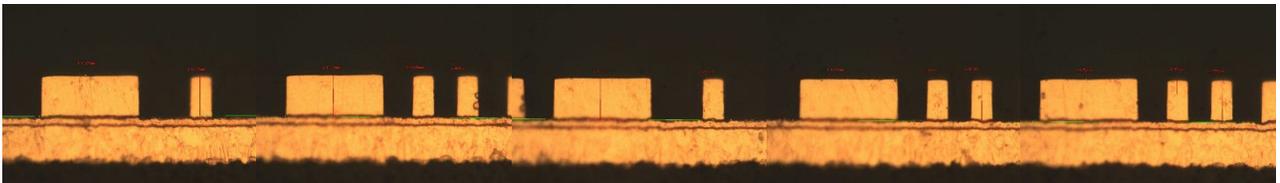

Figure 2. Embedded trench fill performance of the formulation, showing uniform height between pads and lines

KEYWORDS: Redistribution Layer (RDL), Embedded Trench, Via Fill, Pattern Plating, Metallization, Fan Out Panel Like Packaging (FOPLP), Electroplating, IC Substrate Manufacturing

INTRODUCTION

The IC substrate is the highest level of miniaturization in PCB technology, providing the connection between the IC chip and the PCB. These connections are created through a network of electrically conductive copper traces and through holes. The density of the traces is a crucial factor in terms of miniaturization, speed, and portability of consumer electronics. Trace density has grown immensely over

the past few decades to meet today's printed circuit designs, which include thin core material, fine line widths and smaller diameter through holes and blind vias. The development of fan-out panel-level packaging (FOPLP), has been a topic among the microelectronics community for some time. The main driving forces to push this new technology are cost and productivity.

Traditional Fan Out Wafer Level Packaging (FOWLP) uses 300 mm wafer as the production vehicle because larger wafers are difficult to obtain. Therefore, the FOWLP has a limitation on the basic unit of process, thereby increasing the processing steps, manpower, and cost whilst also having a low yield. The advantage of using a PCB-like substrate is that manufacturers have more design flexibility and surface area compared to the wafer. As an example, a 610 x 457 mm panel has almost 4 times the surface area of a 300-mm wafer. [1] Therefore, processing a panel this size reduces cost, time and processing steps drastically. This is a huge advantage for the high-volume production market. However, applying FOPLP technology to substrate scale poses challenges that require more research and development. These challenges are the resolution and warpage issues of FOPLP technology. If successfully implemented, this new technology will reshape consumer electronics resulting in higher production, lower cost, thinner package sizes, and faster and lighter consumer electronics. [2]

ACID COPPER VIA FILL

Electrodeposition is the one of the crucial steps in developing a circuit board, as this is where the network for routing electrical current is plated onto the PCB board as traces, vias and through holes. Copper is the conductive metal of choice due to several advantages such as its cost and relatively high electrical conductivity. Therefore, usage of copper as an electroplating metal has grown immensely over the last few decades as have the methods of plating it. Advanced, proprietary board designs require cutting edge plating tools and innovative solutions. As a result, within the last few decades impingement plating tools have become a widespread tool among the plating industry.

Copper via filling baths typically have high concentrations of copper (up to 200 - 250 g/L Copper sulfate) and lower concentrations of acid (approximately 50 g/L sulfuric acid) to promote rapid filling. Organic additives are used to control the plating rate and obtain acceptable physical properties. These additives must be designed carefully to tailor the customer needs such as size of the vias filling requirements, yield, surface Cu thickness, Cu distribution tolerance throughout the panel and the shape of the via after plating. Typical plating formulations will contain carriers, brighteners, and levelers. In theory, it is possible to fill vias with only a two-component system that includes a carrier and brightener. However, there are practical

issues with two component systems such as large dimple size, conformal fill, and difficulty analyzing for process control.

Both carriers and levelers act as suppressors but can be classified in different ways. Type I suppressors like carriers can be deactivated by the brightener whereas type II suppressors like levelers do not undergo deactivation. Carriers are typically high molecular weight polyoxyalkyl compounds. [3] Typically, they get adsorbed on the surface of the cathode and form a thin layer by interacting with chloride ions. Hence, the carrier reduces the plating rate by increasing the effective thickness of the diffusion layer. [4] Consequently, the energy level over the cathode surface topography is being equalized (the same number of electrons become available locally for plating at all cathode surface spots) so that the resultant deposit becomes more uniform and evenly distributed.

On the other hand, brighteners increase the plating rate by reducing the suppression. They are typically small molecular weight sulfur-containing compounds, also called grain refiners.

Levelers typically consist of nitrogen bearing linear/branched polymers, heterocyclic or non-heterocyclic aromatic compounds that are typically quaternary in structure (central positively charged atom along with four substituents). These compounds will adsorb selectively on high current density sites such as edges and corners, local protrusions and prevent copper over plating in high current density areas. [5]

TEST METHOD

Tests were completed in an 8-liter plating cell and 200-liter pilot tanks. Insoluble anodes were used for higher applicable current densities, easy maintenance and a uniform copper surface distribution. Each bath was made up, dummy plated for 1 Ah/L, analyzed, adjusted to correct additive levels, and then the test panel was plated. Each test panel went through a pre-clean cycle of 1 min acid cleaner, 1 min rinse, 1 min 10% sulfuric acid before the plating.

CONDITIONS AND BATH COMPONENTS

Table 1 shows the operational conditions and optimum additive levels for the two formulations. Typically, via fill baths have high copper and low acid to achieve the desired bottom up fill.

Table 1. Bath components and plating conditions.

Parameter	Process I		Process II	
	Range	Optimum	Range	Optimum
Wetter	9 - 11 mL/L	10 mL/L	3 - 8 mL/L	5 mL/L
Brightener	0.5 - 1.5 mL/L	1 mL/L	2 - 3 mL/L	2.5 mL/L
Leveler	15– 25 mL/L	20 mL/L	7 – 13 mL/L	10 mL/L
Copper Sulfate (CuSO$_4$.5 H$_2$O)	190 -220 g/L	200 g/L	80 - 120 g/L	100 g/L
Sulfuric Acid Electronic Grade	40 - 60 g/L	50 g/L	190 - 210 g/L	200 g/L
Chloride Ion (Cl⁻)	40 – 60 ppm	50 ppm	50 – 70 ppm	60 ppm

VIA FILL MECHANISM

The growth rate of copper inside the via and on the surface of the panel is controlled by the additives. Figure 3 shows a schematic representation of via copper growth. The different role played by each additive is shown. Even though the adsorption is exaggerated and shown as highly localized, both selective and non-selective adsorption occur during plating. Additive compositions must be controlled in the set range shown in Table 1 to achieve the desired "bottom-up filling". Common analytical tools used in the industry such as Cyclic Voltammetry Striping (CVS) analysis, and Hull cell plating may be utilized for this.

In Figure 3, the suppressor is shown in green, the leveler in red and the brightener in yellow. Wetter molecules are mainly adsorbed on the surface suppressing the plating there, while the leveler adsorbs selectively on to the negatively charged areas, due to the positively charged quaternized N group. This prevents over plating at the edges and avoids premature closure of the via which could result in voiding in its center. The brightener, being a small sulfur containing molecule, diffuses faster into the via and accelerates the plating. As the geometry of the via changes continuously during the plating process, the brightener becomes concentrated inside the via causing rapid plating in the via. This is called the *curvature-enhanced-accelerator coverage* (CEAC) mechanism. [6]
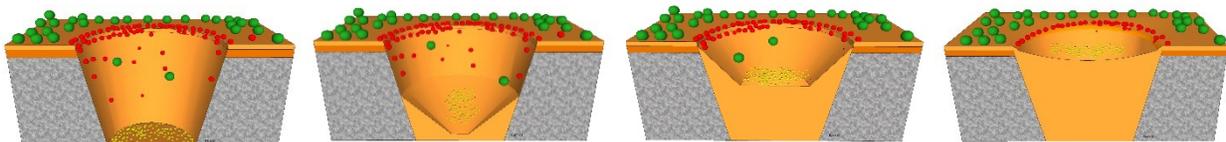
Figure 3. Schematic representation of CEAC mechanism. Suppressor is shown as green, leveler with red and brightener with yellow

Finally, when the copper plating inside the via approaches coplanarity with the surface, the plating rates inside the via and on the surface become equal and the bottom up filling stops. However, depending on how strong the additive adsorbs and desorbs, the brightener may not diffuse as expected and the high concentration of the brightener will keep accelerating the plating, resulting in over plate referred to as a "momentum pump".

FINE LINE PROFILE MEASUREMENT
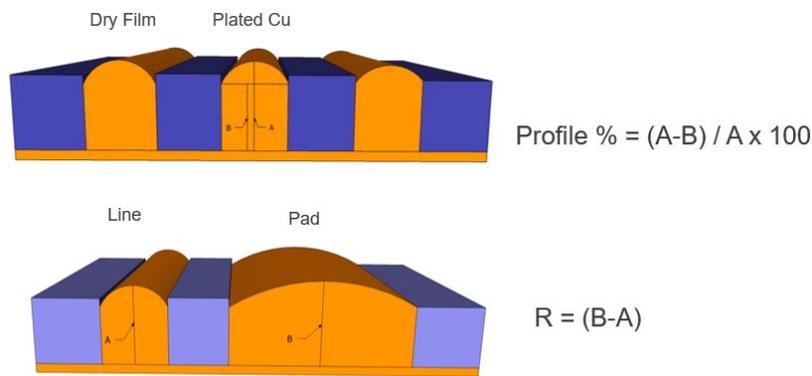
Figure 4. Profile % and R value calculation

Figure 4 shows the calculation of the profile % and the R value. The profile % is defined as the ratio between height difference of the lowest and highest points and expressed as a percentage, while the R value is the height difference between the pad area and fine lines. Minimum values for both numbers are desirable.

Process I is designed to fill vias with flat tops and to plate fine lines with better trace profile %, therefore the plating conditions are optimized as shown in Table 1. In order to achieve desired via fill capability, higher $CuSO_4$ concentration (200 g/L) was used in combination with low sulfuric acid (50 g/L).
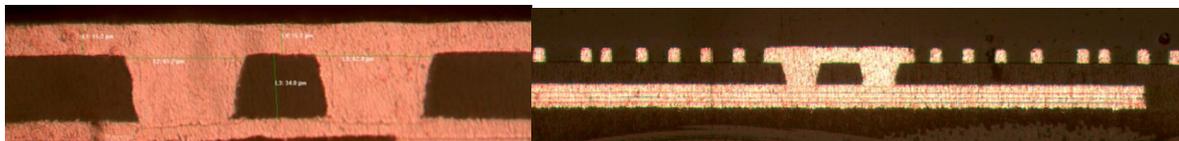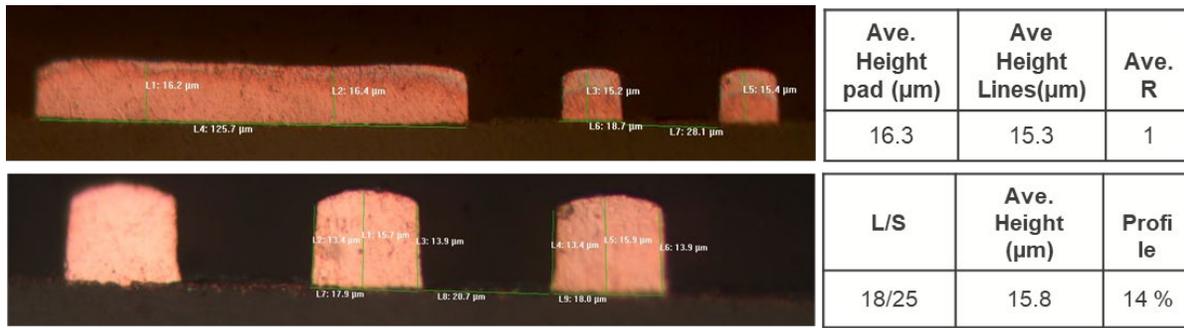
Figure 5. Typical plating performance of Process I

Typical performance of Process I is shown in Figure 5 in which vias 60x35 μm in size were filled while the total surface Cu thickness was 15 μm. Due to the ability of Process I to fill the vias with minimal dimple, no additional planarizing steps are necessary. Profile % was generally in the range of 10-15%, however there were a few instances where it was observed between 15-20%. Plated Cu thickness for the lines was 15-16 μm. The R value was between 1-2. Pad shape was closer to square, had a flat top, while lines showed a slight dome.
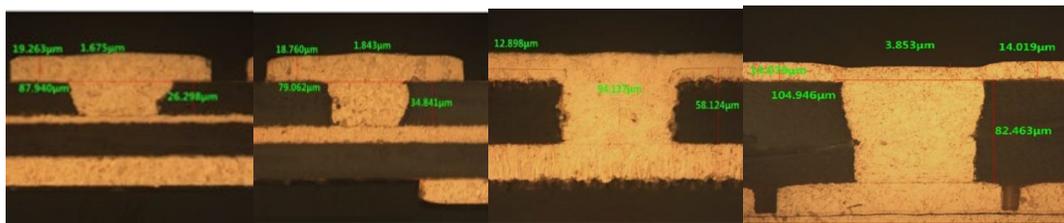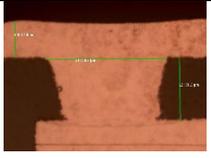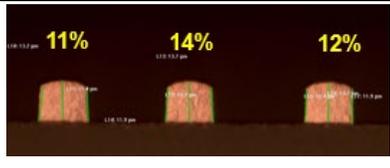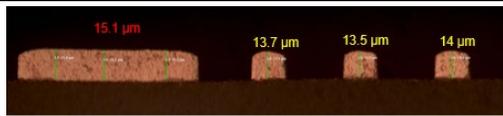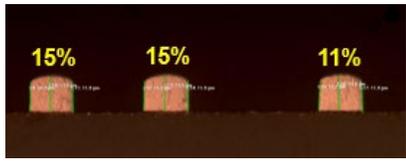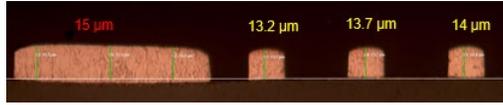

Figure 6. Filling capability of different size vias 90x25, 80x35, 90x60, and 100x80 μm, respectively.

Further evaluation of the via filling capability of the formulation was done using vias of different sizes. Four different via sizes were tested: 90x25 μm, 80x35 μm, 90x60 μm and 100x80 μm. Results are shown in Figure 6. As shown, no dimple was observed up to 90x60 μm via filling. However, larger vias such as 100x80 μm had a 4 μm dimple.

BATH LIFE STUDY

After the initial performance evaluation, a bath was aged up to 150 Ah/L. The volume of the bath was 8 L. The plating cycle for each plating was 15 ASF for 45 minutes, and additive concentration was the same as tabulated in Table 1.

Table 2. Bath aging test results profile % for 18/25, L/S and R value up to 150 Ah/L.

Age (Ah/L)	Via fill	Trace %	R
0		14% 12% 18%	14 µm 14.2 µm 14 µm 15.6 µm 1.6
50		12 % 14% 13%	15.5 µm 15 µm 15 µm 16.8 µm 1.6
100		11% 14% 12%	15.1 µm 13.7 µm 13.5 µm 14 µm 1.4
150		15% 15% 11%	15 µm 13.2 µm 13.7 µm 14 µm 1.4
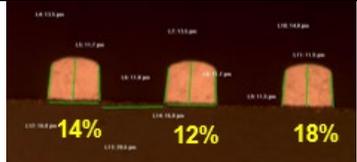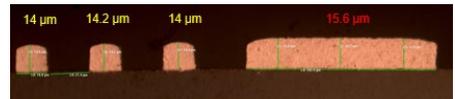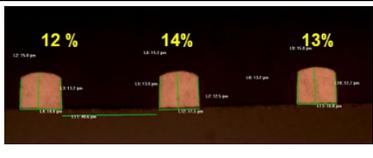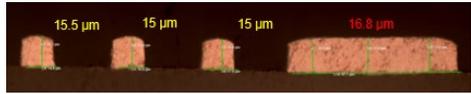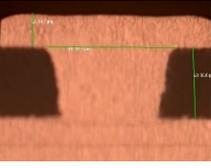
During the aging a test panel was plated at every 50 Ah/L, cross sectioned and evaluated under the microscope. The test board consisted of 60x35 µm vias and with various L/S for fine lines. Plating cycle was adjusted to obtain around 15 µm on the surface. Throughout the aging process, the lines showed Profile % in the range of 10-15% and occasionally 15-20% consistent with the initial performance tests. R value was between 1-2 with flat pad plating.

Through hole fill capability was tested using board thicknesses of 40 and 60 µm. Hole diameters were 40 and 50 µm respectively for the two boards. Results are shown in Figure 7. Plating cycle was 1.24 ASD for 60 minutes. As shown in Figure 7 the X-hole filling was excellent with Process I.
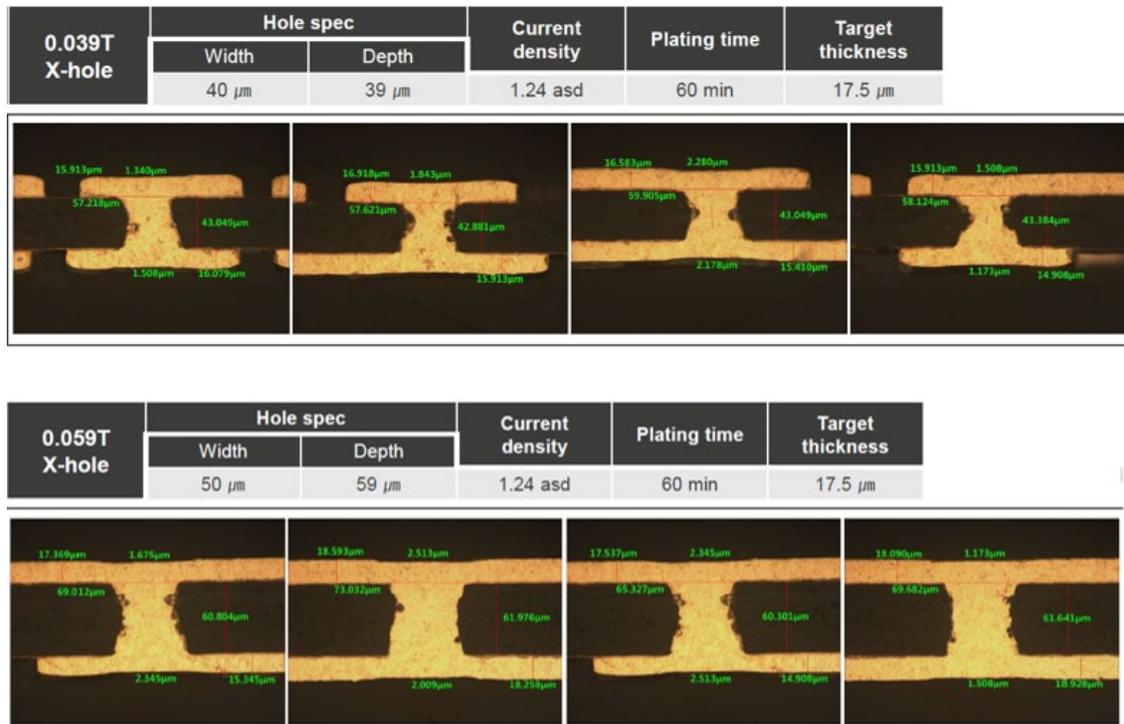
Figure 7. X-hole filling capability of Process I

TENSILE STRENGTH AND ELONGATION

Two of the most important physical properties to PCB manufacturing are the tensile strength and elongation % of the plated copper conductors because these properties are indicative of the ability for the copper metal to withstand the thermal stresses incurred during assembly and end use. The physical properties are a result of the combined influence of the additives, suppressor, grain refiner, and leveler. These properties also depend on the plating rate or current density, temperature at which the plating is done and the crystal morphology. For instance, densely packed equiaxial deposits will have better physical properties than a columnar deposit.

Physical properties were measured according to the IPC TM-650, 2.4.18.1 test method. Sample strips were extracted and baked in an oven at 125 °C for four to six hours. An industry mechanical test instrument was used to test the strips. The measurements from this instrument were used to calculate tensile strength and elongation %. Figure 8 shows the results at two different bath ages, a fresh bath and a bath aged around 100 Ah/L. According to the results the properties did not change much with the bath age and passed the IPC class III requirements.
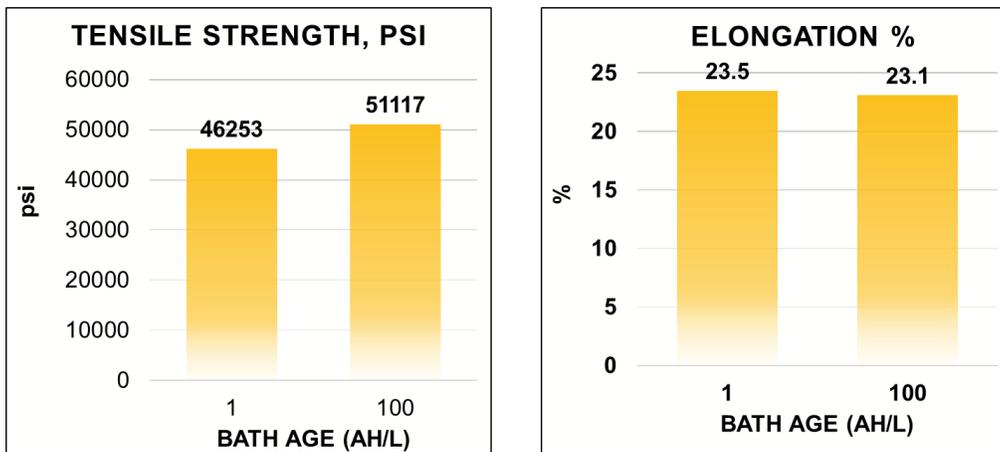
Figure 8. Physical properties, tensile strength and elongation of Process I fresh and aged baths

INTERNAL STRESS

Under the influence of additives, the plated metal deposit will have some residual internal stress. Many factors such as temperature, thickness, additives and annealing will affect the stress. Stress could be either tensile or compressive. In both cases, high stress is detrimental to the PCB board, causing distortion in the final board called warping. Here we used an internal stress analyzer to measure stress of the deposit as plated and after annealing.

To measure the stress, first a test strip was immersed in a cleaner solution at 45°C for up to 30 seconds then rinsed with water. Then the strip was dried completely and weighed. Next, the strip was plated at the desired current density for the desired time to achieve the Cu thickness necessary. Finally, the strip was rinsed with water and dried very carefully with low pressure air. Then the strip was mounted on the measuring stand (Deposit Stress Analyzer). The value for U was measured and recorded as the sum of the total number of measurement increments on both sides of the zero on the measuring stand. The plated test strip was weighed and the final weight was recorded. After the deposit thickness is known and the number of increments spread between the test strip leg tips has been determined, the deposit stress can be calculated using the equation $S = UKM \div 3T$ where, S = pounds per square inch, U = measured number of increments spread, T = deposit thickness in inches, K is the strip calibration constant, and M equals the modulus of elasticity of the deposit divided by the modulus of elasticity of the substrate material.

After the initial measurement was done the strips were annealed at 130 °C for 1h. Figure 9 summarizes the internal stress data for Process I with fresh and aged baths with both as plated and annealed strips. Low internal stress, under 1000 psi was observed for both as plated and annealed conditions and this did not change significantly as the bath ages.

Figure 9. Internal stress of the Cu deposit plated using Process I, both as plated and annealed data for fresh and aged baths.

DEPOSIT GRAIN STRUCTURE

Grain structure of the deposit was studied using focused ion beam (FIB) microscopy techniques. Plated copper samples from fresh and aged bath were evaluated. Figure 10 shows the grain structure of the deposit. In the figures, the top portion of the fine grain structure is the plated Cu from Process I and the bottom portion with larger grains are from the internal stress test strip substrate. Both images are at 5000x magnification. According to the data the grain structure remained unchanged even after aging the bath.
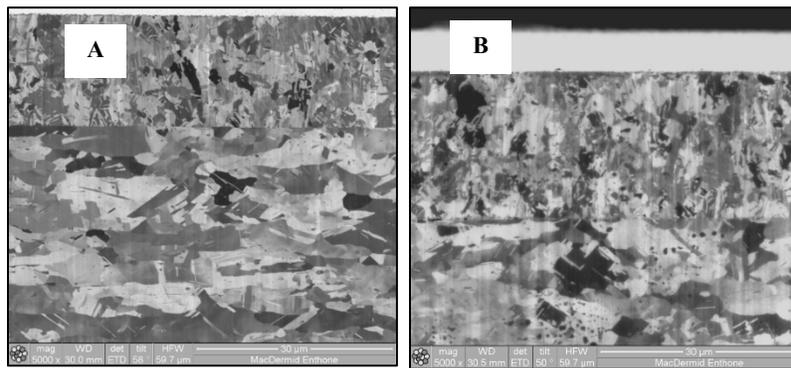

Figure 10. Grain structure with bath age, (a) fresh bath, (b)100 Ah/L

EMBEDDED TRENCH PLATING FORMULATION

Process II is tailored towards embedded trench plating applications with higher acid (200g/L) than $CuSO_4$ (100g/L) in contrast to Process I which promotes the via fill. Results are summarized in Figure 11. However, we tested Process II and its via fill capability by changing the VMS by increasing $CuSO_4$ to 250 g/L. According to Figure 11, an average dimple around 3-4 µm was seen in vias of 60x35 µm size with surface Cu of 10-15 µm. However, Process II showed excellent embedded trench plate capability with

high coplanarity with the R value of only 0.37 in the given example. The tops of the trenches were square shaped.
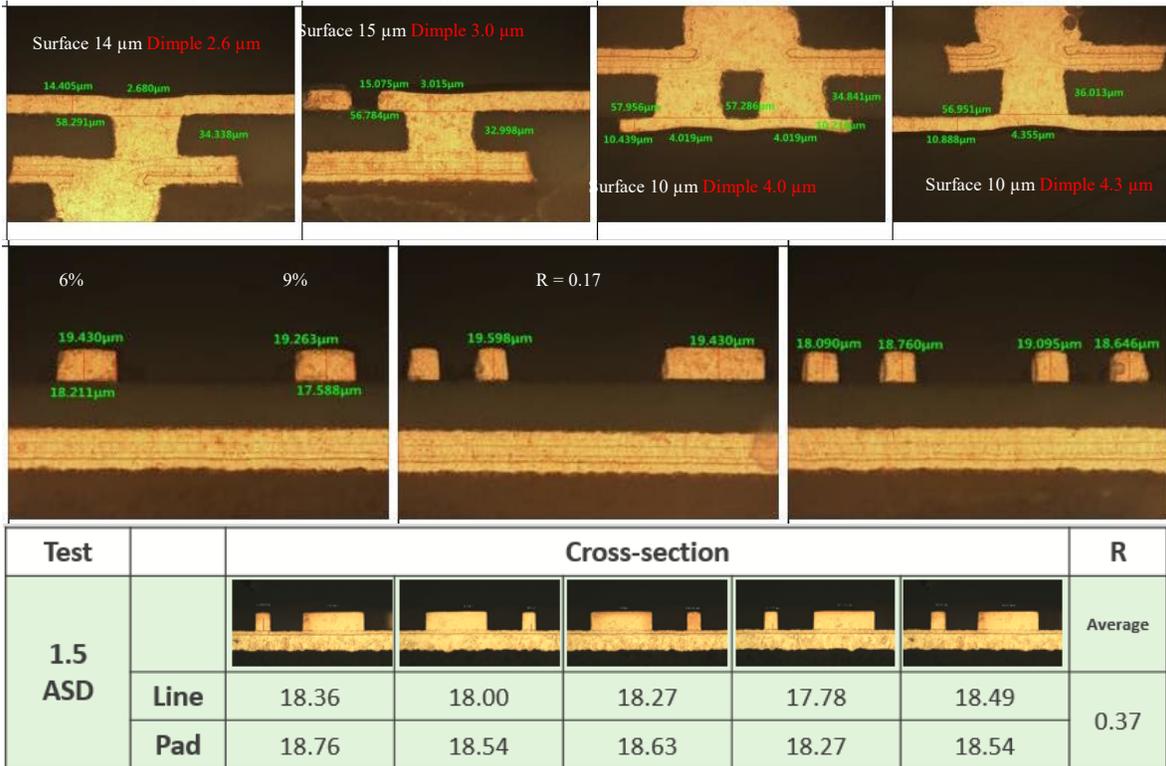

Figure 11. Via fill and trace plate capability of Process II

Process II was optimized to obtain square shaped trenches. Inorganic components, $CuSO_4$, acid, and chloride were optimized as summarized in Figure 12. Lower $CuSO_4$ and high acid gave better trench shape than the high $CuSO_4$ and low acid.

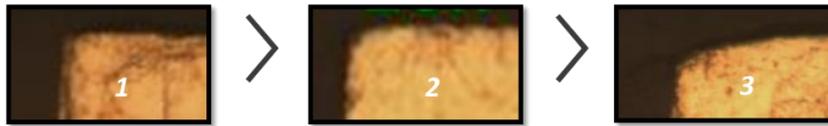| VMS	CuSO₄	H₂SO₄	Cl⁻
1	100 g/L	200 g/L	60 ppm
2	150 g/L	150 g/L	60 ppm
3	200 g/L	100 g/L	60 ppm
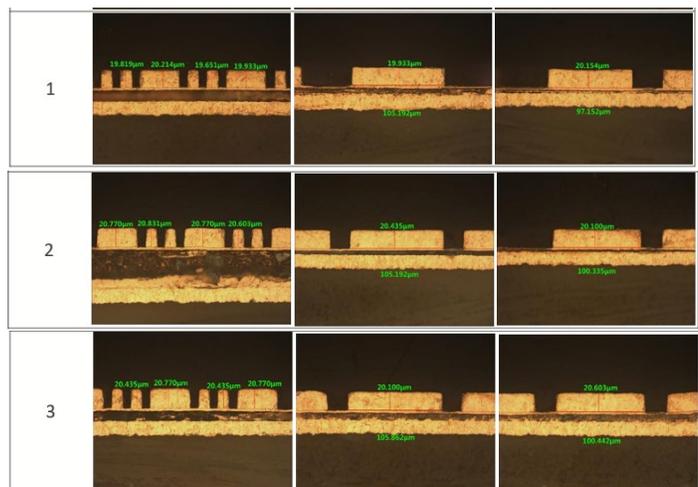
Figure 12. Trace plate with varying VMS for Process II

Further, the physical properties of Process II were measured. Specifically, tensile strength and elongation for the fresh and aged bath. As shown in Figure 13, the tensile strength and elongation % for Process II passes the IPC Class III requirements of tensile strength greater than 36000 psi and elongation greater than 18%.
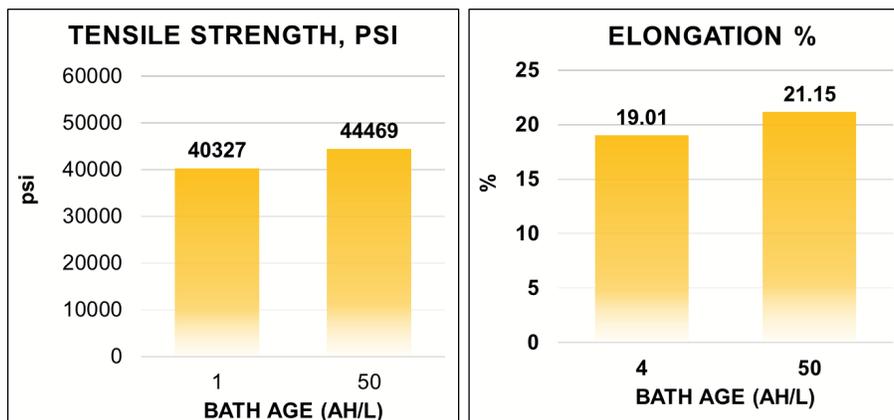

Figure 13. Physical properties, tensile strength and elongation of Process II fresh and aged baths

CONCLUSIONS

Two innovative processes for acid copper metallization in IC substrates were presented. The objective was to achieve planar via fill and flat profiles for fine line applications, and for higher uniformity of embedded trench designs between the pad height and fine line height. The formulations reported here showed excellent via fill capability and fine line profile%. Excellent uniformity between the pad and fine line areas was obtained. The deposits produced by these formulations were shown to have low internal stress both as-plated and annealed. The physical property of tensile strength and elongation produced by these deposits was stable as the bath aged and passed IPC Class III. A combined summary of these is shown in Figure 14. All the additive components utilized in these processes can be analyzed with common analytical tools used in the industry.

Process	Tensile Strength(psi)	Elongation %
I Fresh	46253	23.5
I Aged	51117	23.1
II Fresh	40327	19.01
II Aged	44469	21.15

Figure 14. Comparison of the Tensile Strength and Elongation % of the via filling focused Process I and the embedded trench focused Process II, fresh vs aged 50 Ah/L.

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