Frequently Asked Questions (FAQ)

Embedded Instrumentation:
The future of advanced design validation, test and debug

Why Embedded Instruments?

The necessities that are driving the invention of embedded instrumentation arise from several imperatives. First, the speed and complexity of technology today, starting at the chip level, has escalated geometrically. Chip-to-chip interconnects and input/output (I/O) buses have blown past the gigabits-per-second (Gbps) and are pushing into the five to eight Gbps range. Moreover, the hundreds of millions and billions of gates now present on chips have increased the complexity of devices exceedingly. This has lead to multi-core devices, multi-chip devices, new complex packaging with multiple dies and other technologies, all of which complicate the design validation, test and debug process. Happily for system developers, manufacturers and support organizations, embedded instrumentation is much more cost-effective, efficient, agile and better suited to today's emerging computer and communications technologies than are other alternatives. Embedded instruments are able to do certain aspects of design validation, test and debug that the technologies now deployed in the industry simply can not do. Necessity, of course, has had a lot to do with the invention of embedded instruments, but straightforward business sense will certainly carry it a long way in the marketplace as it becomes a critically important design validation, test and debug technology in the future.

Why is Embedded Instrumentation Needed?

Since the very beginning of the electronics industry, designers and manufacturing engineers have relied upon standalone, external instruments like oscilloscopes and logic analyzers to validate designs, verify the signal integrity on chip-to-chip interconnects and

input/output (I/O) buses, test manufactured assemblies and diagnose failures. These external instruments, which invariably relied upon physical probes to determine what was happening on the chip or circuit board and in the system, performed their tasks with admirable distinction. But, as the complexity and speed of chips, buses and systems increased, as well as the sheer density and integration of semiconductor devices on boards escalated, the inadequacies of external and modular instrumentation have become immediately apparent. Moreover, new multi-core and multi-die chip packaging techniques such as system-in-package (SiP), package-on-package (PoP) and others are only exacerbating the chip-level validation, test and debug situation.

Consider these facts:

- Placing an oscilloscope's probe on a test pad on a high-speed serial bus like PCI Express (PCIe) introduces capacitance anomalies on the bus. The validation or test engineer can't tell the difference between an instrument-induced anomaly and a fault in the design or on the manufactured assembly.
- Using external instruments to validate a typical design with high-speed serial interconnects and I/O buses is difficult and time consuming, often taking months to complete. Design validation can become a huge portion of the product's critical path. Time-to-market slows to a crawl.
- Embedded instrument technologies can perform test that existing testing strategies cannot. An example of this would be Intel IBIST technology used to stress the high speed I/Os beyond traditional OS based testing.
- Traditional measurement techniques typically only measure margins on one, or a few, lanes at a time. Embedded instrumentation such as IBIST can test and measure all lanes on all buses in parallel. This exerts more stress and provides a more complete test. It also drastically speeds up the time required to validate the system.
- Unlike OS-based testing techniques, which are typically used to test high-speed serial buses and require some system resources to run the OS, embedded instrument technologies like Intel® IBIST can test all buses and all ports at the same time without involving the OS.

As a result of these and other instances of crippling deficiencies, design and test engineers have turned to embedded instrumentation because they need the solutions only embedded instrumentation can provide.

What are Embedded Instruments?

Embedded instruments can take many shapes and forms. Some experts in the industry expect that soon the capabilities of a complete oscilloscope will be embedded as an additional resource on a chip. The types of instruments that will be embedded will be determined by many factors, such as the needs of the application, the resources of the system and the ingenuity of the chip's design team.

An IEEE working group is developing the Internal JTAG (IJTAG) standard (P1687). When ratified, this standard will specify methods for managing the configuration, operation, and collection of data from embedded instrumentation. This group defines embedded instrumentation as: "Any logic structure within a device with a purpose for Design-for-Test (DFT), Design-for-Debug (DFD), Design-for-Yield (DFY), Test..." This document goes on to say: "There exists the widespread use of embedded instrumentation (such as BIST Engines, Complex I/O Characterization and Calibration, Embedded Timing Instrumentation, etc.)…"

How Do Engineers Use Embedded Instrumentation?

At least initially, the ASSET ScanWorks platform will automate, acces and analyze instruments embedded at the chip level through the JTAG (boundary scan or IEEE 1149.1) port on chips and the JTAG infrastructure on circuit boards and in systems. Given the fact that ScanWorks is the leading tool for accessing JTAG resources and applying tests, this is a natural place to start for ASSET. However, future generations of the ScanWorks platform will likely incorporate the access method best suited to the application, chip technology and/or the embedded instruments involved in the application. In addition, ASSET's MicroMaster CPU emulation system can also utilize the debug port found on many processors.

What does ScanWorks do?

ScanWorks automates, accesses and analyzes embedded instrumentation.

For example, pattern generation and checking is a basic functionality for the ScanWorks platform. This capability provides the basis for several instrumentation applications such as bit error rate testing (BERT) and margining. With pattern generation and checking, ScanWorks can validate the transfer of basic, user-definable test patterns across buses and even individual lanes on buses.

ScanWorks' BERT testing capabilities can test individual lanes or multiple lanes simultaneously, accelerating design validation time as well as stressing a significant portion of the system to identify interrelated or dependent faults and failures. Margining gives the designer a push-button tool to generate graphical eye diagrams that visually demonstrate the signal integrity on high-speed channels in the system. An example of a graphical margining diagram appears below.

Margin Chart for PCIe Ports 0 23
10:34:22 AM, 5/7/2007
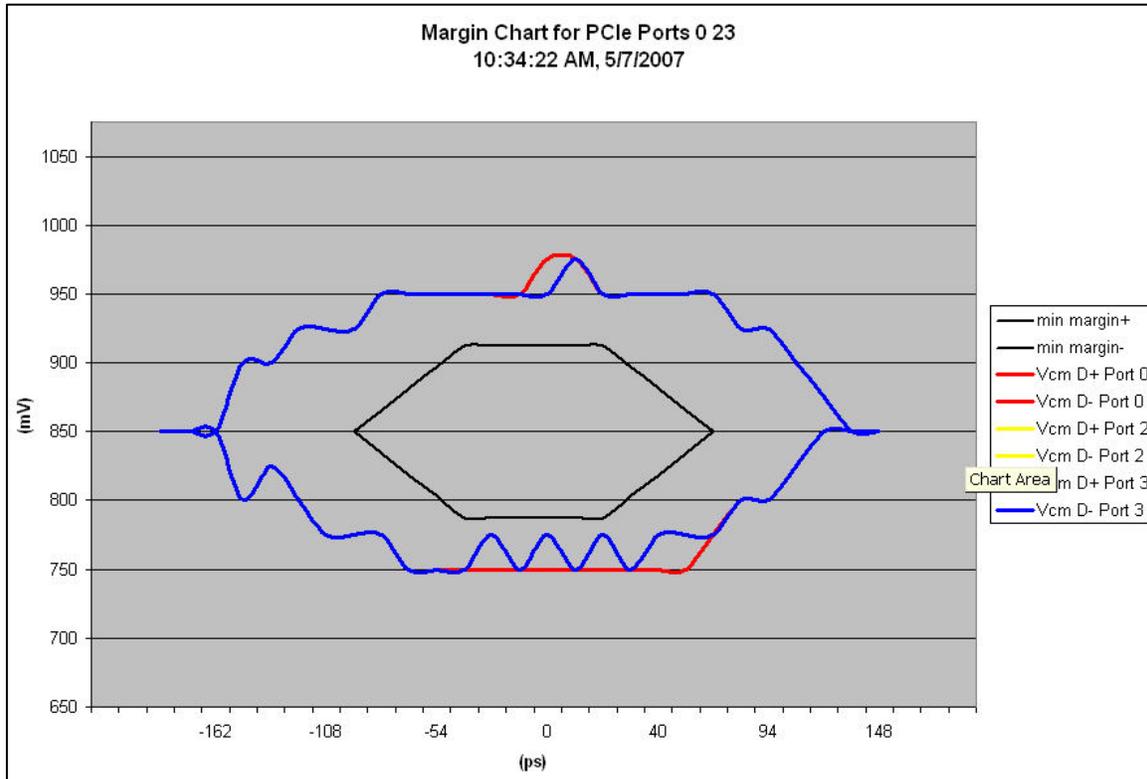
Where and When Is Embedded Instrumentation Used?

Embedded instrumentation can be called upon during every phase of a system's life cycle. For example, design validation has a critical need for the capabilities of embedded instrumentation. Without it, the design team can not test and validate the signal integrity on high-speed buses. As the circuit board, sub-assembly or system move into manufacturing, embedded instrumentation will be used to perform at-speed tests and diagnose failures. And once the product has been deployed in the field, embedded instrumentation could be accessed and engaged locally or remotely by service technicians to diagnose performance issues and troubleshoot failures.

Who's Doing What with Embedded Instruments?

ASSET InterTech has taken a leadership position in developing tools that automate, access and analyze embedded instrumentation. The ScanWorks environment is the only tool available today for Intel®'s Interconnect Built In Self Test (IBIST), an embedded instrumentation technology that Intel is designing into its next-generation processor chips and server platforms.

In addition to Intel's IBIST, several other embedded instrumentation initiatives are underway at this time. These include the following:

- IEEE P1687 (Internal JTAG or IJTAG) – Based on the 1149.1 boundary-scan infrastructure, this standard is being explored as a control methodology for embedded instrumentation.
- IEEE P1149.7 – This is a chip-to-core interface using the core's 1149.1 port, P1687 and/or other technologies.
- IEEE 1500 – This is a core wrapper standard, which has no access standard defined for it at this time. The P1687 working group is considering offering IJTAG as a solution to the IEEE 1500 committee.
- IEEE 1450 – This is the STIL test language that was defined for the reuse of chip test data.

Many companies are active in embedded instrumentation. Some of their initiatives are listed below:

- **Intel**: -- IBIST is Intel's next-generation embedded instrumentation technology which is being deployed throughout the company's high-end chips and chipsets. ASSET's ScanWorks platform was the first and is still the only third-party open tools platform that supports IBIST.

- **Synopsys**: -- The DesignWare® Verification Library consists of embedded instrumentation intellectual property (IP). Some of the modules in the library integrate into Verilog, SystemVerilog, OpenVera and VHDL testbenches to generate and respond to bus traffic, check for protocol violations and generate coverage reports that can be incorporated into chip designs. Instruments like digital and analog converters, pattern matchers and generators, voltage and phase controllers, limit comparators and others are included to provide test coverage within chips, not just at the pins.

- **Rambus**: -- This memory company has integrated a programmable pseudorandom-pattern generating instrument and bit-stream comparators into I/O blocks on its memory chips. This was prompted by high-speed receivers that make it virtually impossible to see what is going on inside a memory block.

- **Xilinx**: -- This company's ChipScope Pro real-time debug and verification tool inserts logic analyzer, bus analyzer, and virtual I/O instruments directly into an FPGA, allowing the engineer to view any internal signal or node, including embedded hard or soft processors.

- **Altera**: -- Altera recently made its Pre-emphasis and Equalization Link Estimator (PELE) available to EDA companies such as Mentor so that designers could embed PELE and deploy it in signal integrity applications on Altera's Stratix® II GX FPGAs.

- **Vitesse Semiconductor**: -- This networking/communications chip vendor has devised a two-channel approach to obtain an eye diagram or other instrumentation plots that validate the performance of high-speed receivers. The primary channel

is set up as the center of the eye diagram while the secondary channel collects phase and amplitude data to populate the diagram and compute bit error rates.

- **Maxim**: -- A family of power managers from this chip company features monitoring instrumentation so that the devices can monitor, sequence, track and margin multiple system voltages, adjusting voltages according to pre-programmed limits and storing fault data for further analysis.

- **DAFCA**: -- DAFCA is an EDA software company with tools that allow chip design teams to seamlessly incorporate compact and reconfigurable instrumentation from this company's IP library.

- **Logic Vision**: -- This chip tools company's ET*Serdes* product is described as an embedded SerDes loop-back solution that structurally characterizes the parameters which determine signal eye distortion tolerances, verifying the parameters designers consider during a SerDes core design.

The list above is by no means complete or comprehensive. Several others companies, including Tundra, Texas Instruments, LSI, Avago and others are also providing embedded instrumentation technology.

How Will Embedded Instruments Change the Design Validation/Test/Debug Landscape?

Over time, embedded instruments will have a profound effect on design validation, manufacturing test and other aspects of a system's lifecycle, including debug. Embedded instruments give designers a cost-effective and software-driven alternative to external and modular test instruments. Greater agility and flexibility will result. Validation routines and tests can be applied practically anywhere and at any time because the needed instruments are already present in the system and application tools like ScanWorks are software-based.

Moreover, the thoroughness and comprehensive nature of design validation and manufacturing test will only be enhanced by embedded instrumentation. Not only will this accelerate the delivery of new products to market, but it will also improve the reliability, durability and overall quality of electronic systems.

What is the Industry Saying about Embedded Instruments?

"As the industry continues to expand high speed serial signal architecture demands, a growing dependency on IBIST is required for validating and testing the technology within Intel Corporation."
Gene Pitts, Director Server Platforms, Technical Marketing, Intel Corporation

"With the growing complexity of SOC designs, leading design teams report that they are dedicating more and more planning, implementation, and silicon area to circuitry that supports debugging rather than test."
Ron Wilson, Executive Editor, EDN Magazine in an article entitled: "Design for debugging: the unspoken imperative in chip design", June 21, 2007

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