

# Package-on-Package (PoP) Warpage Characteristic and Requirement

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## Abstract

Package-on-Package (PoP) technology is widely used in mobile devices due to its simple design, lower cost and faster time to market. Warpage characteristic and requirement of PoP package becomes critical to ensure both the top and bottom package can be mounted with minimal yield lost. With this challenge in placed, iNEMI has been working relentlessly to fingerprint the current PoP package technology warpage characteristic and to establish some key learning for packaging technologies. The work also extended to understand the basic requirement needed for successful PoP stacking by analyzing the warpage data obtained and formulate a simple analytical equation to explain the true warpage requirement for PoP packaging. The warpage characterization also extended to evaluate the effect of bake and Moisture Exposure Time (MET) on package dynamic warpage. These will provide a better holistic view of cause and effect in PoP package stacking. Keywords—dynamic warpage; Package-on Package (PoP).

## Introduction

Electronics packaging technology has been relentlessly changing and pushing the design boundaries [1]-[4] where new materials, assembly process, ultra small geometry, 2.5D and 3D integration have been adopted. This drives multiple assembly and surface mount challenges. Among many, package warpage characteristic has been the industry wide common focus. The introduction of a JEDEC's reflow temperature warpage specification [5] gives more realistic assessment to component board assembly yield compared to room temperature coplanarity as demonstrated in [6]. Based on JEITA specification [7] and experimental work from Cho and Amir et.al. [8], both concluded that there are sets of warpage flatness requirement at elevated temperature that depends on the gap formed between the package joints and board pads. The iNEMI technology roadmap [9] gathered a more conservative high temperature warpage allowable for range of ball pitch and diameter. To put these in perspective, Fig. 1 shows the respective specifications as a function of ball pitch and diameter. The graph shows that as the ball pitch and diameter reduces, the allowable warpage reduces. However, these specifications may and may not encompass the need for Package-on-Package (PoP) technology.

PoP is widely used in mobile devices due to its integrated design, lower cost and faster time to market [10]. Warpage characteristic and requirement of PoP package becomes critical to ensure both the top and bottom package can be mounted with minimal yield lost. The current state of PoP warpage requirement has not been reevaluated and formed in clear specification other than customer specific requirement. The typical SMT defect modes like Non-wet open, solder bridging, head and pillow and non-contact open as shown in Fig. 2 are applicable to both the joints between the PoP bottom

package with the board and the PoP memory package. Other gross SMT defect can occur when there are geometry interference between the PoP packages. This shows the need of ensuring the warpage between PoP bottom and memory package is compatible. There were efforts to leverage the warpage characteristic of the PoP packages warpage to predict the SMT yield performance as highlighted in [11][12].

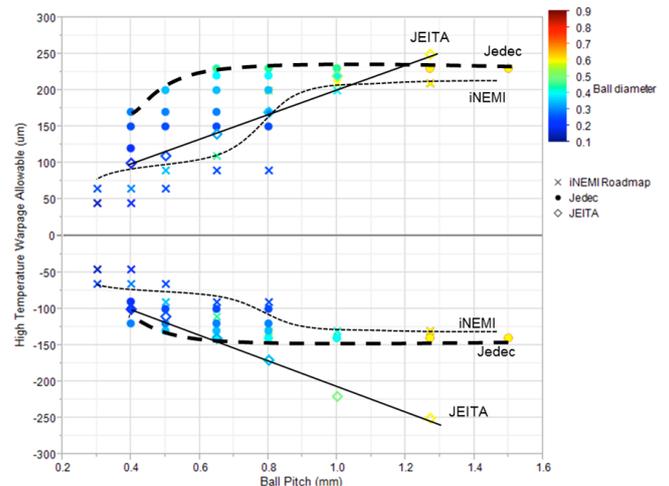


Fig. 1. High temperature package warpage allowable for BGA package stated in respective bodies.

With more emerging PoP packaging technology development, iNEMI is working relentlessly to establish the current PoP package warpage characteristic and understand the effect of current measurement criteria that potentially address the component board assembly challenges. The proposed work also incorporates an evaluation on how to improve the package warpage qualification process, such as sample size used, reporting, shape definition and effect of environmental staging.

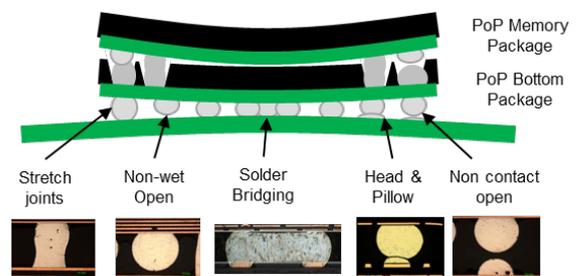


Fig. 2. Typical SMT defect modes.

## Approach

### A. Samples

The PoP package is widely used in smart phones, tablets, etc. where the end product thickness and size constraints are paramount. In recent years, PoP has gained significant attention on enabling sleeker package construction. For this study, there are basically six types of PoP bottom packages with different geometry and construction as shown in TABLE I. The package size ranges from 12x12mm to 14x16, while the package thickness ranges from 500um to 600um (excluding the BGA ball height). There were a few variance of PoP memory package considered with size ranges from 12x12mm to 14x16mm as well. The PoP package constructions varies depends on design choices, package thickness requirement and compatibility to PoP memory package. The samples acquired for this study were from kind donation from the industry and limited geometrical information were given.

TABLE I. POP PACKAGING TECHNOLOGY CONSIDERED

Design	Schematic drawing
Overmold TMV <sup>®</sup>	
Expose Die TMV <sup>®</sup>	
Bare Die PoP	
Interposer PoP	
Pre-stack PoP package	
MCeP <sup>®</sup>	
PoP Memories	

### B. Dynamic Warpage Measurement Technique

Electronic package warpage changes under the influence of temperature due to thermal strain mismatch among the materials used to construct the package. Dynamic warpage is common terminology used to describe such behavior. There are many measurement tools that are used to measure the dynamic warpage of the package as listed in [10]. The most common tool made available for this study is the thermal shadow moiré tool. The ability to measure the warpage at elevated temperature gives better risk assessment for component board assembly joints formation. The common convention used to define the warpage direction is based on “+” and “-” magnitude which represent convex and concave direction. However, there are shapes that are hard to determine just using the two signs.

The measurement was conducted based on the availability of the sample and perceived risk level. There were three preconditioning considerations; As Is, Bake and MET

(Manufacturing Exposure Time), listed in TABLE II. The purpose of these considerations are an attempt to mimic potential condition prior to board assembly.

The As Is mimics the potential condition where packages are directly mounted to the board after taken out of sealed bags without much staging time. The Bake mimics the condition where the package is baked after being staged for unknown condition prior to board assembly. The baking process potentially alters the stress state of the package and removes any diffused moisture. The MET-9Days mimics the condition where the package is being staged in the factory floor for 9 days exposed to 30°C and 60%RH prior to component board assembly process. The typical MSL 3 calls for a maximum 7 days of staging, but the work here extended to 9 days to take into account any unforeseen circumstances. These three precondition environments may potentially demonstrate different package warpage behavior and board assembly yield depending on the packaging technology used. Due to uneven samples acquired, some package types listed here were not subjected to all these preconditions.

TABLE II. PRECONDITION

Preconditioning	Description
As Is	Units used for board assembly immediately after taken out from seal bag.
Bake	Mimic condition where package moisture level being reset by baking it for 24hrs at 125°C
MET 9 Days	Mimic 7 days component board assembly staging time + 2 days of unforeseen delays. Exposed to 30 °C and 60%RH prior to warpage measurement

### PoP Bottom and Memory Package Warpage Characteristic

The As Is dynamic warpage behavior for these PoP bottom packages is shown in Fig. 3. It can be observed that the majority of the dynamic warpage behavior started from convex (+) at room temperature to concave (-) at elevated temperature. There is one sample that behaves in a unique way, where it was concave at room temperature and less concave at elevated temperature. While other samples remain the shape in concave or convex across the temperature range with minimal magnitude changes. Depending on the construction of the package, they exhibited different room temperature warpage magnitude ranges from ~50um to 150um while at high temperature warpage float more than -100um.

The effect of Bake and MET on room temperature and 260°C are shown in Fig. 4. It has been determined that the package warpage was technically comparable among the preconditioning considered. There is some signal where baking the package reduces some variation of the warpage magnitude but this requires more statistical approach to confirm the finding. In general, the data suggested that these ultra-thin packages are not sensitive to the precondition



Based on warpage measurement stipulated in [14], the PoP package warpage can be extracted just from the BGA region along the peripheral edge of the PoP Memory package. The peripheral warpage magnitude, as shown in Fig. 6, is generally lower than the entire package area, as expected due to the smaller area of interest. The benefit of analyzing peripheral BGA warpage provides some perspective of which region of the package contributed the most warpage. For example, POPmB5 has ~50um warpage for entire package area while <20um for the peripheral BGA warpage at elevated temperature. This shows that the region without BGA balls contributed part of the warpage magnitude. While for POPmB7, both package area and BGA area have approximately the same level of warpage. Depending on the engineering assessment needed, the entire package area warpage plays more critical role in PoP stack up assembly because it gives better insight of any geometrical interference with PoP bottom package. However, the coplanarity specification in [2] only called for measurement of the BGA area coplanarity, which may subject ambiguous correlation to PoP component board assembly yield.

As for the effect of preconditioning on PoP memory warpage, Fig. 7 shows the interaction of room temperature and peak reflow temperature warpage magnitude as a function of As Is, Bake and MET 9 Days. The room temperature warpage for POPmB4 and POPmB7 are affected by Bake and MET preconditioning. POPmB7 exhibited 50um increase in room temperature warpage while exposure to moist environment reduces the warpage. This could be due to stress relaxation happened during baking while the package swells when exposed to moist environment. However, the warpage at high temperature was not impacted among the PoP memory considered. This seems to suggest that baking and moisture induce warpage changes has less impact on thin packages at high temperature.

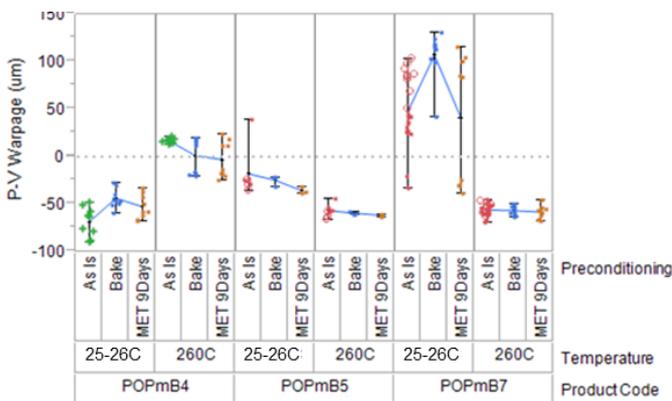


Fig. 7. Effect of As Is, Bake, MET 9 Days to package warpage at room and peak reflow temperature for POP memory packages

### Package Warpage Qualification Improvement Opportunity

Based on the warpage data collected, we have a fundamentally broad dataset to analyze further with respect to warpage qualification assessment. The reporting format of the

package warpage as stipulated in [14] and data reported elsewhere typically used a few samples due to limited resources and other specific constraints. When addressing board assembly yield related issue, the limited sample used for dynamic warpage measurement may, or may not explain the corresponding yield performance. Hence some statistical method is required to determine the minimal requirement of sample size needed within allowable resources. Fig. 8 shows the warpage magnitude obtained from multiple random sampling simulation by selecting pre-defined sample size from a pool of units. The pool of data was obtained by combining the earlier warpage measurement for As Is, Bake and MET 9 Days for a given product candidate to capture the potential noises that may exist in manufacturing environment. From the graph, the mean warpage and standard deviation will fluctuate more than 5% when less than five samples are chosen from the pool. The mean warpage and standard deviation are kept within 5% when sample size used was nine, or more. The same finding is established when repeating this sampling simulation on other products. This seems to suggest that a minimal of three samples as stipulated in [14] may not be enough in some cases. Furthermore, the sampling method may need to consider multiple assembly batches to establish a representation of the warpage magnitude range that is useful for component board assembly yield assessment [11][12].

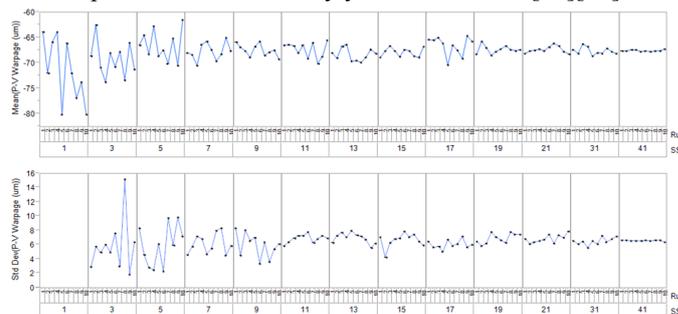


Fig. 8. Effect of sample size used for dynamic warpage characterization. (SS: Sample size; Run: Random selection of sample from a pool of units).

Based on the dynamic warpage characteristic obtained for PoP bottom and PoP memory packages, it shows that the electronic industry is creating packages with broad dynamic warpage characteristic that depends on the entire design and material set used. The warpage magnitude at peak reflow temperature can play a major role in surface mount yield and such should be reflected in the Jeduc or any industry guideline. Alternatively, there are many customized component board assembly recipes that may be used to mount packages [11]. The impact of As Is, Bake and MET requires constant evaluation to ensure the dynamic warpage characteristics are understood. The impact of more complex warpage shapes like “M” and “W” in PoP stack up analysis require more focus to establish the fundamental of component board assembly yield assessment.

### Summary and Next Steps

The work here covered a very broad dynamic warpage characteristic of different PoP bottom, PoP memory packages.

Impact of As Is, Bake and MET were quantified and requires more consistent characterization across component suppliers to establish the sensitivity to the precondition environment, in order to mimic potential component board assembly. The sample size needed to establish a representation of warpage and the use of statistical tool in package warpage reporting requires more focus if the attempt is to correlate with component board assembly yield. This is because most of the yield lost may be due to extreme warpage characteristics that may not have been captured by just using a few samples. The data collected here requires further analysis to enhance the warpage qualification method.

### Acknowledgment

This project is a joint effort of iNEMI members: Akrometrix, Alcatel-Lucent, Delphi, Flextronics, Hitachi Chemical, Intel, iST, Sanmina-SCI, SEMCO, Shengyi Technology and TI. We appreciate the supports from industry and companies who provided samples, including Altera, Amkor, Cisco, Freescale, Fujitsu, Intel, Shinko, StatsChipPAC, TI and Wistron.

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