Joule Heating Effects on the Current Carrying Capacity of an Organic Substrate for Flip-Chip Applications

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ABSTRACT

This paper deals with the thermal effects of joule heating in a high interconnect density, thin core, buildup, organic flip chip substrate. The 440 μm thick substrate consists of a 135 μm thick core with via density of about 200 μm. The typical feature sizes in the substrate are 50 micron diameter vias is the core/buildup layers and 12 micron thick metal planes. An experimental test vehicle is powered with current and the temperature rise was measured. A numerical model was used to simulate the temperature rise in the TV. Good agreement between the test results and model are established. The numerical model is then used to simulate via and substrate temperature rise by varying a variety of parameters. Using typical arrangements for via distribution, it is shown that currents in excess of 500A can be supplied to a 16mm chip using the thin core organic substrate technology while limiting the maximum via temperature rise to less than 10C above the chip temperature.

INTRODUCTION

Organic flip-chip packages are increasingly being used for high performance ASIC and microprocessor applications [1]. Electrical performance enhancements [2], interconnect reliability [3], and cost are the primary reasons for choosing organic substrates. Recently, [4, 5] showed that the thermal performance of flip chip packages with organic substrates can be on par or better than packages with ceramic substrates.

Innovation in fabrication techniques and materials has led to the adoption of "thin core" organic substrates for the many demanding applications. These substrates are characterized by reduced thickness (around 0.5mm or less). This in turn enables reduction in core via diameter. Consequently, the core via pitch can be of the same order of magnitude as the flip chip bump pitch, if needed. Further, this also enables the use of laser via drilling.

It is well known that increasing chip power dissipation has made severe demands on package thermal management schemes. For high powered flip-chip packages, the most common thermal management technique is to use a heatsink or coldplate directly attached to the package heatspreader/lid. The substrate often plays a minor role (there are exceptions, see [5]) in such situations. However, increased power dissipation and decreasing core voltage increases the current demand of the chip. Thus, there is a creeping trend of higher ohmic or joule heating (I^2R) in the path of the current flow. Since the substrate is in the current path, there is a very real concern of excessive temperature rise in the substrate [6, 7]. Although the joule heating power is orders of magnitude less than the chip power it tends to be localized in the vias. Consequently, the local temperature rise (vias/substrate) has to be contained. This is especially perceived to be true for organic substrates because of the relatively lower thermal conductivity of the dielectric material. The existence of voltage and ground planes mitigates this concern somewhat. In general, it is necessary to have clear guidelines for the current carrying capability in order to assist electrical layout designers.

This paper addresses the concern [7] of joule heating in organic substrates. The issue of electro-migration [8] is another issue concern high current densities, but is not addressed in this study. A high performance thin core substrate is used as a demonstration vehicle. The maximum temperature rise of the via/substrate is assumed to be no more than 10C. This study is a numerical study. Experimental testing is undertaken with an appropriate test vehicle so that boundary conditions and material property assumptions can be validated. The numerical model is then used under various scenarios of via distribution and substrate boundary conditions to predict temperature rise. Finally, the results are condensed based on the chip power density (W/mm^2) that can be supported by the thin-core substrate technology.

SUBSTRATE DESCRIPTION

Figure 1 shows a cross-section of the substrate under consideration [3]. It is a "3-4-3" crossection comprised of a core layer and three layers of buildup on each side of the core layer. The nominal via diameter is 50μm for both the core and the buildup layers. The core vias are plated with a via wall diameter of about 12mm. The buildup vias as shown are plated fully solid and stacked. Figure 1 shows a "thick" version of the substrate with a total thickness of 700μm. A "thin" version of the substrate with a total thickness of about 580μm can be fabricated. Some salient features of the substrate that are favorable to the joule heating concern are substrate thickness (thin-core), and stacked/solid vias. Both these features improve the electrical characteristics by reducing the DC resistance, and improve the thermal characteristics by reducing the thermal resistance.

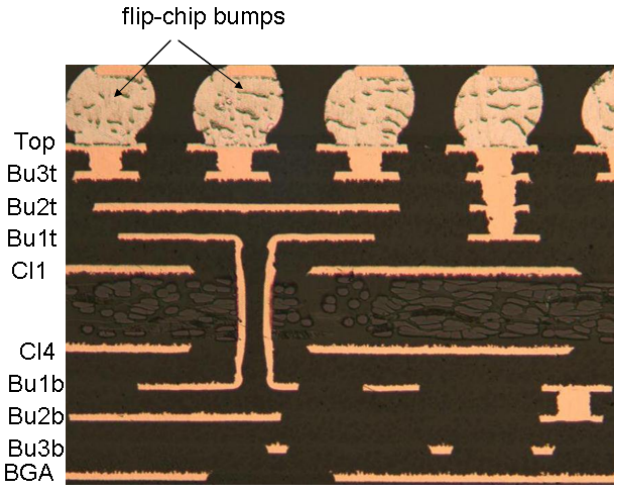

Figure 1: Cross-section of substrate (700 μm) showing flip chip bumps at top and BGA pads at the bottom.

VIA COUNT BY LAYER IN A TYPICAL DESIGN

Table 1 below shows the typical via count for a 16mm chip connected to a "2-4-2" substrate similar to the section in Fig.1. The via count in the table was determined based on careful examination of a number of representative ASIC designs. Note that since there are only four buildup layers (two on each side of the core), two layers (Bu3b and Bu3t) in Fig.1 are absent in Table 1.

Table 1: Layer to layer via count in a "typical" 2-4-2 substrate

Layer	Under chip signal	Under chip power	Surround chip signal	Surround chip power
Top to Bu2t	1080	1038	0	150
Bu2t to Bu1t	830	1038	250	150
Bu1t to Cl1	830	1038	250	200
Cl1 to Cl4	580	1038	500	250
Cl4 to Bu1b	330	519	750	300
Bu1b to Bu2b	330	250	750	343
Bu2b to BGA	80	176	1000	343

JOULE HEATING EXPERIMENT

Experiments were performed to validate the geometry and modeling assumptions used in this study. Test vehicles with a stitch pattern were fabricated. A cross-sectional schematic of the test vehicle is shown in Figure 2. Stacked via stubs are arranged in a pattern. The pattern of vias is connected in a "daisy-chain" manner. There are two independent daisy chain patterns on the top and bottom sides of the core respectively. The core vias are not included in the stitch pattern. Only the upper and lower buildup layers are included. When current is passed through the stitch daisy chains, joule heat causes the entire substrate to heat up.

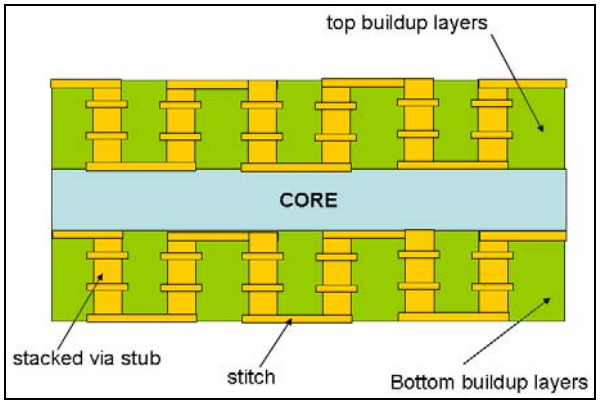

Figure 2: Cross-sectional view of the substrate stitch pattern.

In the planar direction, the via stubs are arranged twenty five to a row. There are ten rows in all. The transition from one row to the next row in the stitch pattern occurs as shown in Figure 3. All vias are 50μm in diameter. Along a row, the via-to-via pitch is about 450μm. The stitch features connecting adjacent via stack stubs are 12mm in thickness and 88μm wide.

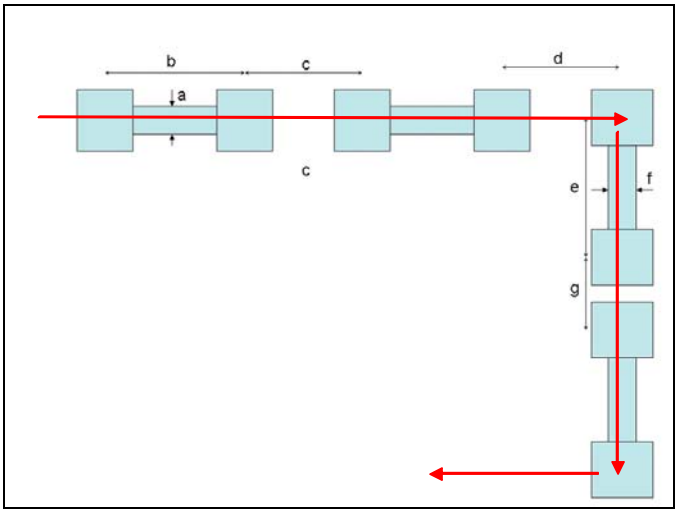

Figure 3: Via stub stitch pattern. Squares indicate stacked via stub. Rectangles indicate stitch connections from one stub to the adjacent stub. Current path is shown by red arrows

Based on the description in Figs. 2 and 3 and the relevant dimensions, the calculated electrical resistance of the stitch pattern is 2.48ohms. The measured resistances using the 4-wire technique was 2.45 and 2.24 ohms respectively.

A sample of the test vehicle (TV) was subject to joule heating experiments. The TV was fixtured vertically inside a closed enclosure (cubical plexiglass box) of side 300mm. The closed enclosure ensured that room air did not interfere with the natural convection currents. Controlled electric current (DC) was supplied to the top and bottom stitch pattern and the surface temperature of the TV was measured until (upto 30minutes) steady state was reached. Due to the small size of the features and to avoid conduction losses, a thermocouple was not used to monitor temperature. Instead,

an IR camera was used to map the TV surface temperature through a window in the plexiglass enclosure. The average surface temperature of the TV was documented. While the local hot spots near the stitches were visible, it was not possible to determine the local maximum.

A thermal model of the experiment was constructed in IcePAK™. The model took into account the geometry features and heat generated. Both natural convection and IR radiation effects were included. Figure 4 shows the thermal resistance and temperature rise of the TV as a function of the joule heating current. In the context of the TV experiment, the following is noted:

(1) Even though the current values are small (<0.35A), due to the fact that the current flows in all the vias, it is equivalent to 250 (the total number of vias in the TV) times the value indicated on the x-axis.

(2) There is not active cooling of the TV. It is merely cooled by natural convection and IR radiation. In a chip package, the vias are connected to the chip. So, the temperature rise is expected to be smaller.

(3) The heat generated in the TV is about 0.77W at 0.35A (equivalent to 88A in parallel). This is two orders of magnitude smaller than the expected heat dissipated in a chip that is supplied with this current assuming a core voltage of 1V.

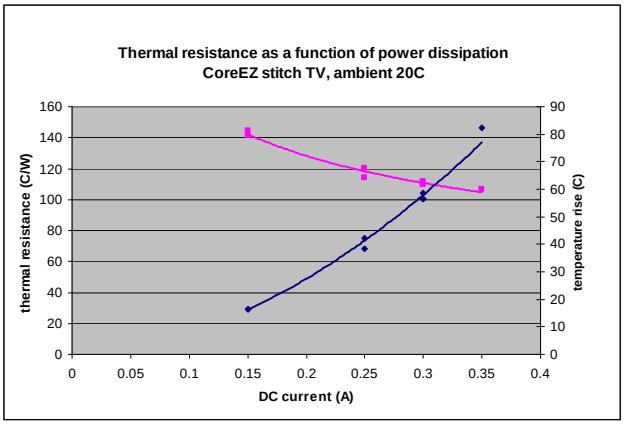

Figure 4: Experiment data showing temperature rise (diamonds) and thermal resistance (squares) as a function of joule heating current

The table below shows the modeling results for the temperature rise as a function of the current. Excellent agreement with experiment data is obtained for the average temperature. The localized hotspots undergo about a 10-15% higher temperature rise.

Current (A)	Measured temperature (C)	Model with uniform heating (C)	Model with local effects included (C)
0.15	26	26	27
0.25	38	41	44
0.3	57	58	65
0.35	83	83	94

NUMERICAL STUDY

Using the numerical model validated in the previous section, simulations were performed under the boundary conditions relevant to a high powered chip package on a PWB. It is implicitly assumed that the heat sink attached to the package is in the primary cooling path. Figure 5 shows a schematic of a flip-chip package showing the overall thermal management scheme. For the purposes of this study, current carrying vias in three zones are considered as described below:

1. Zone 1 is directly under the chip shadow. This zone has a direct cooling path to the package thermal solution (the heatsink).
2. Zone 2 is not under the chip shadow and is near the periphery of the package where a stiffener or an integral lid contacts the substrate for additional support.
3. Zone 3 is in the potentially "exposed" region between Zones 1 and 2. It is least desirable to place vias in this zone because there is not direct cooling path to the package thermal solution. Later in the study, schemes to mitigate this concern will be discussed.

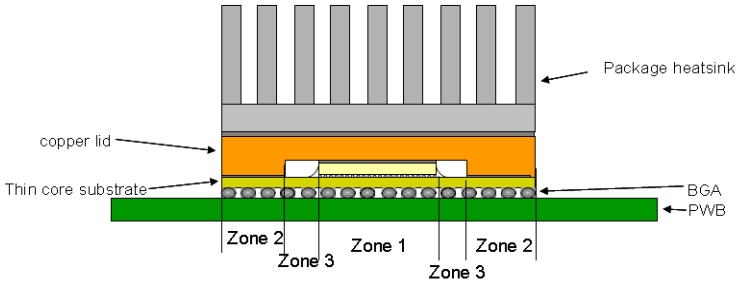

Figure 5: Schematic of a package, PWB and heatsink showing the three zones for via placement.

Simulations were performed for vias in the three zones detailed above. Appropriate boundary conditions were assigned as shown in Figs. 6a,b,c. Although one via chain is shown in Figs.6, a variety of scenarios with single and multiple parallel via chains were investigated. A brief description of the zones and boundary conditions is given below.

In zone 1, both the top and bottom of the substrate are assumed to be at the chip temperature. This may not be entirely realistic for the bottom of the substrate, but it is conservative in most situations.

In zone 2, the top of the stiffener (upper boundary) and the bottom of the substrate (lower boundary) are at the chip temperature. These are both conservative conditions in most situations

In zone 3, the bottom of the lid (upper boundary) and the bottom of the substrate (lower boundary) are at the chip temperature.

Under these boundary conditions, the temperature rise of the vias in zones 1,2, and 3 above the chip temperature is computed.

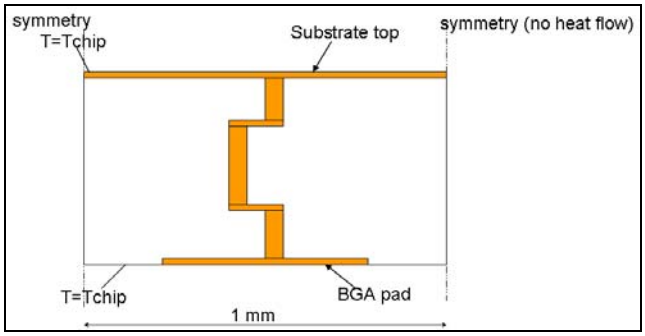

Figure 6a: Boundary conditions and domain size for via current simulations in Zone 1. A single via chain is shown for illustration only.

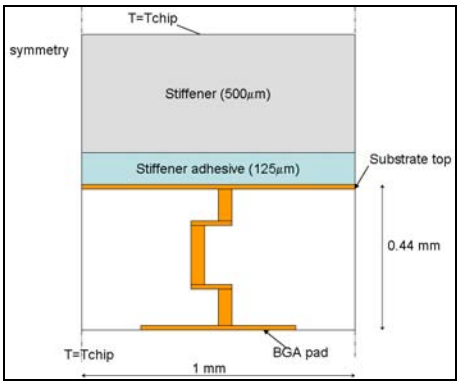

Figure 6b: Boundary conditions and domain size for via current simulations in Zone 2. A single via chain is shown for illustration only.

Figures 6a,b,c also show the dimensions of the domain. In all cases, the substrate thickness is 0.44mm. In the planar directions, a domain size of 1mm is used. The implicit assumption here is that in the high density region of power/ground vias, every adjacent BGA pad has either voltage or ground assignment. Consequently, a symmetry (thermally insulated) condition along the four sides is the most appropriate condition. For all simulations, the following properties are assumed

Material	**Thermal Conductivity(W/m-K)**	**Electrical resistivity(ohm-m)**
Copper	395	2.06e-8
Dielectric	0.4 (outer core, buildup)	
Dielectric	0.2 (inner core)	

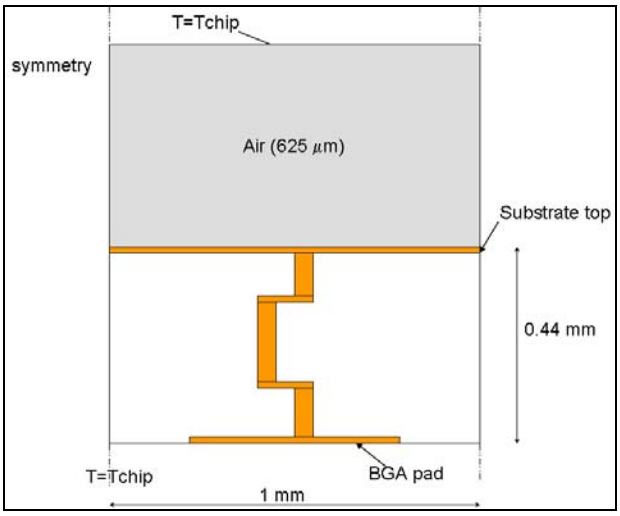

Figure 6c: Boundary conditions and domain size for via current simulations in Zone 3. A single via chain is shown for illustration only.

Figure 7 shows the temperature contours for the base case via arrangement per Table 1. Based on the ratio of vias at every level of the substrate, for every BGA pad, there is/are

a) one via at the lowest level (Bu2b to BGA)
b) one via at the next level (Bu2b to Bu1b)
c) three vias at the next level (Bu1b to Cl4)
d) six vias to from next level to the top (Cl4 to Top)

The temperature rise in Fig. 7 is for 1A of current. The via location is in Zone 1 (Fig. 6a). Wherever there are parallel paths for current, it is assumed that the current is divided equally in each path. The prediction for the situation in Fig.7 (Table 1) is a 0.1C temperature rise. Consequently, for a 10C rise above the chip temperature, the current flow in the via chain needs to be about 10A.

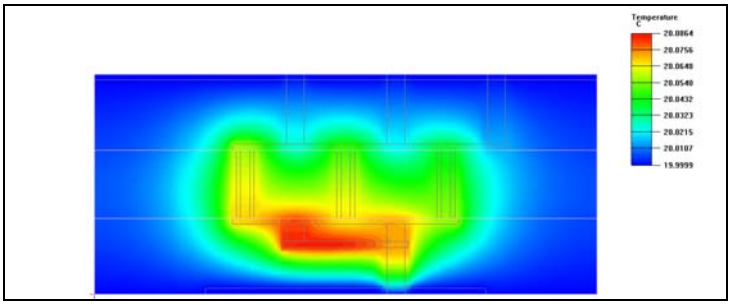

Figure 7: Simulation results for base case via arrangement (per Table 1) in Zone 1.

In order to better understand the parameters affecting the extent of substrate heating, a parametric study was performed by varying the number of vias in the unit cell. Figures 8 and 9 show the temperature contours for a single via chain in zones 1 and 2 respectively. To clarify, a single via chain means that there are no parallel paths for current flowing from BGA pad to flip chip pad.

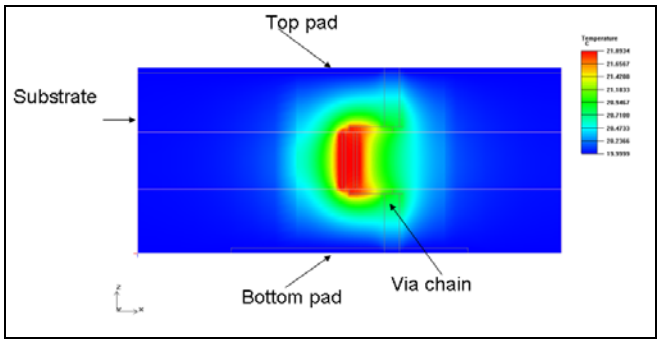

Figure 8: Simulation results for current flowing in a single via chain in Zone 1 (per Fig. 6a)

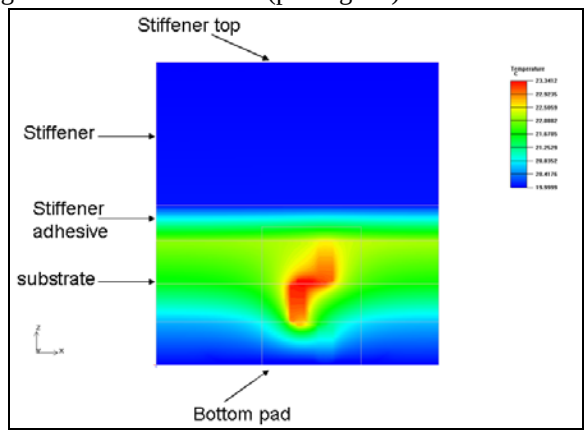

Figure 9: Simulation results for current flowing in a single via chain in Zone 2 (per Fig. 6b)

Based on the above simulation results (Figs.8,9), for a 10C rise of the via above the chip temperature, the maximum current is 2.23A if the via is under the chip shadow (zone 1), and 1.7A if the via is under the stiffener shadow (zone 3). The via temperature rise is higher in zone 3 because of the relatively lower thermal conductivity of the stiffener adhesive material. A higher thermal conductivity adhesive will improve the current carrying capacity of vias in zone 3. In addition, a number of simulations were performed under different conditions to predict the via temperature heat up. These results are given in Table 2. In each case, the maximum via current for a 10C rise in via temperature is given.

Table 2: Current carrying capacity of vias for 10C rise

Via configuration (BGA to flip chip bump pad)	**Via location**	**Current for 10C temperature rise (A)**
Base case per table 1	Zone 1	10 A
Single via chain	Zone 1	2.25 A
Two via chain	Zone 1	4.45 A
Four via chain	Zone 1	8.9 A
Single via chain	Zone 2	1.7 A
Single via chain	Zone 3	1.5 A
Single via chain (thermal interface filling air gap)	Zone 3	1.85 A

The results in Table 2 were obtained with similar boundary conditions as described in Figs.6. The minimum via pitch of 200μm was maintained for the two via and the four via simulations. It is noted that for the two and four via chains, the temperature rise scales linearly with the current supplied. That is, if a single via chain can supply 2.25A, a four via chain can supply almost four times that current (8.9A). The important finding is that at that via pitch, the interaction between adjacent via chains is negligible. The results in Table 2 can be extended to other situations. For e.g., a four via chain in Zone 2 will have a current limit of about 6.8A (four times the single via limit).

The results in Table 2 can also be scaled for a different temperature rise (for e.g. 5C instead of 10C). This is done by recognizing that for a 5C rise, the heat dissipated is one half of that for a 10C rise. Consequently, the maximum current is $(1/\sqrt{2})$ of the value for a 10C rise. This is because heat dissipation which is linear with temperature rise varies as the square of current (I^2R).

SUBSTRATE CURRENT CARRYING CAPACITY

The results in Table 2 give the current for a 10C maximum rise in via temperature. From these results, it is possible to estimate the current carrying capacity of the entire substrate. The results can also be used to "budget" the number of vias per BGA ball based on the current delivery requirement. Alternately, depending on the fabrication capability of the substrate, the right number of BGA assignments can be made for the expected current delivery.

In most high power situations, current is supplied from the PWB to BGA locations directly under the chip (zone 1). However, if the current demand cannot be met by vias under the chip alone, it might be necessary to include BGA locations in zones 2 and 3. For the example configuration in Table 1, there are 176 power/ground BGA locations under the chip. Assuming a 1:1 voltage/ground split and further assuming that two-thirds of the voltage connections are high current ones, a total of 58 BGA locations are available for current delivery. Based on the results in Table 2, for this configuration 580A can be supplied with a 10C via temperature rise. However, if a single via configuration is used, only about 130A can be supplied for the same BGA assignments. For a two via chain, this number rises to about 260A. It should be noted that by utilizing vias in zones 2 and 3 additional current can be delivered, as needed.

Figure 10 is an attempt to quantify the chip power density that can be supported by the substrate technology when current delivery is taken into account. In making these calculations, the following are assumed:

1. Only under-chip BGA locations are used to deliver power.
2. The number of BGA locations scales according to the square of the chip size. The base value being 58 for a 16mm chip.
3. The core voltage is 1V

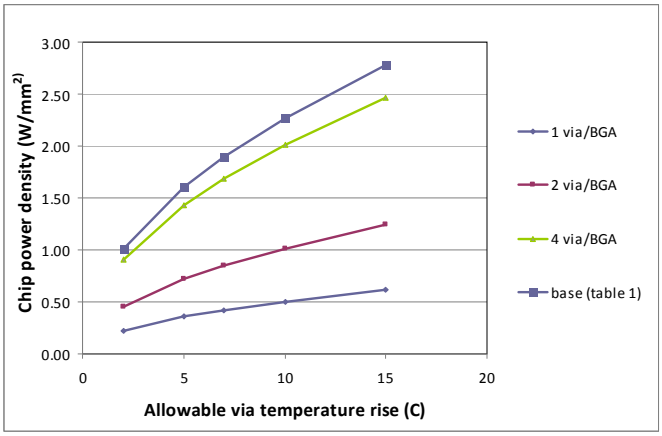

Figure 10: Allowable chip power density based on substrate current delivery as a function of via temperature rise. Core voltage of 1V is assumed.

It is noted that the results in Fig.10 should be treated as guidelines and not as limits. However, it does provide a good starting point in estimating the via configuration that is required to handle a certain chip power density

CONCLUSIONS

This paper presents a study of the current carrying capacity of a high electrical performance, thin, highly dense build-up organic package. Conservative assumptions for boundary conditions are used so that the results can be applied for a number of applications. It is shown that significant amounts of current can be supplied to high power chips without causing the substrate to heat up significantly (<10 C). For a 16mm chip assembled to a 42.5mm package, more than 500A can be delivered using a realistic via configuration in a 2-4-2 substrate. The results presented can also be extended based on the via configuration, changes in allowable temperature rise, and number of BGA locations available for current delivery. Finally, the results are presented in terms of the power density (W/mm^2) that the substrate technology can support as a function of the allowable temperature rise (Fig. 10).

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