PCB DYNAMIC COPLANARITY AT ELEVATED TEMPERATURES

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ABSTRACT
With the advent of larger packages and higher densities/pitch the Industry has been concerned with the coplanarity of both the substrate package and the PCB motherboard. The iNEMI PCB Coplanarity WG generated a snapshot in time of the dynamic coplanarity of several PCB designs from four market sectors. This paper address's the question as to whether room temperature coplanarity measurements can predict the coplanarity at Lead-Free assembly temperatures. This paper investigated the trends in dynamic coplanarity between market sectors, board thickness and global versus local area of concern measurements. It also shares the learning and issues of undertaking dynamic coplanarity measurements of PCB motherboards.

INTRODUCTION
In Q3, 2008 iNEMI initiated the SMT Coplanarity project to develop metrologies and recommendations to enable the measurement and specification for board land coplanarity to ensure high quality, high yield SMT processes for current and next generation components and boards.

Several of the reasons/drivers for the establishment of this WG were;

- The current specifications for component lead coplanarity and board bow and twist have not kept pace with the developments in packaging and board technology. Currently some system manufacturers are experiencing poor SMT yields using materials that meet the current specifications.
- The converse is also true. Some of the newest component technologies are hampered as they fail to meet the current component standards; however have demonstrated high yields in SMT assembly.
- It is clear that updated standards are needed that can provide the needed assurance of quality while maintaining the continuous innovation that is basis of the industry.
- New measurement techniques have enabled the measurement of flatness during simulated SMT conditions allowing more relevant standards to be developed.
- Several Standards bodies have already issued standards using these new measurement techniques for components. These standards efforts could be extended to ensure the flatness of system boards as well.

EVALUATE AND ESTABLISH METROLOGY
After various discussions with industry members the team chose to use the Shadow Moiré technique because of its capability to measure warpage from room to elevated temperatures (260°C). This is a known method used in substrate/component coplanarity evaluations and several members of the WG had access to this type of metrology. The following section outlines the equipment and methodology used in this evaluation. A more detailed report of the test methodology is available upon request.

Both the global PCB (large area/full board) and at least two local areas of interest (BGA sites) on each board were measured and analyzed throughout the temperature range.

TEST PROCEDURE

Hardware/Software

Several systems were used to gather data included Akrometrix TherMoiré PS400, AXP, PS600 and PS24 units. A 100 lines per inch (lpi) grating was utilized for the PS400, AXP, and PS600 systems. A 50 lpi grating was utilized on the PS24. The primary impact of using the coarser 50 lpi grating is that the sample to grating distance could be increased without notably compromising the clarity of the ShadowMoiré image. When correlating data between sample test sets, submitted data from any system should include a declaration of the following:

- System Model
- X and Y extents or Field of Vision (FOV) employed
- Grating Pitch
- Spacing from Grating Glass to Sample Surface
- Type of Sample Support, Uniform Area Support (UAS) fixture or 2 parallel support braces (edge support).
- Temperature Profile applied
- Software used for Analysis (TherMoiré v. 2.X or Akrometrix Studio v. 5+)

Sample Prep and Surface Finish

Each sample was purged of any absorbed moisture. Outgassing of any residual moisture could fog the grating glass and compromise multiple data point images. Prior to imaging the samples were kept in either a sealed bag or a nitrogen dry box along with a humidity indicator card (HIC), which demonstrates the proper dryness of the samples inside. Since the moisture/storage history of all samples were unknown, in order to reduce the amount of outgassing the samples were baked for 24 hours at 125°C to insure dryness prior to measurement in the TherMoiré heating chamber. Note that the bake time was increased from 12 to 24 hours in an attempt to decrease outgassing effects causing lost data points. However, the 24 hour bake time did not improve the situation, so a 12 hour bake to remove moisture should be sufficient for future testing.

The ideal surface finish and color for use with the shadow moiré technique is one that is diffuse and white. Such a sample surface will result in the least amount of noise and highest contrast for the moiré fringe pattern. In order to achieve this surface type, a thin layer of high-heat white paint was applied on top of the sample. This coating should be scattered uniformly across the whole sample but still be “semi-transparent” so that surface features are not completely covered (see **Figure 01**).

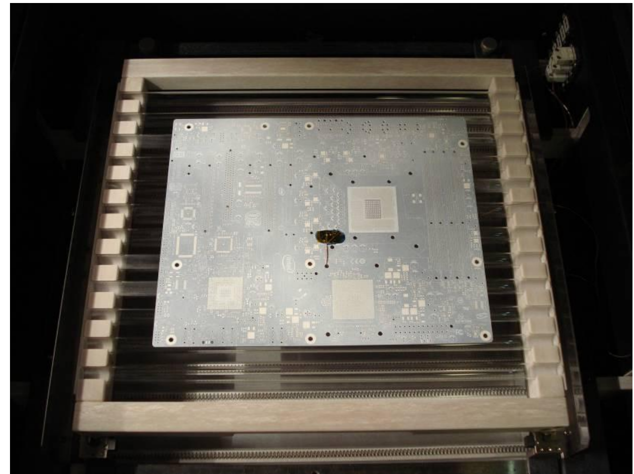


Figure 01 Painted Sample on UAS Fixture

Sample Placement

There was a great deal of early discussion on how to support the PCB’s when measuring at elevated temperature, especially for thinner PCB’s. Since the goal was to model what the dynamic coplanarity is during SMT reflow, supporting the PCB with a jig, pallet, Uniform Area Support (UAS) fixture or other means would prevent sagging at elevated temperatures but may not represent what is truly happening during the reflow cycle. Since the use of pallets during SMT assembly is growing but not universal at this time, the WG decided to model the SMT Assembly process using the two rail edge support method.

Thermocouple Placement

The test method attached one thermocouple to the top surface and multiple thermocouples to the bottom surface of the sample depending on the number of BGA sites to be measured:
Thermocouples were attached to the sample surface using thermal grease and Kapton® tape as described in JEDEC standard JESD22B112

Thermal Profile and Temperature Range of Data

Measurement points were taken from room temperature through the heating cycle to 260 °C and back down through the cooling cycle to room temperature at 20°C increments for a total of 25 measurements.

Three thermal profiles were evaluated in this study. Profile #1 had a heating and cooling rate of approximately 0.3°C/s to better aid in achieving uniform temperatures throughout the board. Profile #2 attempted to more closely emulate a typical temperature profile found in a PCBA production environment. Profile #3 used a soak cycle to bring the PCB to a more uniform temperature prior to recording the measurement. **Figure 02** shows the comparison of the #1 & #3 thermal profiles used in the Industry Snapshot Data. Process 1 is the temperature of the bottom thermocouple and process 2 is the temperature

of the top thermocouple. The results of the warpage magnitude between a continuous ramp temperature profile and a soaking cycle temperature profile on a specific test vehicle is shown in **Table 01.** The coplanarity values were within 3µm of each other for all measured temperature. It was decided by the WG that there was no benefit in having a PCB soak cycle that only added time to the testing process.

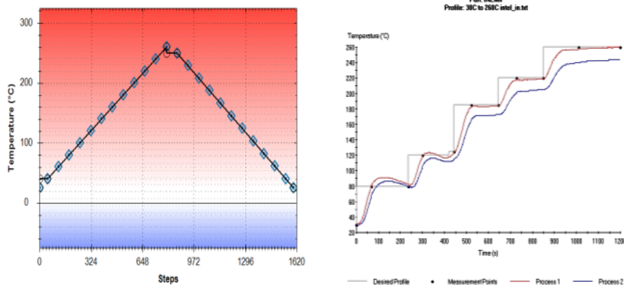


Figure 02: Comparison of 2 thermal profiles

Temperature profile	Measurement Temperature					
	28˚C	80˚C	125˚C	185˚C	220˚C	260˚C
Continous ramp	62 µm	63 µm	66 µm	63 µm	60 µm	60 µm
Soak at measurement	57 µm	60 µm	63 µm	62 µm	58 µm	58 µm

Table 01: Comparison of the warpage measurement between a continuous ramp temperature profile and a soaking cycle temperature profile

Coplanarity Ratio System

Since one of the goals of this project was to establish a correlation between the global PCB warpage and the local BGA site coplanarity, a new gauge, **Coplanarity Ratio**, was used. This allowed for direct comparison of many sizes of BGA and PCB's with this unitless ratio. Figure 03 describes the Coplanarity Ratio as the coplanarity value (um) at any temperature divided by the diagonal length (mm) of the measured area. For example, if a 150 × 200 mm PCB has a co planarity of 1000 microns and a 30 × 40 mm BGA has a co planarity of 200 microns, their co planarity ratios are both 4 microns/mm. Coplanarity ratio can be calculated by mils/inch or microns/millimeter. The calculations of these two cases are presented in the following.

Example of Coplanarity Ratio:

$$1000/\sqrt{150^2+200^2} = 1000/250 = 4(um/mm)$$

$$200/\sqrt{30^2+40^2} = 200/50 = 4(um/mm)$$

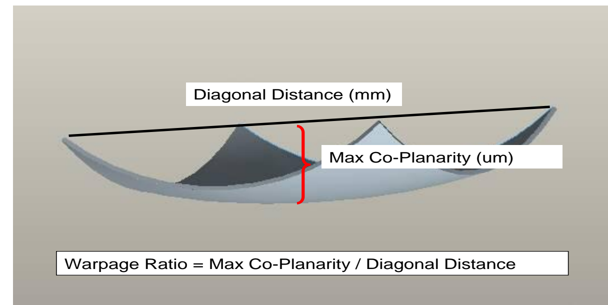


Figure 03: Coplanarity Ratio Diagram

METROLOGY ANALYSIS

PCB Gravitational Deformation

It was found that the thin PCB's and any thick multi-up PCB which had large rout lines would sag or deform under it own weight during the measure cycle using the two rail support system. This was a concern for the WG and should be heavily considered for future testing or process definition. The WG's recommendation is that the support methodology should model the SMT assembly process, but be aware of the effects of heat and gravity on the total board curvature. Fortunately, the Akrometrix systems have algorithms that can compensate for this gravitational sagging. It uses a Least Square Fit algorithm (LSF). The LSF rotation was applied to the data obtained during this project.

The LSF rotation must be applied during analysis to obtain correct co planarity values. Choosing LSF rotation also allows concave or convex shape to be defined as in JEDEC standard JESD22B112 or JEITA standard ED-7306.

LSF (Least Squares Fit) Rotation is a method of orienting the displacement (Z) data measured to remove overall 'slant' of the 3D shape and rotating it so its 'least squares' representative plane is parallel to a common XYZ coordinate system. For this project, the result is that the measured shape is retained, but the angle it sits in the oven is removed so that a 'true' co planarity relative to the measured area itself is obtained**. Figure 04** below illustrates the need for and application of LSF for this project. (Z curvature has been exaggerated for clarity.)

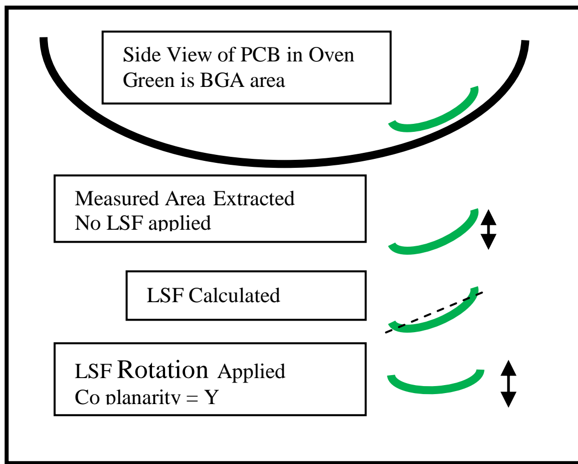


Figure 04: Least Square Fit Rotation method

Outgassing Effects, volatile polymer components

Although global and local data from more than 100 PCBs was collected in this study, for some board designs, vapors from the samples at elevated temperatures coalesced on the grating glass above the samples. **Figure 05** shows that when enough vapor deposited on the grating at any one point, the moiré effect at that point no longer was visible to the TherMoiré's camera, resulting in the loss of that local data point. In some cases, outgassing was so severe, with so much material depositing on the grating the surface could no longer be analyzed and an entire sample measurement at that temperature, for that PCB, was lost.

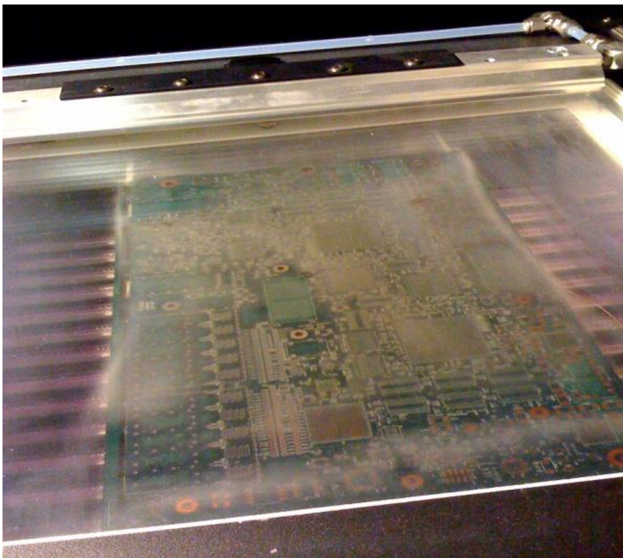


Figure 05 shows the outgassing seen on the grating glass.

The vapors in question are released closer to 250°C, and the increased bake time at 125°C may have reduced the moisture content further but had no noticeable effect on the loss of data points.

The work group tried to increase the grating distance which had no effect. As shown in **Figure 06**, where missing data points result in breaks in some of the plot lines, the best method for eliminating the negative effects of outgassing may be to simply test enough samples that a trend is determined. With multiple samples, any data lost for a single sample has less effect on the overall analysis.

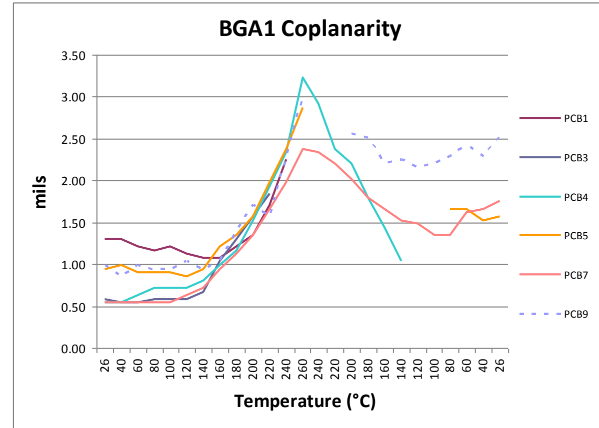


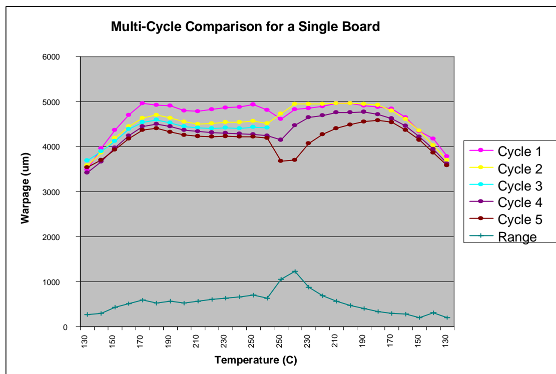
Figure 06: Data loss caused by outgassing of samples

Multiple Thermal Cycle Measurement of a PCB Board

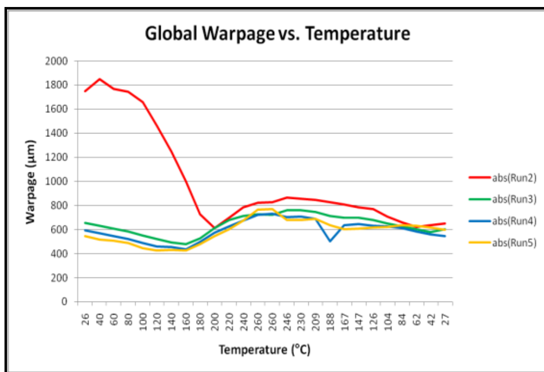
In an effort to understand the best time for the Warpage measurements to occur during the PCB Fabrication through Assembly cycle the WG investigated the effect of multiple measurement cycles. This experiment compared warpage variations of a single PCB board between repeated thermal cycles. PCBs were subjected to 5 TherMoire temperature cycles at 3 different sites with various supports and temperature ramp profiles. The Flextronics Austin and Intel Chandler Austin labs each ran a single PCB using the Max Rate temperature profile while being supported across 2 rails at opposing PCB edges. The Akrometrix Atlanta lab ran a PCB using the 0.3°C/sec while being supported across the Uniform Area Support (UAS) fixture. The rail supports would allow for gravitational sagging as the PCB reaches and exceeds its Tg temperature and softens in rigidity. The UAS provides a more level and planar support across the PCB's surface area.

Testing at all three facilities showed a general trend of warpage reduction that held across multiple temperature cycles for any support condition.

Figure 07 shows that the warpage reduces in magnitude with each subsequent temperature cycle with a large drop in warpage from the first reading and second readings.



2 rail support



Full board support (UAS)

Figure 07: Multi Cycle Warpage vs. Temperature

The UAS supported run implies that once Tg temperature is achieved the soften structure of the PCB can be strongly influenced by the measurement support structure utilized. In this case an initial run impressed gravitational sag that it held upon cooling when it was supported across pair rods during the initial run. Then upon reaching Tg while supported in an UAS fixture the PCB dramatically flattened and remained in that general flattened contour throughout subsequent runs.

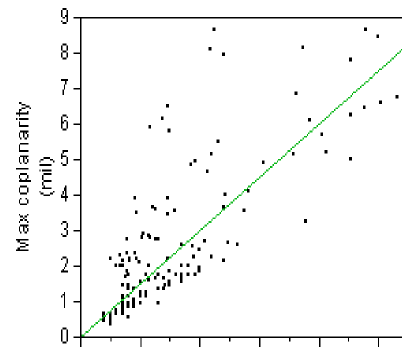
HISTORIC DATA ANALYSIS

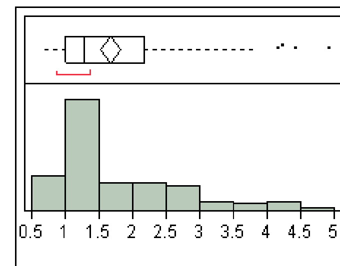
In an attempt to gather as much PCB coplanarity data as possible for this study during the initial phase of the project, the WG collected over a hundred archival coplanarity readings across multiple designs, thickness and layer count PCB's. Because this data was archival, much of the exact configuration and board design/material etc was missing. This historic data is a composite of various materials, BGA sizes, board designs and thicknesses from .032" - .125". It is interesting to note that even with this large but random set of coplanarity samples the results are very similar to the values set in the Phase #2 Industry Snapshot data.

Historic BGA correlation of Initial Room Temperature to Maximum Coplanarity.

One focus of the WG was to answer the question if Room Temperature Coplanarity could be used to predict the Dynamic Coplanarity at Temperature. In order to analyze the relationship of Room Temperature Coplanarity to Maximum Coplanarity the WG decided to graph all the Room Temperature and Maximum Coplanarity BGA data points available and fit a linear trend line to the results. **Figure 08** shows the correlation between Room Temperature and Maximum coplanarity for the historic data set.

The overall trend shows that the Maximum Coplanarity for all the Historic data analyzed is **1.67** times the room temperature coplanarity. Note: The Historic data is raw coplanarity values in mils, not the coplanarity ratio used in Phase #2.





Moments	
Mean	1.6734906
Std Dev	0.9057082
Std Err Mean	0.0776638
Upper 95% Mean	1.8270857
Lower 95% Mean	1.5198954
N	136

Figure 08: Historic data showing the relationship of Maximum to Room Temperature BGA Coplanarity

INDUSTRY SNAPSHOT

Once the WG had developed the measurement methodology they decided to get a Snapshot in time (2011) of what the coplanarity of BGA and PCB's are for real product in the market place. They focused on four market segments, Desktop, Notebooks, Workstations and High End Servers. These unassembled product PCB's were obtained from various OEM/ODM's in the industry. The WG measured 10 PCB with 2 BGA per PCB from each lot. The following data is from this dataset and utilizes the Coplanarity Ratio for analysis. This section analyzes the series of questions raised in the SOW during project formation.

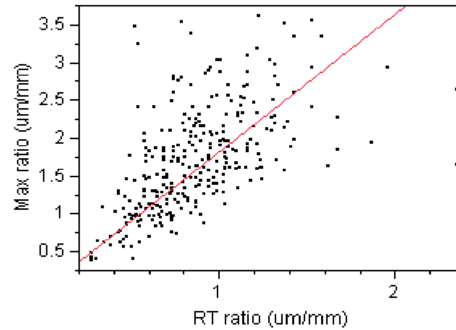
Can the Room Temperature Coplanarity predict the Maximum Coplanarity?

Figure 09 shows the BGA correlation of Initial Room Temperature to Maximum Coplanarity. To better understand the initial room temperature to maximum coplanarity relationship the WG divided the maximum coplanarity ratio by the room temperature ratio. The overall trend shows that the Maximum Coplanarity for all the Industry Snapshot data analyzed is **1.93** times the room temperature coplanarity. This Snapshot data is a composite of various materials, BGA sizes and board designs from the four market sectors under evaluation. Although the Historic data was in raw coplanarity numbers it is interesting to note that the Maximum Coplanarity correlation was **1.67** times the room temperature coplanarity.

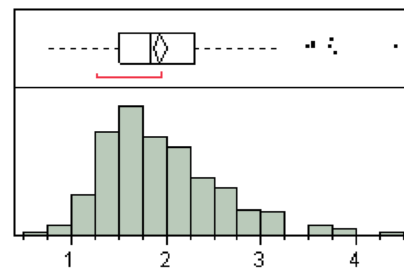
Table 02 shows that the individual lot results may be design dependent. The thicker and higher layer count boards have lower Max/RT ratio's than the thinner Desktop and Notebook designs. It is also interesting that the variation within a market sector can be quite large, as shown by both the Notebook and Desktop data. Although the sample size of the lots within these market sectors is small, it is does raise the questions concerning what is it about the design of these boards that lead to the various warpage values since the size, thickness and layer counts were very similar within the market sector. NOTE: The WG believes that this is an important area for further study and understanding.

The WG found that multiplying the Room Temperature Warpage by 2X will give a fairly good prediction the Dynamic Maximum Warpage for any BGA size. This rule of thumb holds well for all market sectors analyzed.

The WG believe that the use of the 2X multiplier on any Room Temperature warpage data will allow for Elevated Temperature prediction or process control within a reasonable tolerance. If a more precise ratio is desired for any specific design, the data set evaluated showed that using the Dynamic Warpage Methodology found in Appendix 1, to measure 25-30 boards per design over several fabrication lots is sufficient to generate a design specific Room Temperature to Maximum Warpage ratio at a 90% confidence level. This number can then be used for a more precise predictive value of Elevated warpage from Room Temperature measurements.



Distribution of Max/RT ratio



Moments

Mean	1.9315938
Std Dev	0.5946793
Std Err Mean	0.0351028
Upper 95% Mean	2.0006864
Lower 95% Mean	1.8625011
N	287

Figure 09: BGA data showing the relationship of Maximum to Room Temperature Coplanarity

Table 02: Maximum Warpage divided by initial Room Temperature Warpage (means + 3 sigma).

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
Notebook Sector	2.30	3.33
SNB0210	2.23	3.23
SNB0310	2.44	3.35
TNB0110	2.02	1.86
VNB0110	1.92	1.46
VNB0210	1.43	1.44

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
Desktop Sector	2.09	1.82
ADT0110	2.69	1.49
EDT0110	1.82	1.81
NDT0110	1.95	1.81
TDT0110	1.42	1.53

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
HE Server Sector	1.44	1.72
HSE0110	1.29	1.90
CSE0210	1.74	1.83
CSE0110	1.46	1.49

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
WS Server Sector	1.94	2.07
CSW0205	1.23	1.16
CSW0305	1.76	2.00

Can one board/BGA measurement predict the warpage of the lot?

This question is of particular interest as the dynamic measurement method is a lengthy and costly analysis. Additionally, the test method exposes the PCB to a thermal excursion which could adversely affect long term reliability.

To help answer this question the WG looked at the variability in the measurements between boards in a lot. **Table 03** shows the board variance within a lot as a % of the mean value (3σ/mean) for the measured features throughout the thermal profile range. Measurements demonstrating a variance > 50% has been highlighted as a means of visually understanding the variability within that lot/market sector.

Looking at the data with the 50% threshold we find all 4 market segments show designs with high within a lot variance. In fact the Notebook market segment is the only segment to have any designs that almost pass this threshold.

Based on the 50% variance threshold (chosen by the team) we concluded that a measurement from a single PCB would be a poor representation of an entire lot. It would be up to the individual company to decide on an acceptable variability threshold and re-evaluate based upon their application or requirements.

The team believes that this variability reflects the effects of the manufacturing process since the design and materials were held constant within each lot.

Table 03: Variation within a lot (3 sigma/means)

Workstation	% Warpage Ratio Variability within a Lot (3 Standard Deviation/Average)								
	CSW0110			CSW0205			CSW0205		
Temp	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global
26	40%	42%	73%	62%	31%	86%	58%	91%	59%
40	54%	46%	67%	68%	36%	75%	70%	36%	58%
60	45%	31%	57%	80%	33%	62%	106%	50%	44%
80	64%	52%	55%	82%	47%	52%	83%	59%	40%
100	56%	50%	63%	45%	28%	44%	85%	66%	38%
120	51%	48%	72%	57%	31%	42%	76%	48%	44%
140	70%	51%	74%	62%	37%	49%	97%	51%	50%
160	50%	50%	65%	65%	37%	40%	91%	101%	78%
180	46%	63%	46%	70%	33%	41%	120%	80%	35%
200	46%	40%	50%	69%	36%	38%	119%	79%	56%
220	53%	59%	50%	57%	26%	35%	77%	76%	69%
240	71%	139%	46%	51%	18%	37%	63%	45%	52%
260	90%	202%	26%	51%	35%	49%	70%	51%	73%
240	55%	152%	26%	27%	36%	39%	95%	96%	91%
220	51%	104%	37%	49%	30%	46%	80%	70%	81%
200	70%	102%	25%	59%	37%	36%	84%	85%	69%
180	86%	114%	29%	44%	53%	42%	119%	84%	51%
160	64%	130%	16%	35%	34%	33%	156%	110%	44%
140	67%	142%	45%	16%	40%	50%	124%	77%	38%
120	46%	154%	41%	45%	37%	37%	92%	123%	36%
100	85%	211%	39%	46%	51%	33%	79%	106%	37%
80	102%	165%	68%	46%	53%	42%	105%	86%	35%
60	87%	197%	53%	43%	61%	37%	55%	53%	31%
40	97%	177%	34%	58%	69%	39%	101%	87%	39%
26	48%	61%	57%	74%	57%	41%	93%	108%	39%

Notebook	% Warpage Ratio Variability within a Lot (3 Standard Deviation/Average)														
	SNB0210			SNB0310			TNB0110			VNB0110			VNB0210		
Temp	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global
26	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
40	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
60	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
80	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
100	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
120	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
140	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
160	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
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200	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
220	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
240	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
260	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
240	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
220	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
200	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
180	24%	22%	42%	51%	65%	2%	29%	37%	25%	57%	28%	66%	112%	161%	20%
160	10%	22%	38%	51%	55%	17%	32%	40%	24%	47%	16%	67%	133%	159%	19%
140	19%	25%	40%	45%	43%	27%	29%	36%	22%	59%	24%	67%	135%	160%	22%
120	21%	21%	42%	57%	51%	24%	29%	35%	23%	54%	23%	62%	79%	160%	16%
100	14%	19%	40%	71%	55%	31%	29%	37%	25%	59%	28%	60%	111%	161%	13%
80	15%	22%	37%	60%	42%	20%	28%	34%	21%	58%	29%	55%	127%	161%	19%
60	20%	31%	36%	61%	45%	33%	22%	35%	19%	49%	28%	50%	109%	161%	20%
40	27%	22%	35%	42%	47%	32%	22%	33%	19%	54%	25%	53%	137%	160%	19%
26	30%	26%	33%	33%	37%	12%	32%	38%	25%	65%	22%	53%	84%	22%	16%

Desktop	% Warpage Ratio Variability within a Lot (3 Standard Deviation/Average)											
	ADT0110			EDT0110			NDT0110			TDT0110		
Temp	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global	BGA 1	BGA 2	Global
26	102%	54%	66%	76%	51%	59%	55%	58%	100%	62%	89%	105%
40	102%	55%	37%	87%	42%	60%	58%	62%	96%	56%	75%	98%
60	92%	54%	41%	109%	52%	72%	57%	56%	97%	48%	93%	102%
80	78%	53%	45%	114%	54%	72%	51%	52%	98%	56%	84%	103%
100	80%	48%	46%	98%	54%	79%	55%	53%	101%	53%	79%	108%
120	68%	44%	44%	87%	45%	81%	51%	47%	106%	40%	78%	101%
140	44%	35%	44%	86%	48%	83%	61%	56%	110%	45%	76%	92%
160	37%	40%	61%	70%	47%	75%	53%	28%	103%	54%	75%	94%
180	40%	38%	72%	82%	42%	78%	50%	41%	96%	41%	78%	91%
200	36%	43%	93%	60%	36%	58%	58%	32%	93%	47%	57%	83%
220	29%	57%	109%	73%	51%	57%	67%	36%	104%	47%	56%	75%
240	32%	59%	84%	84%	36%	60%	58%	50%	110%	46%	59%	73%
260	38%	68%	33%	103%	45%	65%	67%	56%	105%	55%	65%	68%
240	47%	59%	60%	111%	72%	48%	73%	73%	106%	48%	79%	89%
220	17%	84%	63%	85%	69%	40%	45%	127%	84%	46%	64%	94%
200	36%	84%	70%	80%	74%	35%	66%	81%	73%	33%	92%	94%
180	61%	79%	74%	81%	59%	33%	76%	129%	60%	38%	73%	85%
160	67%	69%	90%	40%	50%	31%	58%	58%	54%	55%	100%	76%
140	114%	71%	93%	45%	41%	31%	67%	58%	57%	50%	88%	70%
120	79%	84%	97%	42%	45%	29%	99%	85%	107%	51%	81%	78%
100	102%	53%	64%	32%	41%	31%	94%	111%	121%	31%	70%	71%
80	82%	51%	86%	37%	32%	29%	119%	127%	148%	26%	69%	67%
60	72%	61%	78%	21%	29%	23%	65%	73%	54%	27%	58%	69%
40	67%	65%	74%	33%	30%	21%	53%	66%	68%	35%	56%	74%
26	80%	79%	70%	19%	31%	26%	100%	75%	97%	60%	71%	86%

Hi End Server	% Warpage Ratio Variability within a Lot (3 Standard Deviation/Average)											
	HSE0110				CSE0210				CSE0110			
Temp	BGA 1	BGA 2	BGA 3	Global	BGA 1	BGA 2	BGA 3	Global	BGA 1	BGA 3	BGA 2	Global
26	76%	212%	99%	104%	105%	84%	95%	146%	96%	115%	97%	100%
40	71%	187%	116%	98%	105%	84%	87%	175%	130%	52%	71%	60%
60	154%	177%	159%	80%	101%	91%	69%	169%	117%	63%	65%	66%
80	120%	178%	119%	76%	95%	85%	79%	143%	133%	56%	73%	70%
100	87%	249%	121%	65%	105%	86%	84%	111%	117%	56%	68%	52%
120	75%	255%	139%	61%	77%	86%	86%	89%	85%	140%	96%	65%
140	75%	237%	112%	54%	102%	69%	74%	97%	170%	77%	61%	58%
160	86%	189%	129%	68%	104%	94%	104%	138%	79%	121%	40%	57%
180	86%	179%	119%	70%	101%	139%	53%	119%	89%	159%	124%	62%
200	88%	177%	120%	81%	97%	90%	66%	123%	143%	94%	81%	90%
220	88%	180%	101%	85%	115%	115%	91%	123%	160%	114%	56%	65%
240	116%	146%	119%	77%	163%	87%	94%	127%	135%	128%	49%	74%
260	122%	148%	93%	76%	134%	80%	88%	129%	92%	99%	72%	63%
240	85%	140%	125%	46%	160%	79%	101%	160%	133%	132%	138%	58%
220	142%	229%	185%	60%	107%	89%	104%	161%	90%	147%	65%	62%
200	69%	160%	113%	69%	185%	95%	140%	172%	80%	135%	137%	52%
180	86%	171%	129%	68%	143%	101%	110%	188%	112%	137%	63%	48%
160	106%	164%	104%	66%	147%	76%	159%	179%	98%	114%	57%	60%
140	131%	138%	136%	70%	150%	83%	123%	192%	68%	130%	135%	84%
120	103%	183%	108%	69%	146%	87%	115%	192%	77%	103%	71%	54%
100	121%	178%	123%	53%	125%	91%	172%	191%	102%	110%	94%	64%
80	120%	187%	127%	48%	143%	104%	166%	192%	102%	105%	48%	50%
60	88%	190%	124%	43%	134%	89%	181%	199%	79%	133%	72%	52%
40	92%	180%	139%	46%	114%	90%	86%	197%	103%	105%	83%	53%
26	107%	207%	96%	47%	94%	91%	101%	199%	138%	129%	74%	55%

Can one BGA size predict another BGA size coplanarity on a board?

The WG was unable to find neither a correlation based on the data set nor any statistical correlation between the BGA Coplanarity and the Diagonal length. **Figure 10** shows the composite graph of the Maximum BGA Coplanarity as a function of BGA diagonal length for all BGA's. The data did not show a hard correlation between BGA sizes. There seems to be another factor that affects coplanarity other than just the BGA size.

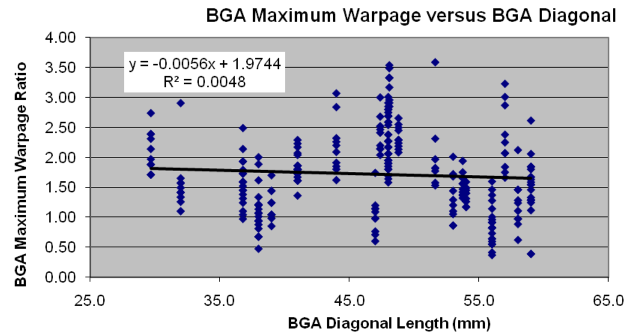

Figure 10: BGA maximum Warpage as a function of BGA diagonal length

Local Area of Interest (BGA) Vs. Global Relationship:

The Local Area of Interest (BGA) is the most important area to the SMT process. Both Room Temperature and Dynamic Coplanarity are important since they affect both the ability to screen the solder paste and the formation of the solder joint. The Global warpage value is more important for processing whole boards through equipment and installation into racks while the Solder Joint formation is more dependent on the BGA/Local Area of Interest Coplanarity.

Table 04: Coplanarity Ratio Values for all Market Sectors and Lots (Means + 3 STD)

	Average Warpage Ratio in um/mm			
	BGA		Global	
	RT	Maximum	RT	Maximum
Notebook Sector	**1.64**	**3.78**	**7.22**	**24.03**
SNB0210	2.13	4.75	5.49	17.74
SNB0310	1.23	2.99	6.96	23.35
TNB0110	1.54	3.11	6.81	12.67
VNB0110	1.74	3.35	7.80	11.37
VNB0210	1.74	2.48	6.14	8.86

	Average Warpage Ratio in um/mm			
	BGA		Global	
	RT	Maximum	RT	Maximum
Desktop Sector	**1.79**	**3.75**	**5.77**	**10.52**
ADT0110	1.39	3.75	3.90	5.80
EDT0110	1.87	3.40	4.17	7.54
NDT0110	1.89	3.69	7.57	13.71
TDT0110	1.38	1.96	4.52	6.94

	Average Warpage Ratio in um/mm			
	BGA		Global	
	RT	Maximum	RT	Maximum
HE Server Sector	**1.81**	**2.62**	**2.30**	**3.96**
HSE0110	2.18	2.81	1.05	2.00
CSE0210	1.18	2.06	1.17	2.14
CSE0110	1.81	2.64	1.42	2.12

	Average Warpage Ratio in um/mm			
	BGA		Global	
	RT	Maximum	RT	Maximum
WS Server Sector	**1.80**	**3.48**	**1.92**	**3.98**
CSW0205	1.92	2.37	1.61	1.88
CSW0305	0.85	1.50	1.93	3.86

Table 04 shows that there is less variability in BGA coplanarity between the market sectors than for the Global warpage Even with a large Global warpage seen with the Notebook & Desktop sector, the BGA areas were relatively flat and consistent across the market sectors.

Temperature of Max Deformation:
The Max deformation did not always occur at the highest temperature or at any one temperature for all the lots/market sectors. **Figure 11** shows that each market sector had a distinct signature at which temperature the maximum deformation/warpage occurred. It should be noted that the slight skew of the Notebook (NB) data was caused by truncating the data at 180°C. The Global and the BGA areas do not always experience the max deformation at the same temperature

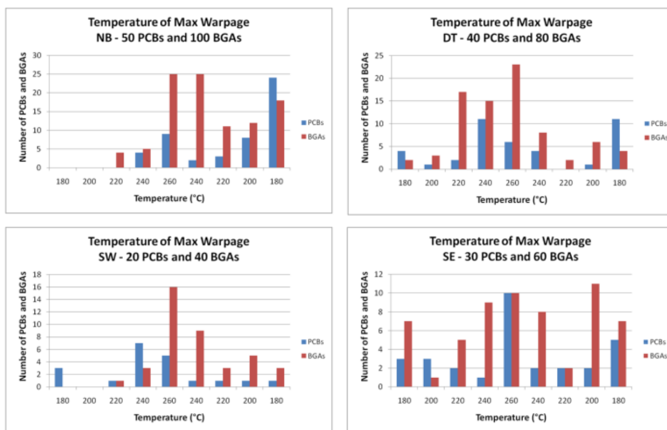

Figure 11: Temperature of Maximum Warpage for the four market Sectors

CONCLUSIONS

Test Method:
Shadow Moiré is a viable test methodology for determining coplanarity values at elevated temperatures.

The heating and cooling rates do not greatly affect the coplanarity values within the heating rates used in the test.

Using a soak cycle did not significantly improve or change the coplanarity value at any specific temperature.

Outgassing of the PCB can occur at elevated temperatures that can affect the ability to measure the PCB. Multiple PCB's are required to get an average value that mitigates the loss of any individual PCB or temperature range.

Simulating the planned assembly set-up/reflow carrier is necessary to get a valid coplanarity value. The use of rails during measurements can introduce sag into the PCB and using a full PCB support /pallet can reduce the sag but may introduce a non real situation or coplanarity value.

Data Analysis:
Multiple thermal passes resulted in a reduced coplanarity value with each pass, especially during the first three passes.

Although there were considerable outliers in the data set, the relationship of Maximum to Room Temperature warpage can be approximated by a factor of 2X the Room Temperature value.

Thinner PCB's have higher warpage or coplanarity values than thicker PCB's.

Design of the PCB/BGA area appears to be the largest factor in coplanarity within a market sector. Thickness and layer count are less important, except for their design/copper distribution effects.

The variance within a single lot of PCB's is often over 50% making the use of one measured PCB/BGA to precisely predict the lot difficult.

There is no trend of increasing coplanarity ratio with increased BGA size for any of the market sectors, and there are always outliers. The ability to predict one BGA's coplanarity using another BGA of a different size is difficult.

The maximum warpage did not always occur at the maximum temperature and the temperature for maximum warpage for the BGA and Global PCB did not always occur at the same temperature.

RECOMMENDATIONS FOR SMT ASSEMBLY

Warpage Characterization Process:
A characterization study of dynamic coplanarity should be performed on each BGA/local area of interest for each new design including the temperature range from the laminate transition temperature (Tg) up to the peak assembly temperature and cooled to the solder solidus temperature to capture all movement of the BGA/Global areas during the critical times.

Once the characterization study has been completed, measurements of a sample size from each lot's BGA Room Temperature value can be used to predict the Maximum Coplanarity value for that design/lot using this calculated Max/RT ratio.

Coplanarity measurements need to be done within the BGA land area/local areas of interest. It is much harder to predict the effect on coplanarity of the BGA from the Global values.

PCB Warpage/Coplanarity specifications should include both 'Room Temperature Global' and an Elevated Temperature 'BGA Land Area/Local Area of Interest' limits and/or requirements.

Test Conditions:
A slower cycle including soak time is not required for valid measurements, ramping the heating cycle at 0.3°C/sec can accomplish a simulated assembly profile.

All data collection needs to be done on fresh (non-thermal cycled) boards due to the change in coplanarity values brought by each thermal cycle. This will assure the worst case data. Pre-baking to remove warpage-affecting moisture is required.

All Dynamic Elevated Temperature measurements should use the support system (rails or pallets/jigs) based on the method of SMT assembly being used for the PCB. Using a support system like the UAS system developed by Akrometrix is recommended for thin PCB's

Any specification using dynamic elevated temperature will have to address the amount of data loss due to outgassing which would make the reading at that temperature invalid. Averaging over several boards helps with this analysis but can skew the data if too much data is lost with the lot.

Dynamic Warpage Methodology:
OEM/ODM Characterizes the PCB design dynamically across the full assembly temperature range. This may require a design modification if the Maximum Coplanarity exceeds the allowed specification value.

OEM/ODM calculates the Max/RT ratio for use in setting the Room Temperature value

ODM/EMS/CMS/SMT Assembler jointly set a Room Temperature specification for each design from the characterization study in #1. This specification may need to be component specific based (family of parts/components) since the coplanarity requirements maybe vary with BGA package/size.

PCB supplier will measure each lot at Room Temperature (a statistically valid sample size) and report on the Certificate of Conformance (COC).

Measure boards/BGA's from room temperature through the heating cycle to 260 °C and back down through the cooling cycle to room temperature at 20°C increments for a total of 25 measurements.

Support boards in the chamber by the method utilized in the assembly process

Recommended Next Steps
The WG recommends that IPC reviews the Warp & Twist and Bow specification and establishes a Dynamic Coplanarity Ratio for the BGA area or Local area of interest.

The WG recommends that IPC reviews the test methodology for the Warp & Twist and Bow test method and develop one that includes the BGA or Local area of interest.

The WG recommends that IPC and JEDEC form a joint evaluation WG to analyze the Dynamic Coplanarity specification and jointly set the requirements for board and package. Using iNEMI and other consortia data would be advantageous.

The WG recommends a study of the influence of PCB Fabricator on any single design be untaken to quantify the affects of PCB Fabrication/Processes.

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