

Avoiding the Solder Void

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Abstract

Solder voiding is present in the majority solder joints and is generally accepted when the voids are small and the total void content is minimal. X-ray methods are the predominate method for solder void analysis but this method can be quite subjective for non grid array components due to the two dimensional aspects of X-ray images and software limitations. A novel method of making a copper “sandwich” to simulate under lead and under component environs during reflow has been developed and is discussed in detail. This method has enabled quantitative solder paste void analysis for lead free and specialty paste development and process refinement. Profile and paste storage effects on voiding are discussed. Additionally an optimal design and material selection from a solder void standpoint for a heat spreader on a BCC (Bumpered Chip Carrier) has been developed and is discussed.

Introduction

Solder voids in solder joints are a common occurrence in SMT assemblies. Their origins are not well understood but are typically faulted as a failure of the solder fillet to thoroughly expel flux remnants during the reflow process. The amount of solder voiding can vary significantly within an assembly, between different flux formulations, solder alloys, board and component metalizations. Reflow profiles as well as stencil aperture designs can often affect the overall level of voiding.

Adding to the mystery of solder voiding is a lack of quantitative measurement tools in the industry with few exceptions. BGA void analysis software is one of these exceptions. This software uses gray level pixel analysis to determine the perimeter of the solder sphere and the internal perimeters of the voids. Once the perimeters are established the areas within these structures can be measured and an overall percent voiding can be calculated. This type of measurement works well if the voids are large or found on the outer edges of the sphere but if the void is small and centrally located where the sphere density is the greatest then the void may be invisible due to its relatively similar gray level to the surrounding material. Increasing the X-ray power will reveal the small void but also shrink the measured area of the sphere and yield an inaccurate and inflated percent voiding. This problem is even more complicated in a chip or a leaded component solder joint. When X-raying a completed assembly, internal traces, vias and even components on the backside of the board that intersect the image of the solder joint confound the software algorithms ability to accurately determine the perimeter of the solder joint. In simple terms the X-ray image is two-dimensional and the ideal structure must be symmetrical about the Z-axis such as a box or a cylinder.

Novel Approach

Based on the assumption that the ideal quantitative void measurement method will utilize BGA analysis software and a symmetrical Z-axis reflow structure, the “sandwich” concept was developed.

This a novel approach simulates the worst conditions of a solder joint for voiding, under the component where flux evacuation is the most difficult while maintaining the same reflow thermal environment and metallurgies if desired. This idea was born out of a quest for a quantitative method of determining the percent voiding on a Ceramic Column Grid Array (CCGA)¹. In the CCGA the columns are 10/90 Sn/Pb and cover about 45% of the solder fillet. If enough power is used to see through these dense columns, the perimeter of the solder joint is washed out and 55% of the total fillet is invisible. If adequate power is used to see the perimeter of the circular fillet, the area under the columns is invisible. The effort is complicated by column parallax, internal traces and vias as can be seen in Figure 1. With the thought of a column the same diameter as the solder pad that is thin enough to be X-rayed without excessive power, a solder preform was selected. In this application the preform alloy was selected to be the same as the 10/90 columns to minimize the variables that could contribute to solder voiding. Several thicknesses were tested with a 30 mil diameter by 5 mil thick as the final solution.

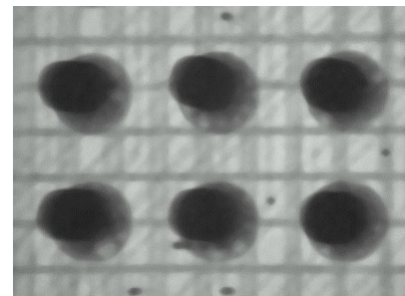


Figure 1 - CCGA X-ray

There were numerous challenges placing these discs. The first problem was a reliable source cup shaped and stacked discs were the first problems to solve. The second problem was the mechanics of actually placing the discs in that the vision systems in the pick and place were never programmed to recognize round components, only components with corners like typical chips. This relegated a “ballistic” pick and place strategy. For this problem a precision matrix tray with cylindrical pockets, each holding one preform, was developed as in Figure 2. Next came improvements to the pick and place nozzle. The stock smallest nozzle OD was the same as the preform. This presented numerous pick problems if the preform was not perfectly centered, occasionally the preform would flip on its edge after pick and crash on placement deforming the preform. Several improvements were made ultimately reducing the nozzle tip down to what would be typical for a 0201 chip as in Figure 3. Reducing the nozzle tip surface area helped eject the preform better in the placement operation.

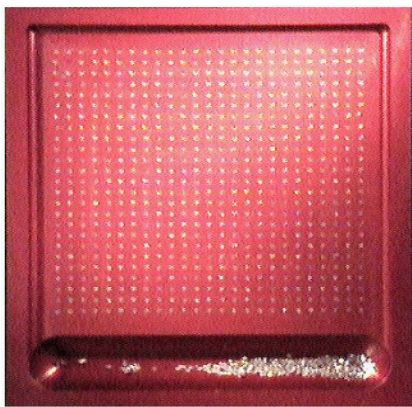


Figure 2 - Pick & Place Tray

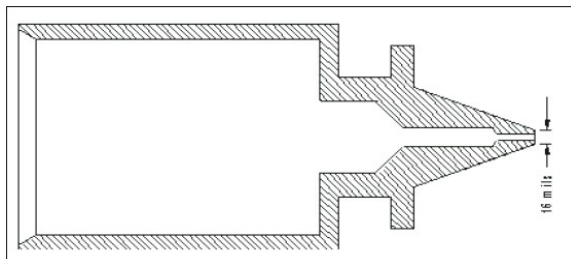


Figure 3 - Custom Nozzle

Assembly of the CCGA test coupons is simple SMT assembly beginning with a “pads only” ceramic coupon to maintain the geometries and pad metalization of the application. This coupon is free of internal traces as in Figure 4. The solder paste is printed through a circular aperture that is 1 mil smaller in diameter than the pad, the preform is placed over the solder paste and then reflowed as in Figure 5. It was established that if the preform was

off pad less than 4 mils that it would self-center. Careful attention to Z-axis placement is required to prevent shorting with adjacent preforms.

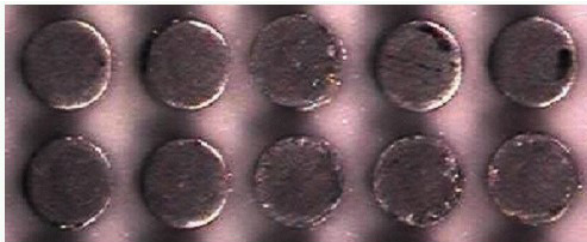


Figure 4 Assembled 10/90 Preforms



Figure 5 - Reflowed Preform Side View

After assembly the coupon area was X-rayed and quantitative void analysis was performed on the image using off-the-shelf BGA analysis software as in Figure 6. This software provides both total percent voiding and a pass/fail status if any individual void within a structure is larger than a preset number (ie 5%). This technique worked very well for the custom formulated 63/37 Sn/Pb based solder paste or any other alloy with a similar melt point but when tested with lead free (Sn/Ag/Cu, Mp 219°C) it was noticed that the preforms had appeared to melt and partially join the underlying solder paste under test. This was remedied by switching to OFHC copper preforms of identical geometries. For generic paste void benchmarking² a dedicated pad test area (Figure 7) was included in the Benchmarker II test board. This allows the testing of solder pastes on standard PCB surfaces such as Entek OSP (Organic Solder Protectant) and ENIG (Electroless Nickel Immersion Gold). Quite simply we are making copper sandwiches (Figure 8) that result in cylindrical structures, which permit highly quantitative void analysis with standard BGA analysis software.

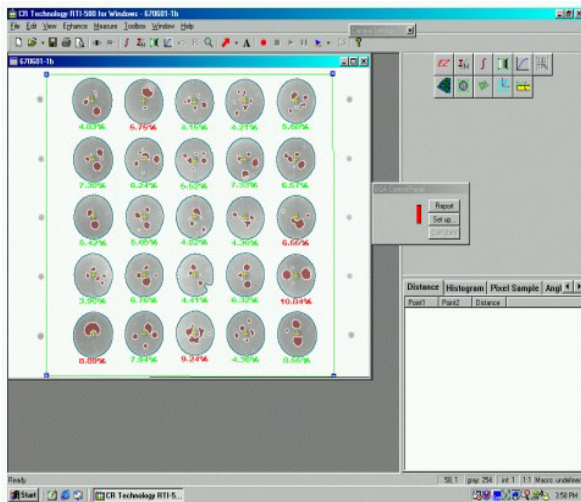


Figure 6 - Void Analysis Software

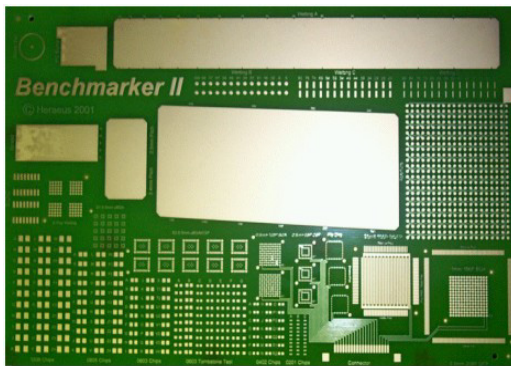


Figure 7 - Benchmarker II Test Board



Figure 8 - Assembled Copper Preforms

Shelf Life Effects

The first application of the CCGA quantitative void test was to study the effects of aging on a materials tendency to void. Two materials were tested, Material A was a standard rosin based RMA and Material B was a synthetic resin based low residue no clean for 24 weeks at both room temperature and cold storage. For each paste/storage combination, each week 250 preforms (10/90) per paste test were assembled and x-rayed. A frequency distribution was run on the data as well as a bulk average. Pass/fail data for structures that had an individual void of 5% or greater was also

assembled into the data set. The summary chart in Figure 9 shows the four key data points tracked:

1. $>10\%$ is the percent of structures that have high total voiding of 10% or more from the frequency distribution.
2. *Big Voids* is the percent of structures that have an individual large void of 5% or more.
3. $<5\%$ is the percent of structures that have low total voiding of 5% or less from the frequency distribution.
4. *AVG* is the bulk average of the data.

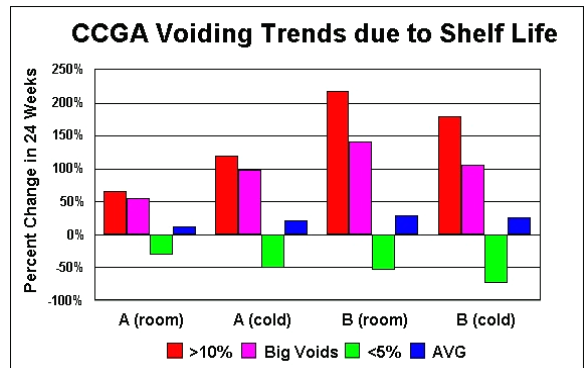


Figure 9 - Storage Effects on Voiding

From this data there are clearly different trends for the two materials as well as a significant difference in void behavior between them. The effect of time on Material A is accelerated in cold storage and just the opposite with Material B. Both materials have the exact same source and specifications of the inorganics (powder + additives).

Profile Effects

The effect of the reflow profile can be significant but the magnitude varies greatly from one formulation to another. The following example involves two 63/37 Sn/Pb no clean materials^{3,4}, tested over Entek passivated copper using the copper preforms with the 4 profiles as illustrated in Figure 10. This profile matrix is designed to expose profile sensitivity of a given formulation, in this case relating to voiding. There are two profiles with a ramp style preheat and two with a soak preheat. There are 2 profiles with a peak of 225°C with 60 seconds over liquidous and two hotter profiles with a peak of 240°C with an extended liquidous of 90 seconds. The X-ray data has been compressed into a single “point scale” to facilitate comparisons. These points (100 is best) are calculated as follows:

$$\text{Points} = (\leq 4\% - \geq 6\%)$$

“% of structures with 4% total voiding or less minus the % of structures with 6% total voiding or more.”

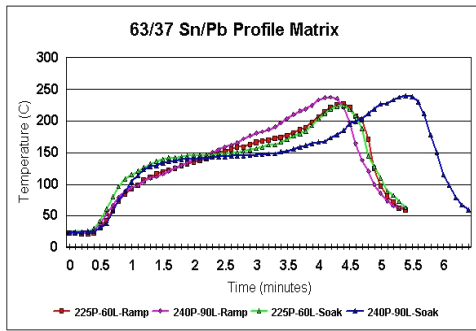


Figure 10 - Profile Sensitivity Matrix

The results in Figure 11 clearly indicate that Material 1 is insensitive to the profiles tested for void formation and significantly better than Material 2 for overall voiding. The two materials share the same resin system and concentrations; the major difference between the two materials is that Material 1 has a blend of activators at a significantly higher concentration than Material 2. A solvent blend is another difference in Material 1 versus a single solvent in Material 2. Material 1 is a newly engineered no clean illustrating the ability to formulate for low voiding given the proper quantitative tools for measuring voids.

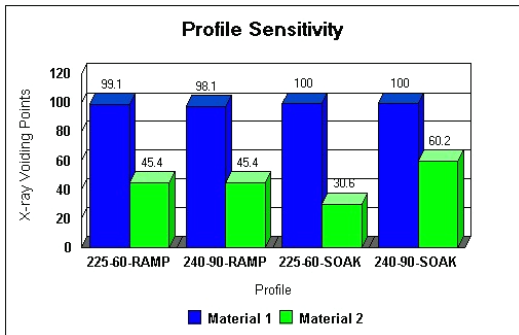


Figure 11 - Profile Sensitivity Test Results

The next example of profile sensitivity involved the Department of Energy (DOE) to improve CCGA voiding. (See Table 1.) Eight different profiles were created and two volumes of solder paste (control + 120% control). The table below summarizes the major differences in the profiles.

Figure 12 indicates a large contrast in DOE results indicative of severe profile sensitivity but also a solution for this material of a higher peak temperature (cells 5-6H and 13-14H) and increased solder volume.

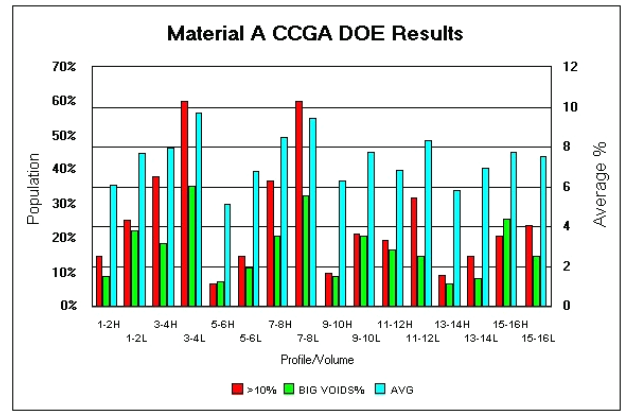


Figure 12 - Optimizing CCGA Reflow

Table 1 - CCGA Profile /Paste Volume DOE

Trial	Peak	Liquidous	Slope	T ₁₅₅₋₁₆₅
1-2	203	1.3min	0.8	
3-4	220	3.8min	0.8	
5-6	217	1.5min	0.5	
7-8	201	3.9min	0.5	
9-10	203	1.7min	0.5	4.9min
11-12	220	3.7min		4.8min
13-14	219	1.6min		4.7min
15-16	203	3.6min	0.8	4.8min

Metallurgical Effects

It is fairly well known that lead free solder pastes exhibit a higher level of voiding than their tin/lead counterparts. Figure 13 shows the extreme contrast of voiding results between leading lead free⁶ and lead bearing⁵ no clean solder pastes. Figure 14 shows the data distribution of the worst lead free and the best lead bearing material. All of this data was generated on Entek OSP boards and copper preforms.

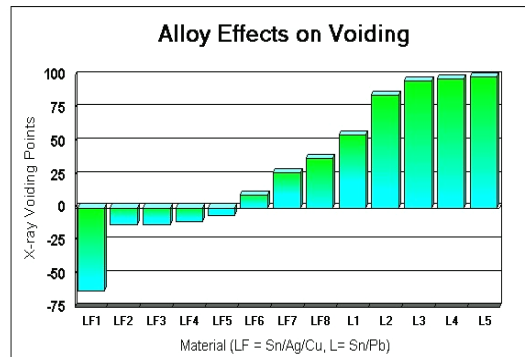


Figure 13 - Lead Vs Lead Free Voiding

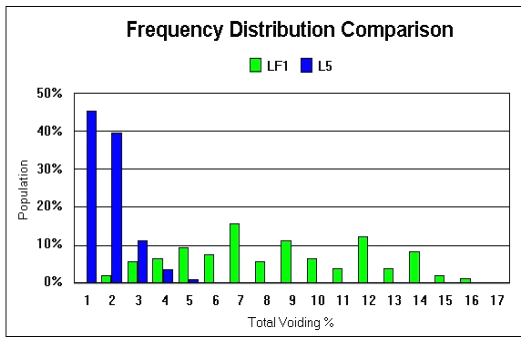


Figure 14 - Data Distributions

The next example⁷ further emphasizes the relationship between the solder pastes inherent voiding tendency and the additive effects of a solderable surface. Material A (specialty paste for CCGA) was printed through a 10 mil stencil as circular deposits onto a bare 4.5" sq 96% Al₂O₃ substrate. Several copper 5 mil thick preforms were placed around the printed deposits to act as spacers and a second substrate was placed over the wet paste then reflowed. After reflow the solder formed discs ranging from 10 to 15 mils thick. From the X-ray in Figure 15 it is revealing to see very little voiding, in fact many of the structures are void free. The red arrow points to a 30 mil diameter 10/90 10 mil thick preform as a reference. This test indicates the voiding characteristics of just the paste in that there were no solderable surfaces in this system. Voiding ranged from 0% to 1.76%. The next observation related to this product is the increase in voiding when the same lot of material is simply printed and reflowed on the coupon metalization as in Figure 16. This leads to the postulation that there is some form of a reaction between the coupon metalization and the solder paste during the reflow operation. Voiding ranged from 0.14% to 4.13%. The final observation is yet another noticeable increase in overall voiding ranging from 2.62% to 8.21% when the solder paste was "capped" with 5 mil thick 10/90 preforms.

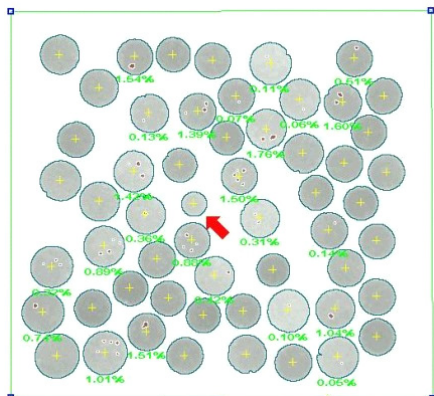


Figure 15 - Solder Paste "Discs"

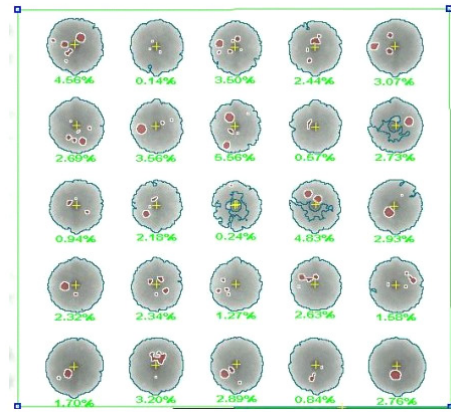


Figure 16 - Paste on Pad Voiding

Initially it was thought that the capping process was the cause of the increase in voiding by preventing flux from escaping during reflow but the "substrate sandwich" experiment in Figure 17 possibly negates this theory. Perhaps the additional solderable surface of the solder preform cap is more the cause of the additional voiding. If this theory holds true then 80% - 90% of the voids are due to the interaction with the surfaces to be joined and not the raw solder paste.

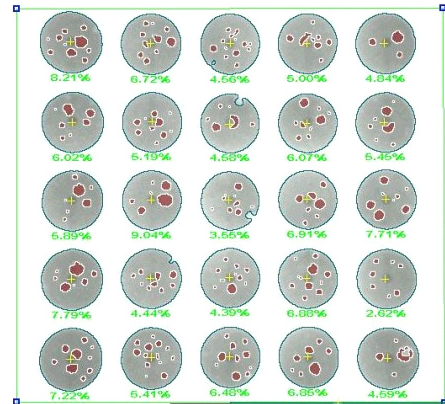


Figure 17 - "Capped" Solder Voiding

Design Effects

Components such as the Bumpered Chip Carrier (BCC) as seen in Figure 18 are typically problematic for voiding under the large flat central heat spreader. Large voids prevent even and rapid heat transfer and can cause premature component failure, a loss of performance or both. The problem is aggravated by the additive voiding with lead free pastes as described earlier. A 27 design element, 4 paste experiment⁸ was constructed to find the optimal design/paste combination. The experiment was repeated with nitrogen reflow with similar to air reflow results. The metalization on both the BCC and the PCB was ENIG. The central large trapezoidal section of the Benchmarker II test board (Figure 7), which is normally used for a printability line resolution test, was used as a common solder pad.

Design ideas ranging from simple squares to complicated shapes were included as can be seen in Figure 19. Devices were simply picked and placed in an array over the 27 designs and reflowed. Paste coverage relative to the central heat spreader area ranged for 25% to 100%.

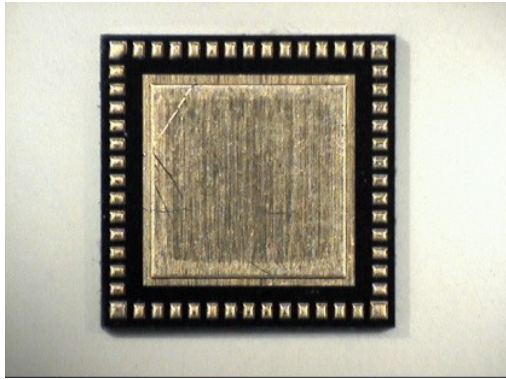


Figure 18 - BCC Package

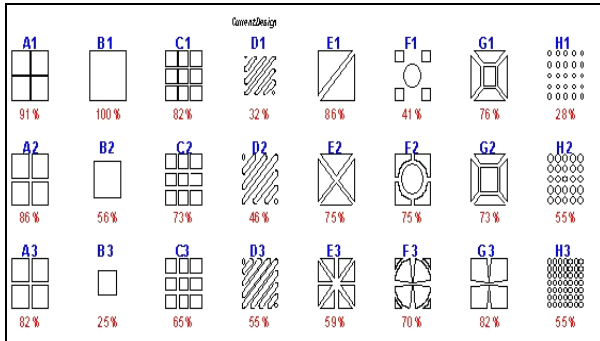


Figure 19 – Heat Spreader Design Matrix

Devices were X-rayed and a die attach % coverage software applet was used to quantify the total % voiding as well as the largest void size. The initial data sort as can be seen in Figure 20 indicated there may be a correlation between paste coverage and total voiding. The data also illustrates a performance difference between materials independent of design for the most part. Regression analysis plots (Figure 21) further supported the simple trend of more coverage equals less voiding with the simplest design (B1) yielding the best results. Further profile work with paste C met the target (<20%) voiding from the customer. The project began with about 70% total voiding.

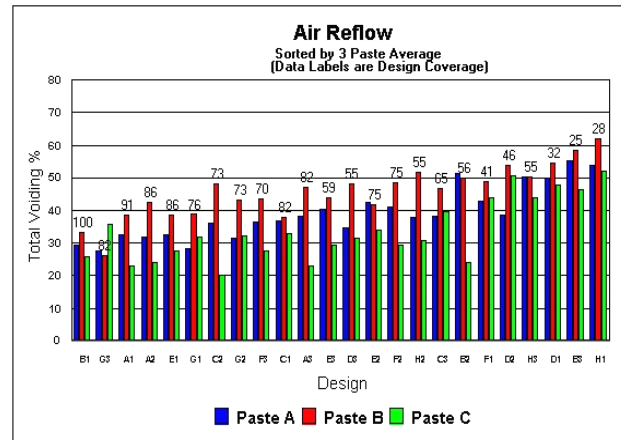


Figure 20 - Heat Spreader X-ray Results

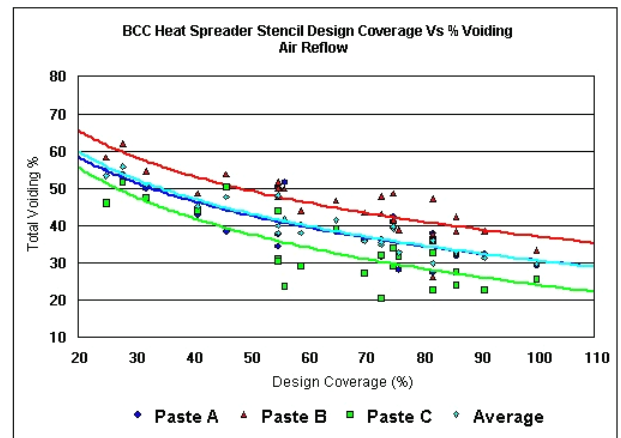


Figure 21 Paste Coverage Vs Voiding Trend

Conclusions

Although many questions remain unanswered, we have learned a few trends for avoiding the solder void.

- Void formation is a result of a system of variables not a single source.
- Each paste is unique in its voiding behavior relative to reflow profile and sensitivity.
- Paste age and storage conditions can affect the level of voiding.
- There are more contrasting results with lead free no clean pastes than their lead bearing counterparts.
- Pad and component metallurgy have a definite impact on total voiding.
- Large area soldering, as in a device with a heat spreader, can be problematic for voiding but can be minimized by maximizing the paste coverage.

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