Advanced Thermal Management Solutions on PCBs for High Power Applications

Gregor Langer[1], Markus Leitgeb[1], Johann Nicolics[2], Michael Unger[2], Hans Hoschopf[3], Franz P. Wenzl[4]

[1]Austria Technologie & Systemtechnik AG, Fabriksgasse 13, 8700 Leoben, Austria

[2]Institute of Sensor & Actuator Systems, Vienna University of Technology, Gusshausstraße 27-29, 1040 Vienna, Austria

[3]Tridonic Jennersdorf GmbH, Technologiepark 10, 8380 Jennersdorf, Austria

[4]Institute for Surface Technologies and Photonics, Joanneum Research Forschungsgesm.b.H. Franz-Pichler Straße 30, 8160 Weiz, Austria

ABSTRACT

With increasing power loss of electrical components, thermal performance of an assembled device becomes one of the most important quality factors in electronic packaging. Due to the rapid advances in semiconductor technology, particularly in the regime of high-power components, the temperature dependence of the long-term reliability is a critical parameter and has to be considered with highest possible care during the design phase.

Two main drivers in the electronics industry are miniaturization and reliability. Whereas there is a continuous improvement concerning miniaturization of conductor tracks (lines / spaces have been reduced continuously over the past years), miniaturization of the circuit carrier itself, however, has mostly been limited to decreased layer-counts and base material thicknesses. This can lead to significant component temperature and therewith to accelerated system degradation.

Enhancement of the system reliability is directly connected to an efficient thermal management on the PCB-level. There are several approaches, which can be used to address this issue: Optimization of the board-design, use of base materials with advanced thermal performance and use of innovative buildup concepts.

The aim of this paper is to give a short overview about standard thermal solutions like thick copper, thermal vias, plugged vias or metal core based PCBs. Furthermore, attention will be turned on the development of copper filled thermal vias in thin board constructions. In another approach advanced thermal management solutions will be presented on the board level, exploring different buildup concepts (e.g. cavities). Advantages of cavity solutions in the board will be shown, which not only decrease the thermal path leading from the high power component through the board to the heat sink, but also have an impact concerning the mechanical miniaturization of the entire system (reduction of z-axis). Such buildups serve as packaging solution and show an increase in mechanical and thermal reliability.

Moreover, thermal simulations will be conducted and presented in this paper in order to reduce production efforts and to offer optimized designs and board buildups.

KEYWORDS

PCB, thermal management, power electronics, low thermal resistance, cavities

1. INTRODUCTION

Modern power electronics is using power components like MOSFETs, IGBTs, GTOs, high brightness LEDs and many more. Due to the enormously rapid advances in semiconductor technology, particularly in the regime of high-power applications, the trend is going to smaller components with even higher switching speeds and higher current densities. In general a strong miniaturization trend for whole modules can be seen.

With these trends and with increasing power loss densities the thermal performance of an assembly becomes one of the most important quality factors in electronic packaging. New materials but also new and innovative approaches in the area of the PCB-substrates are required to meet the required reliability levels.

Interest in power electronics has grown dramatically in the last few years with increasing need for electric power management and control (Smart Grid), renewable energy generation and control (wind power, photovoltaic, fuel cell, etc.), electric transportation, and the desire to improve operating efficiency of heavy systems (trains, industrial motors, electric vehicle, etc.).

Power electronic converters are found wherever there is a need to modify the voltage, current or frequency. These range in power from few milliwatts in mobile phones to hundreds of megawatts in HVDC (high-voltage, direct current) transmission systems (Fig. 1). Usually we think of electronics in the framework of information, where speed is the primary interest. In the context of power electronics improved efficiency and lower power losses are important.

Figure 1. Range of power electronic applications (Source: iNEMI Technology Roadmaps, Jan 2013)

2. THERMAL RESISTANCE

Definition of the thermal path and thermal resistance

For steady-state considerations most frequently used measures for the thermal performance of an electronic module are either the junction temperature T_J of the semiconductor device with the significant power loss or – even more common – the thermal resistance R_{th}. The latter has to be defined by the temperature difference ϑ along a thermal path as e.g.

$$\vartheta = T_J - T_C, \tag{1}$$

where T_C denotes the temperature of the interface of the case of the module and a cooler, and the power loss P_{loss} causing the temperature difference

$$R_{th} = \frac{T_J - T_C}{P_{loss}} \tag{2}$$

Equation (2) is a useful practical approach to describe the thermal performance of a power assembly if T_J and T_C are isotherms and the entire heat flow from T_J to T_C equals P_{loss}. It should be noted that these conditions are not always fulfilled. In small silicon transistors and diodes the rather small temperature gradients within the junction

can frequently be neglected. However, as can be seen by a more detailed thermal investigation of a GaAs high-power transistor, depending on the considered semiconductor device, there are tremendously high temperature differences within the junction itself [1]. Another frequently underestimated danger to misinterpret equation (2) arises if the case temperature is not enough uniform. To reach a uniform case temperature over an area as large as possible is one major concern of the thermal management on the PCB level.

A further approach to describe the thermal resistance R_{th} is shown in equation (3). It can be seen that the thermal resistance can be minimized by reducing the length d of the thermal path or by increasing the thermal conductivity λ of the material as well as by increasing the area of the contact pad A. As already stated in the introduction there is a trend in miniaturization of the power components, so there is no chance to increase the area. For this only the two first possibilities can be used to improve the thermal management of the system. That means the length of the thermal path through the PCB should be as short as possible, and the material between component and heat sink should have a thermal conductivity as high as possible.

$$R_{th} = \frac{l}{\lambda \cdot A} \tag{3}$$

Motivation for thermal management

The main reason for deficiencies of electrical systems beside dust, vibration and humidity is by far the impact of temperature. Therefore an efficient thermal management concept on the PCB is crucial for the reliability of power electronic systems.

As an example we take high power LED applications, which are likely to dominate in the next years residential and commercial lighting, signaling and vehicle headlights due to efficiency and extended lifetime. LEDs that range from 500 milliwatts to as much as 10 watts in a single package have become standard, and researchers expect even higher power in the future.

Thermal management is of critical importance for high power LEDs. More than 60% of the electrical power input is converted into heat and built up at the junctions of LED chips due to non-radiative recombination of electron-hole pairs and low light extraction.

If that heat is not removed, the LEDs run at high temperature, which not only lowers their efficiency, but also makes the LED more dangerous, less reliable and shortens operating life [2,3]. Thus, thermal management of high power LEDs is a crucial area of research and development.

In this paper results of simulations and measurements of different LED-modules will be shown and should serve as representative of thermal solutions for general high power applications.

3. STANDARD PCB-TECHNOLOGY FOR THERMAL MANAGEMENT

Overview and short description

An effective heat removal can be based either on a short heat conduction path to a heat sink perpendicular through the PCB (e.g. thermal vias) or by a conductor layer acting as a lateral heat spreader (extended thermal pads) or a combination of both.

There are many different and well known build-ups for these heat removal concepts on PCBs. Thick copper approaches on PCBs guarantee a very good lateral heat spreading effect due to the excellent thermal conductivity of the copper and are very well used to reduce hot spots.

IMS (Insulated Metallic Substrates) are also state of the art and widely spread for thermal issues in electronic systems. An IMS consists of a metallic base material (mostly aluminum or copper) with a thickness of about 0.5 mm to 3.0 mm. On the metallic base material there is a thin dielectric layer (about 30 µm - 150 µm) with a high thermal conductivity (0.5 – 8.0 W/mK) in respect to standard FR4-material (ca. 0.3 W/mK). The copper design layer is on top of the dielectric layer.

IMS show a very short heat conduction path through the thin dielectric layer, because the metallic base material serves already as first heat sink. There are several different IMS variations available depending on the requested performance.

Further build up concepts using a short heat conduction path to the heat sink are conventional through-hole plated glass fiber reinforced PCB technologies. A sufficient thermal performance in the lower power loss range up to several watts can frequently be achieved by reasonable numbers for via count, via diameter, and hole plating thickness [4]. Figure 2.a shows a scheme of a PCB with open through holes serving as open thermal vias. In figure 2.b an example of a footprint design is shown. It can be seen that the thermal vias are situated in the extended thermal pads beside the pad, where the component will be placed. So, to avoid the well-known problem of solder soaking, it is not possible to place open thermal vias directly underneath a component. Due to this fact, the thermal path is elongated, because the heat has to be spread first laterally on the surface before it can be guided perpendicular through the PCB to the heat sink (Fig. 2.c).

A schematic cross section as depicted in figure 3.a demonstrates a special via plating technology featuring plugged vias with a homogeneous copper layer on the front faces. In contrast to the concept with open vias, this build up allows vias directly beneath a component, which also reduces the thermal path. Figure 3.b shows a microscopic view of a cross section of this type of PCBs.

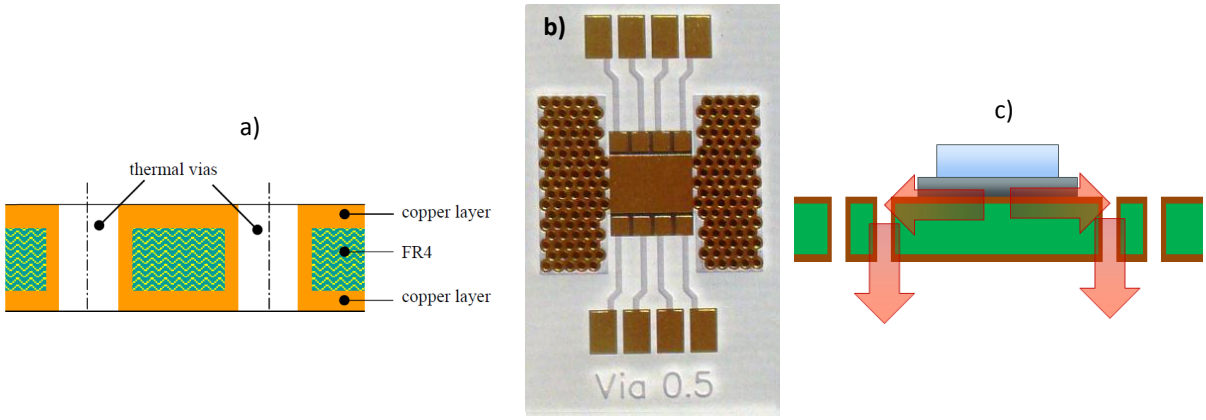


Figure 2. PCB with open thermal vias: a) Scheme; b) design; c) thermal path

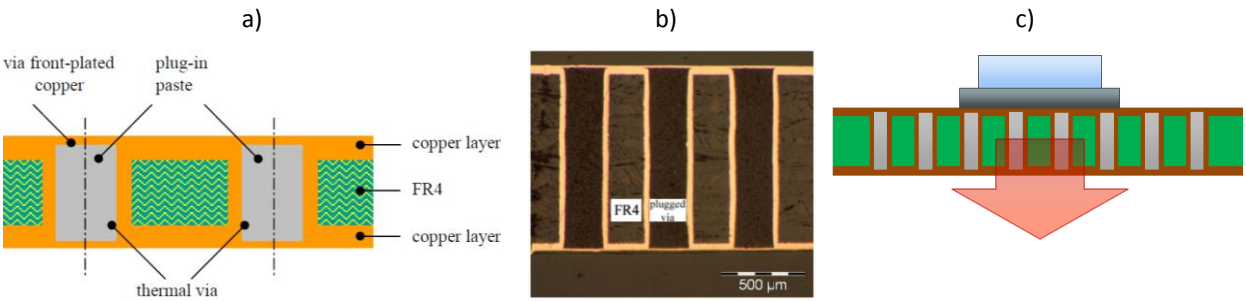


Figure 3. PCB with plugged thermal vias: a) Scheme; b) cross section; c) thermal path

Experimental setup

Test objects were selected with following specifications:

- DK2, (FR4, thickness = 1 mm, pads with plugged thermal vias)
- DK6, (FR4, thickness = 0.2 mm, open thermal vias with 0.3 mm diameter, laminated onto 1.5 mm thick Al-substrate with a 90 µm thick prepreg)
- IMS1, (70 µm thick copper clad, 110 µm thick dielectric, thermal conductivity = 0.5 W/(mK), Al-substrate thickness = 1.5 mm)

- IMS3, (70 µm thick copper clad, 125 µm thick dielectric, thermal conductivity = 4 W/(mK), Al-substrate thickness = 1.5 mm)

All PCB samples were prepared with a size of 30 mm x 40 mm. The layout allowed to test two power LEDs at the same time (Fig. 4.a) whereby the comparatively large via arrays should help to maximize heat spreading.

Most important qualities of an experimental set-up are to simulate boundary conditions as close as possible to the following extreme conditions:

a) The PCB itself acts as a heat sink by conducting the heat flux in the plane direction and dissipating e.g. by natural convection and radiation.

b) The PCB acts as mean to interconnect the power component with a cooler and to help spreading the heat flux uniformly over the entire attachment surface of the cooler.

In this section we compare the thermal performance of FR4-based PCBs with thermal via arrays (two different modifications: with open vias and with plugged vias) and IMS in an experimental set-up according to condition b). For this purpose a water-cooled copper block was used as a heat sink with constant temperature. The samples were attached to the copper block using an equally distributed thin layer of thermal grace with a thermal conductivity of 0.6 W/(mK). The samples were pressed against the copper block with pointed plastic screws in order to keep the thermal resistance of this interface as stable as possible without heat removal from the top side (Fig. 4.b).

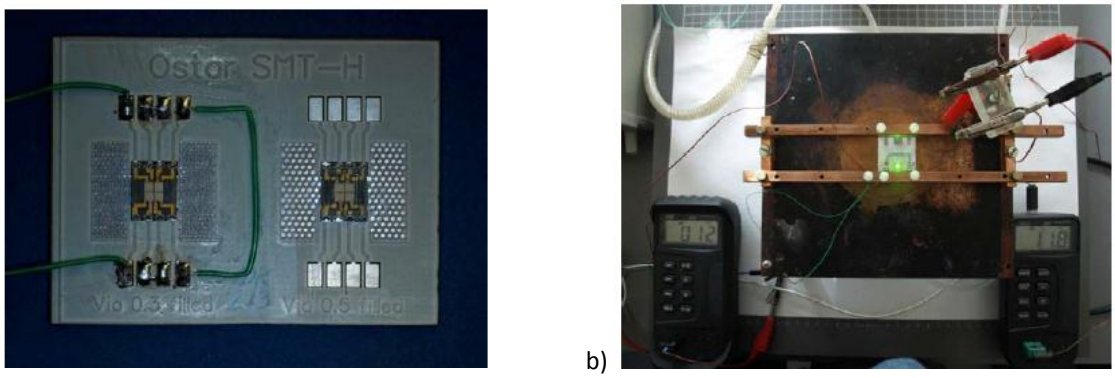


Figure 4. LED module mounted on water-cooled heat sink:
a) Top view of test sample; b) sample under test

Temperature distributions of the top side of the samples during operation with the nominal forward current (I_f = 700 mA) were recorded using a high-end thermography system. An emissivity correction was made by a calibration measurement with a miniaturized thermocouple at the LED pad.

From evaluation of transient thermal response on power-on-steps with the nominal power value we see that the final temperature distribution on the entire sample surface is obtained within only a few seconds in all cases. The temperature distributions obtained by IR thermography in the steady state are compared for all four sample types in figure 4. During experiments with the nominal forward current a voltage drop of $4U_f$ = 13.5 V was measured (four single LED elements in one module, connected in series). Assuming an average photonic efficiency of η = 20% we considered a continuous power loss of 7.56 W per sample. Since establishing of the junction temperature was related to high uncertainties we defined the pad-to-cooler thermal resistance $R_{th,p\text{-}c}$ as the relevant parameter characterizing the thermal performance of the PCBs in the following way:

$$R_{th,p-c} = \frac{T_{pad} - T_{cooler}}{4U_f \cdot I_f \cdot (1-\eta)}, \tag{4}$$

where T_{pad} is the temperature of the copper pad in the vicinity of the LED submount body and T_{cooler} is the temperature of the copper block. Using the respective temperature values from the IR thermography images and the values mentioned above equation (4) the results as listed in table 1 were obtained.

Thermal measurements / Results

From the IR thermography picture of the DK6 sample a well-developed heat spreading effect can be recognized (Fig. 5). The temperature gradients in the vicinity of the LED chip are the lowest ones compared to the other three types, thus the heat flux is conducted into the cooler through an enlarged area of the dielectric. This high heat spreading effect is due to the excellent thermal coupling of the two copper layers by the microvia arrays. However, because of the thick dielectric – a 90 µm thick prepreg with moderate thermal conductivity of only 0.3 W/(mK) the temperature distribution and therewith $R_{th,p\text{-}c}$ reaches the highest values.

From view point of the copper layout the DK2 and DK6 samples are very similar (It should be noted that the thin copper layer at the "plugged" via front faces does not contribute much to the heat dissipation). Though the thickness of the FR4 in the DK2 is five times higher than that in the DK6 the heat is conducted into the cooler at a remarkably lower temperature because the thermal vias are in intimate contact with the cooler. This also leads to a steeply declining temperature in lateral direction outside of the LED chip.

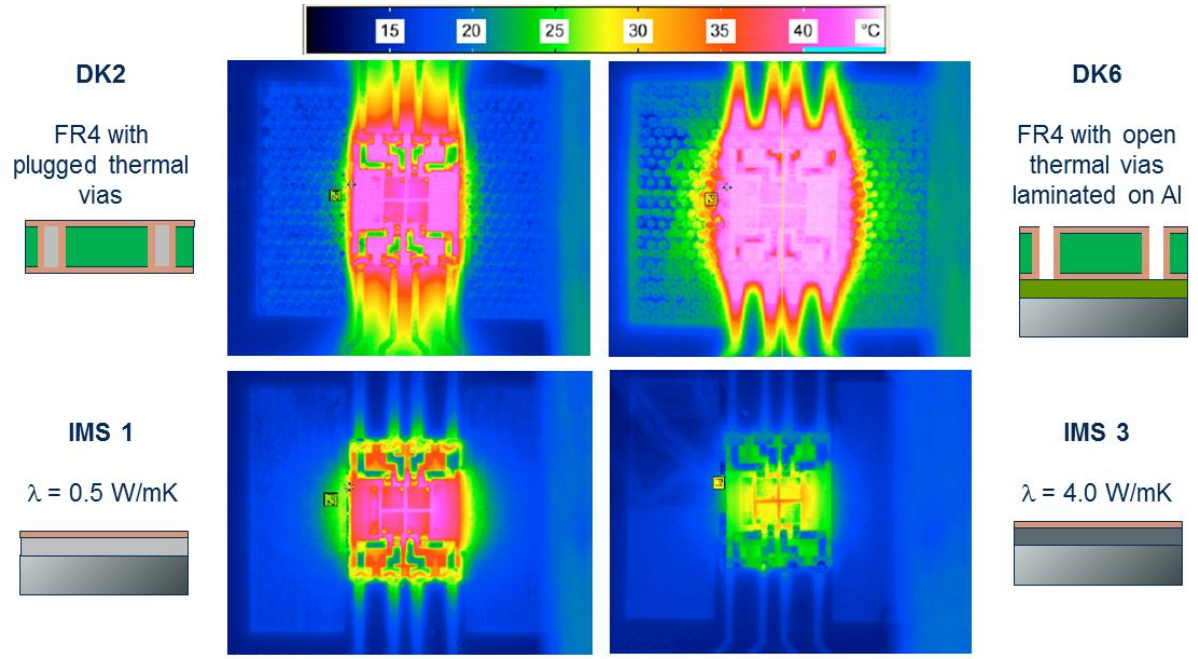


Figure 5. Comparison of results obtained from IR thermography measurements

Significantly lower as on the first two PCB types are the temperature distributions on the two IMS type samples. In spite of a heat flux density of more than 50 W/cm^2 the maximum temperature of the LEDs are lower than 40°C in case of the IMS1 sample and even lower than 33°C in case of the IMS3 sample. This can be explained by the higher thermal conductivity of the dielectric (in IMS1: 0.5 W/(mK), in IMS3: 4 W/(mK)).

Table 1. IR-thermography measurement results and evaluated thermal resistance values

Sample type	$T_{pad,IR\text{-}cam}$	T_{pad}	T_{cooler}	I_F	P_{el}	$R_{th,p\text{-}c}$
	°C	*°C*	*°C*	*mA*	*W*	*K/W*
DK2	36.0	41.6	13	700	9.45	3.8
DK6	42.9	49.6	13	700	9.45	4.8
IMS1	28.2	32.6	13	700	9.45	2.6
IMS3	26.6	30.8	13	700	9.45	2.3

4. ADVANCED THERMAL MANAGEMENT SOLUTIONS: Cavity Boards

Introduction

Another possibility to reduce the thermal resistance of the PCB is the use of cavities. Local depth reduction (through various methods and technologies) has long been applied to achieve a number of design and/or application linked results.

In this chapter the advantages of PCBs with special cavities regarding to advanced thermal management performance are presented.

Cavity Formation

The production method of PCBs with cavities presented in this paper is based on patented technology [5], which enables the removal of multiple layers at varying depths. The specific depth is achieved by the application of a paste on the release layer with subsequent relamination of the entire board. A laser cutting process then trims and cuts at the predetermined shape to separate the relaminated layers from the release layer. The final steps are "cap removal" and paste stripping (Fig. 6). What remains is the solder footprint pattern. Diverse surface finishes and also application of solder mask can be employed in the cavities.

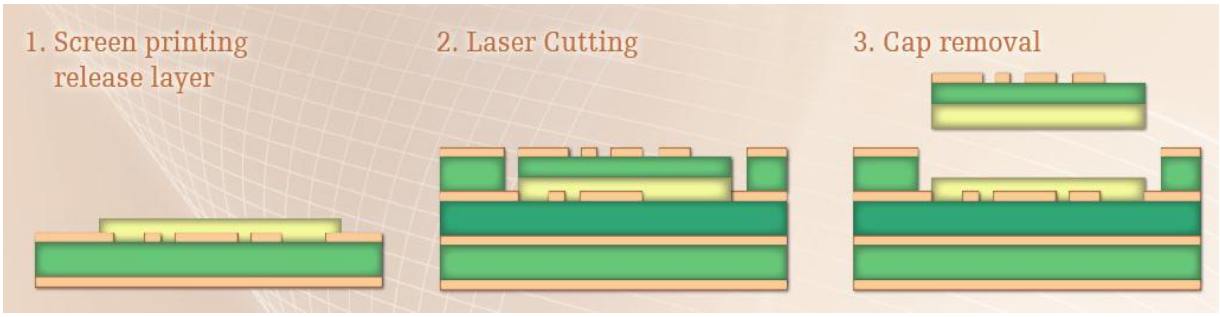


Figure 6. Schematic process flow of cavity formation

In order to achieve an optimal thermal performance the cavity formation process of figure 6 is modified, so that all dielectric layers are removed and only the bottom copper foil is remaining. The high power chip is directly attached into the cavity onto the bottom copper layer of the cavity. In this configuration a very short thermal path with the lowest possible thermal resistance (equation 3) between the component and the heat sink is formed. It consists of only the adhesive or solder layer of the component-PCB connection, the bottom copper-layer of the PCB, and the thermal interface material between PCB and heat sink (Fig. 7).

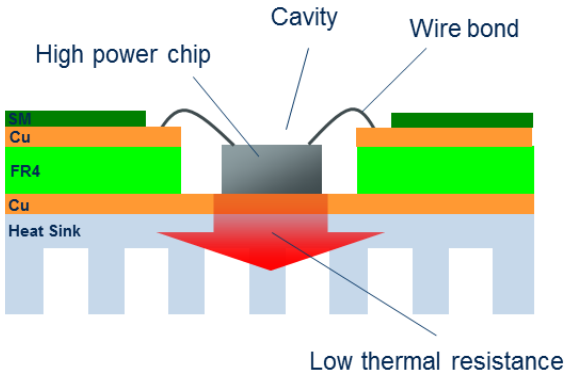


Figure 7. Chip in cavity build-up with optimized thermal path

Surface finishes like ENIPIG is applied on all layers, and the electrical interconnection is done with wire bonding onto pads on the top or medium layer (Fig. 7 and 8). For light applications, the cavity walls can be coated with highly reflective material as well (Fig. 9).

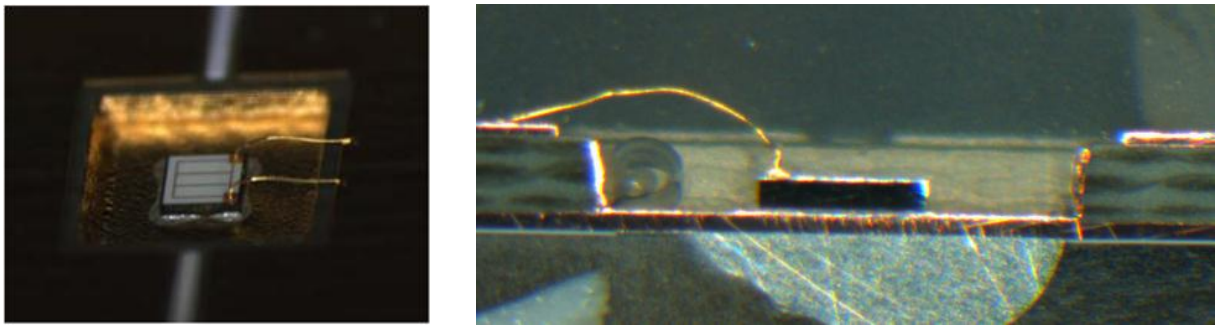


Figure 8. Chip in cavity bonded to the upper layer

Beside the excellent thermal behavior, this cavity board also shows additional advantages: It serves as package, which is protecting the component and in combination with an additional cavity (cavity in cavity, Fig. 9) it is also protecting the wire bonds. All together the concept results in a miniaturization in z-direction and finally in a reliable chip-package solution that supports long-term stability of LED-based luminaires.

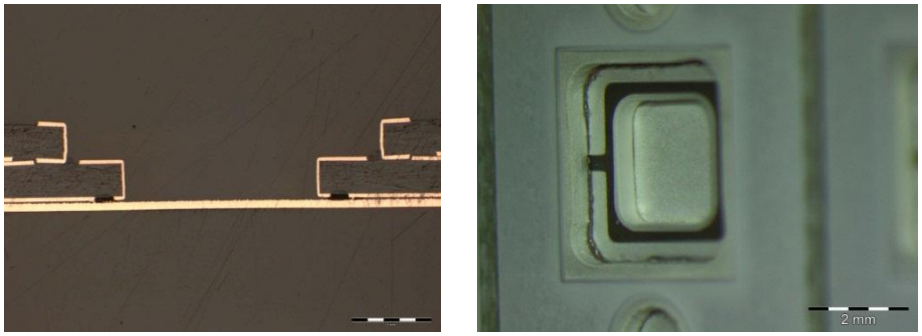
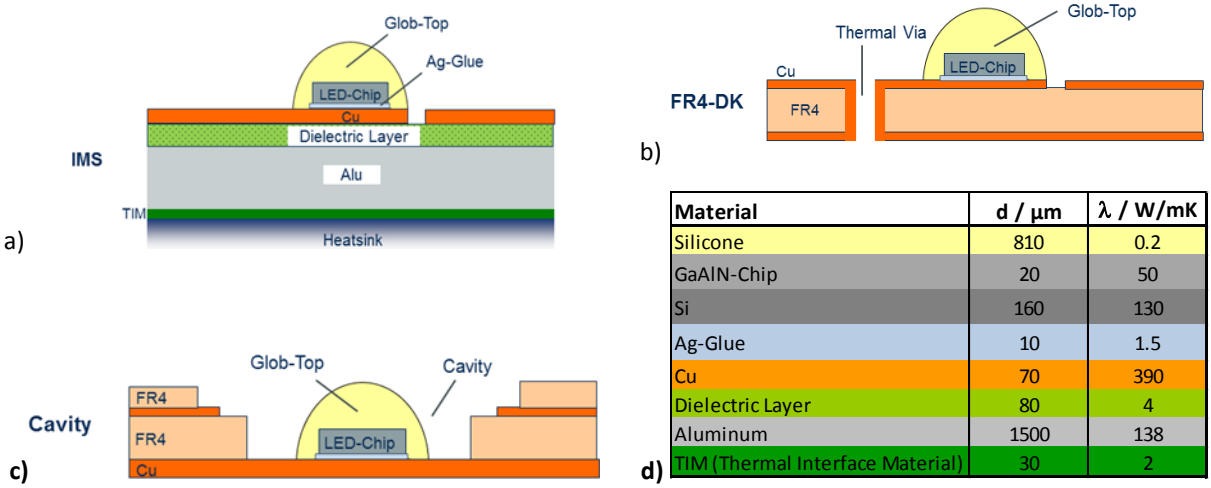


Figure 9. Cavity in cavity board with high reflective cavity walls

Thermal simulation

It is difficult to compare the over-all thermal performance of different packaging concepts purely on the base of single point temperature measurements. A deeper understanding of particular advantages and bottlenecks of particular set-up features is gained by thorough thermal simulations. In the following we compare three different packaging concepts using the same LED chip and the same operation conditions (Forward current I_F = 300 mA). These blue-light emitting LEDs were assumed to produce a power loss of P_{loss} = 660 mW, while the color conversion to white light is related to additional losses due to Stokes shift and absorption in the glob top in a total amount of 160 mW. Though this number might appear small it should be noted that these optical losses are set free in a silicone matrix with low thermal conductivity. This kind of loss causes by far the highest temperature values inside the LED set-up. We considered the spatial distribution of these losses (an exponential approximation of the decrease of the loss intensity with increasing distance to the LED surface) with an "onion shell" model [6]. The test assembly is assumed to be mounted on a heat sink with a constant temperature of 25°C. Thus, at the assembly's bottom face Neumann boundary conditions were considered: T_C = 25°C. Further boundary conditions on the remaining surfaces were considered as natural convection and radiation assuming an emissivity of 1. Three-dimensional steady-state thermal simulations with the finite element method using a Multiphysics software package with materials data were made for all set-ups of the considered packaging concepts as shown in figure 10.



Material	d / µm	λ / W/mK
Silicone	810	0.2
GaAlN-Chip	20	50
Si	160	130
Ag-Glue	10	1.5
Cu	70	390
Dielectric Layer	80	4
Aluminum	1500	138
TIM (Thermal Interface Material)	30	2

d)

Figure 10. Build-up of: a) IMS, b) FR4-DK, and c) Cavity board (LED-in-Cavity); d) material parameters used for thermal simulation

Figure 11 depicts the thermal model of an FR4-DK set-up as shown in figure 10.b. In order to reduce the necessary node number without loss of accuracy, the hollow thermal vias were replaced by cylinders filled with a substitute material of which the thermal conductivity in the perpendicular direction is equivalent to the hollow cylinder shaped copper vias with a wall thickness of 25 µm (Fig. 11.b). In this way a virtual thermal conductivity λ_{sub} of the via can be calculated on the base of the thermal conductivity λ_{Cu} of copper, the cross sections of the copper walls A_{Cu} and of air (DK6) or epoxy (DK2) in real vias [7]:

$$\lambda_{sub} = 4\frac{\lambda_{Cu} A_{Cu}}{d^2 \pi}, \tag{5}$$

where d is the drilling diameter and the thermal conductivity of air or epoxy is neglected in comparison to λ_{Cu}.

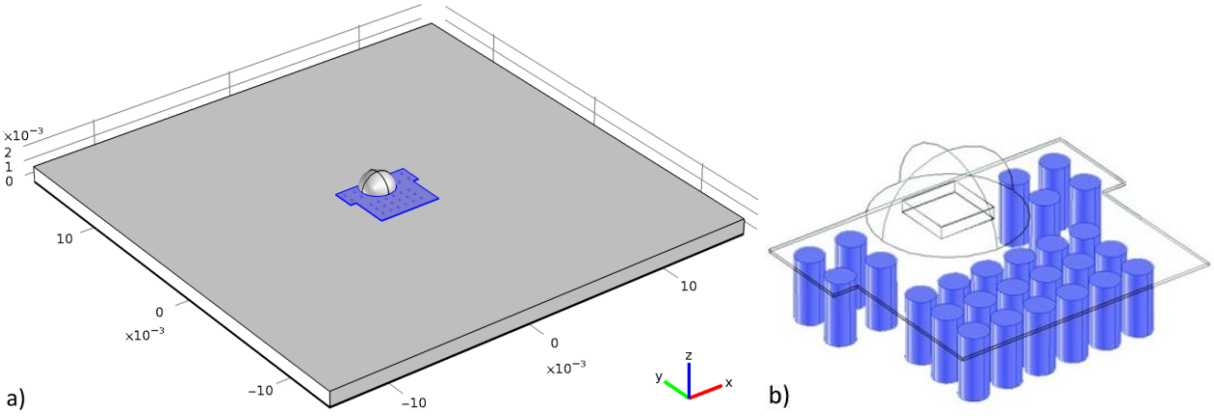


Figure 11. Thermal model of the FR4-DK test sample: a) Entire model; b) detailed view thermal via array

5. RESULTS

The thermal simulation revealed that under normal operation conditions all three investigated packaging concepts allow to keep the LED-chip surface temperature at moderate levels between 27.5°C (LED-in-Cavity concept) and 45.5°C (FR4-DK concept) and that very high temperature gradients (more than 200°C/mm) exist in the silicone glob top immediately above the chip surface. In all cases the temperature maximum is found at glob top surface (ca. 85°C at the IMS, ca. 95°C at the FR4-DK, ca. 70°C at the LED-in-Cavity samples). Figure 12 depicts the temperature distribution of a LED-in-Cavity sample. For reasons of comparability, in all cases the shape of the color converter was assumed as spherical glob tops. It should be noted that in a real case of the LED-in-Cavity the color converter does not tower above the PCB top surface. Therefore, the height of the color converter and therewith the maximum temperature is even lower than considered in our simulation. The quite

remarkable temperature differences inside LED chip and color converter of the three concepts can be understood by considering the temperature course along the perpendicular symmetry axis.

In spite of a heat flux density of more than 80 W per square centimeter the LED-in-Cavity set-up keeps the LED chip at a temperature level below 28°C due to the 70 µm thick copper base layer and the shortest possible heat conduction path. The most significant temperature drops can be found in the thermal interface layer (TIM) between the heat sink and the copper base layer and in the adhesive layer under the LED chip (Fig. 13).

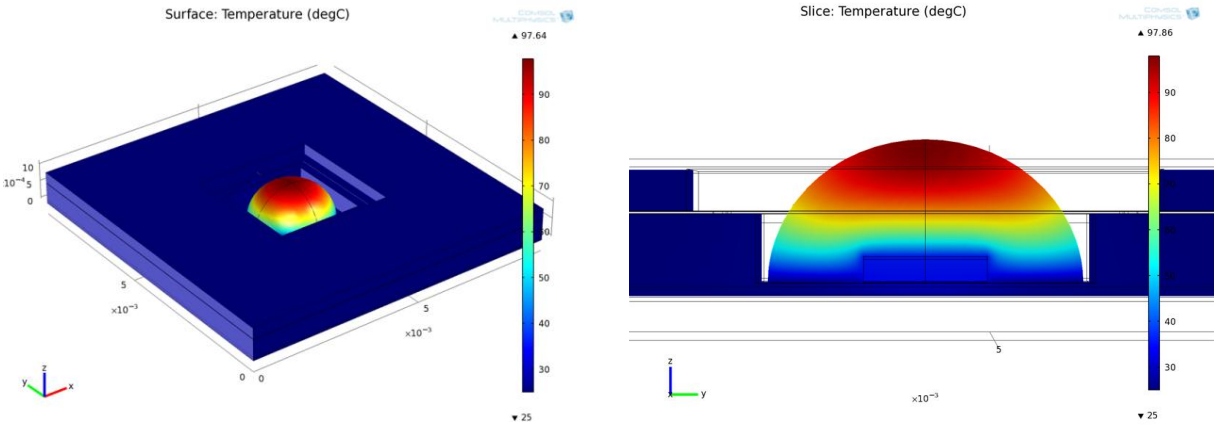


Figure 12. Results of thermal simulations; detailed views of temperature distribution in vicinity of the LED

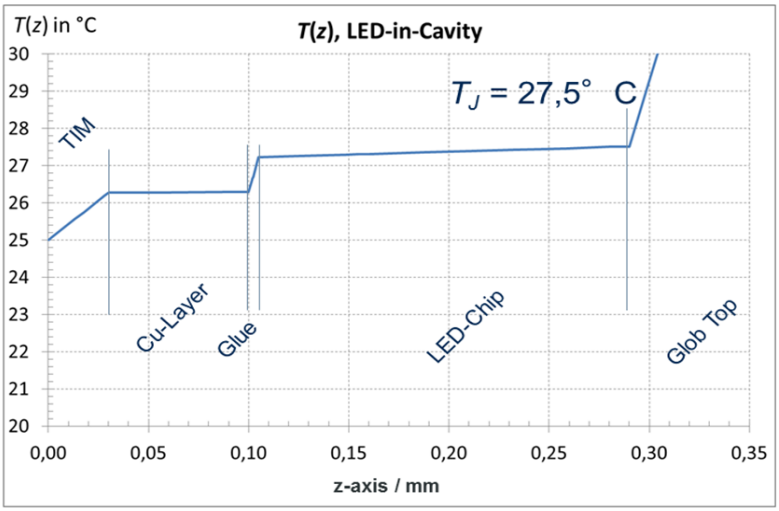


Figure 13. Results: Temperature profile along the symmetry axis in out-of-plane direction (z-axis) of a LED-in-Cavity set-up

The IMS module shows a LED-chip temperature between 32°C and 34°C. The most significant temperature drop is caused by the dielectric between the copper layer and the aluminum plate. The excellent thermal conductivity of the aluminum plate and the 35 µm thick copper layer can be recognized by the almost negligible temperature change inside the layer.

The highest temperature differences between heat sink and LED chip are found in the FR4-DK samples. Due to the fact that the thermal vias are placed only in a pad range apart of the LED chip instead of beneath, the path for a major part of the heat flux is comparatively long. This leads to LED chip temperature between 32°C and 41°C depending on the choice of geometry variation (via count, drilling diameter, Cu thickness etc.). In this context the feature of the plugged via technology should be highlighted: Although the thermal conductivity of a plugged via is practically the same as the open one with same hole geometry, with plugged vias the perpendicular temperature drop across the PCB can be reduced significantly because they can be placed directly beneath the LED chip without the risk of solder soaking. The respective temperature functions along the perpendicular symmetry axis are compared with each other in figure 14.

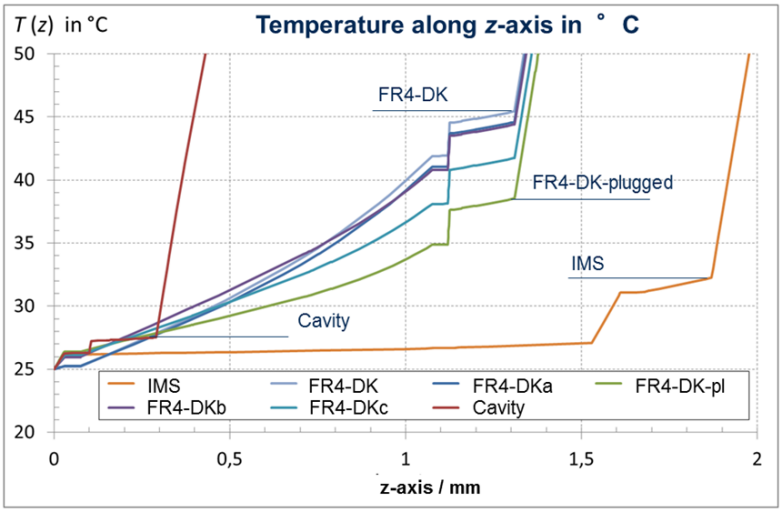
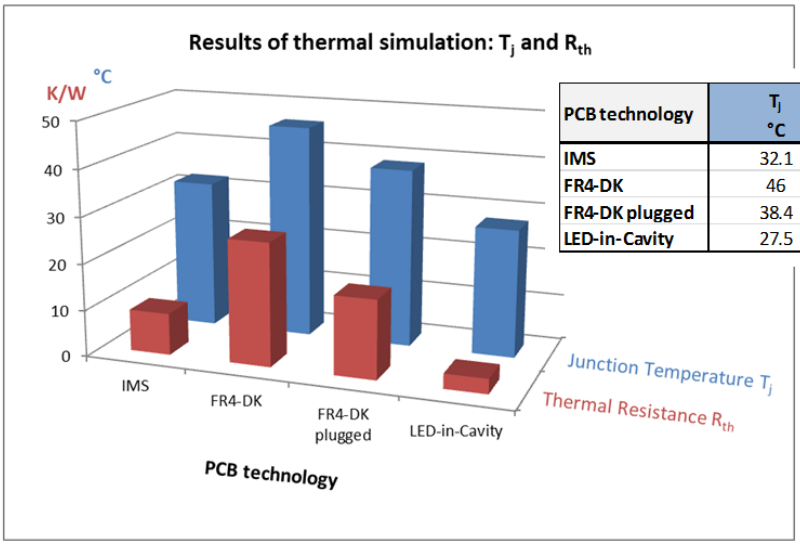


Figure 14. Comparison of the results of the different PCB technologies

Using the average temperature of the light emitting LED chip surface as the junction temperature and the heat sink temperature as the ambient temperature we defined the junction-to-ambient thermal resistance and compared this measure as the most representative one for all investigated set-ups (Fig. 15). The by far lowest thermal resistance can be seen at the LED-in-Cavity set-ups, followed by the IMS variants. However, it must not be withhold that an insulation layer between heat sink and semiconductor is frequently unavoidable. An insulating layer between the copper layer and the heat sink is also possible for the LED-in-Cavity solution but would also increase the thermal resistance. Conventional FR4 PCBs with thermal optimized via technology have higher thermal resistances but proved to be attractive and cost effective variants at least for the mid-power range.



PCB technology	T_j °C	$R_{th,j\text{-}amb}$ K/W
IMS	32.1	9
FR4-DK	46	26.5
FR4-DK plugged	38.4	16.9
LED-in-Cavity	27.5	3.2

Figure 15. Comparison of the results of the different PCB technologies

6. ADVANCED THERMAL MANAGEMENT SOLUTIONS: Cu-filled thermal vias

Thermal vias are employed since a long time to improve the heat transfer between the two sides of the PCB and to couple heat spreading copper areas. Because of the fact that thermal vias are normally hollow cylinders, solder can be soaked by the vias as mentioned above and, therefore, components are frequently not directly placed on top of the via array. Exceptions are large high power components where enough solder can be applied without the risk of critical voids forming underneath the component. This problem can be fully avoided if vias are fully filled with copper using a reverse plating process [8]. This can also help to increase the heat transfer area dramatically as can be shown by the following simple consideration. Let us compare the cross section of a

hollow via A_{hollow} with the one of a filled via A_{filled} an average copper cross section ratio β can be calculated as follows:

$$A_{hollow} = \frac{d^2 - (d-2a)^2}{4}\pi, \qquad A_{filled} = \frac{d^2}{4}\pi, \qquad \beta = \frac{A_{filled}}{A_{hollow}} = \frac{1}{4}\cdot\frac{d^2}{ad - a^2} \tag{6}$$

Herein d denotes the via diameter and a the via copper plating thickness.

For example, for a via with d = 200 µm and a = 30 µm β = 1,96 which clearly shows that by using filled vias the thermal resistance between top and bottom side can be cut in half.

Module build-up and thermal simulations

For an investigation of the effectiveness of the filled-via approach a setup according to figure 16.a is considered. A LED-chip of 300 µm thickness and 1 x 1 mm² lateral dimensions is soldered by Au80Sn-solder onto a bismaleimide triazine (BT) submount (3 x 3 mm²) that is copper coated (35 µm) on both sides forming the thermally relevant structure of the LED submount. Filled vias (d = 200 µm, n = 20) connect top and bottom side of the submount (Fig. 16.b). This submount is soldered with Sn96Ag solder onto an IMS-carrier (10 x 10 mm²) acting as heat spreader and heat sink interface. The solder layers were not modelled (omitted) because the temperature drop caused by the heat flow would be less than 50 mK. The aluminum part of the IMS was replaced by a constant temperature boundary condition. Table 2 lists the thermal properties of the materials inside the model.

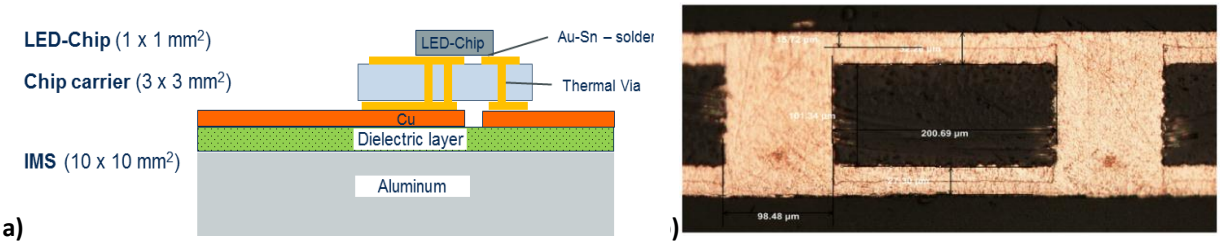


Figure 16. a) Chip carrier module build-up; b) cross section of chip carrier

Table 2. Material properties of components used for finite element model

Component	Material	Thermal conductivity λ in W/mK
LED	Sapphire	36
traces and vias of PCB	Copper	390
Dielectric of PCB	BT	0.12
Solder	Sn96Ag	not modelled (ΔT < 50 mK)
Dielectric on heat sink	Transtherm T2022	0.6
Dielectric of IMS	Filled epoxy	1.0 (thickness = 100 µm)

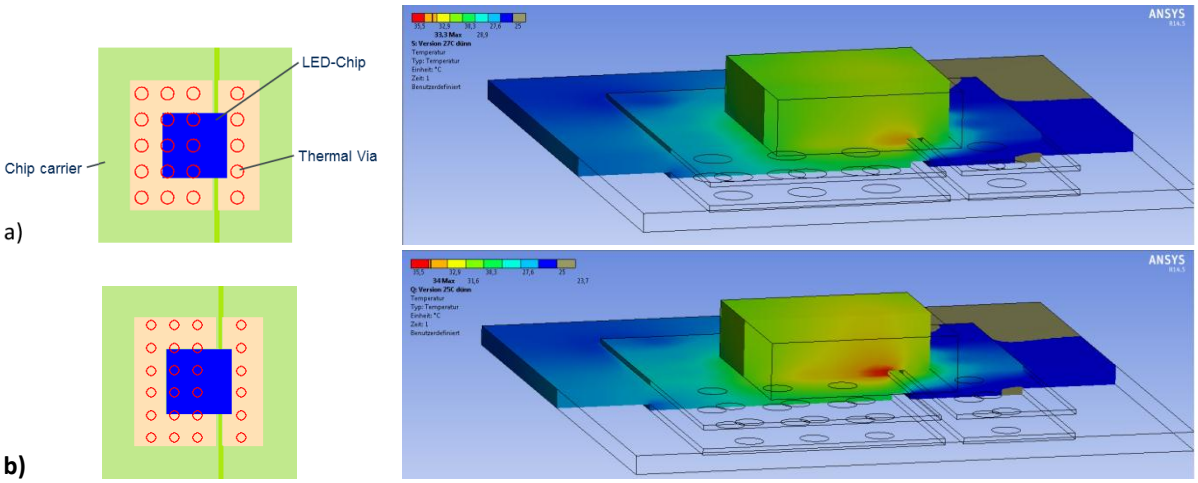


Figure 17. Chip carrier design and first results of thermal simulation:
a) 20 vias, d = 200 µm; b) 24 vias, d = 150 µm

Table 3. Maximum temperature and thermal resistance with different thermal via set-ups

Variant	via diameter in µm	number of vias		effective via cross section in mm²		max. temperature in K	thermal resistance in K/W
		all	under chip	all	under chip		
a	0.2	20	5.9	0.5	0.19	33.3	10.9
b	0.15	24	5	0.42	0.09	34	11.6

The simulation results show, that it is highly beneficial to use filled vias to reduce the resistance of the thermal path. The component can be placed directly on top of the vias without any problems with insufficient solder (e.g. because of solder sucked up by the copper clad via hole). However, experience gained from manufacturing makes it clear, that via-filling is not always perfect and dimples on the surface can occur. Such an air void inside the solder layer beneath the chip is shown in figure 18. The meaning of the solder defect due to the dimple formation in the galvanic process mechanical reliability will be investigated in further studies. However, thermal simulation proved that they are insignificant for the thermal resistance. Also optimization of via geometry and placement will be conducted, as well as the influence of copper thickness of the top layer that contributes the most to initial heat spreading of the chip's power loss.

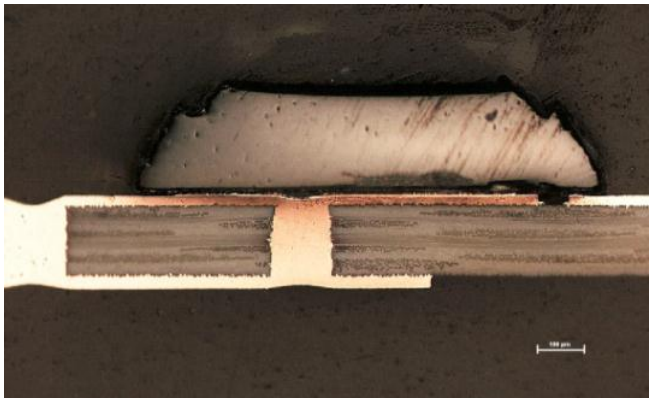


Figure 18. Chip carrier with dimple inside via

SUMMARY

Several different concepts for thermal management solutions on printed circuit boards for high power applications were shown in this paper. Benefits of state-of-the-art concepts, like Insulated Metal Substrates and open or plugged thermal vias were illustrated by comparing the thermal performance of high-power LED modules built-up with different concepts. In particular the plugged thermal vias and the Insulated Metal Substrates as they allow to realize short heat conduction paths turned out be interesting thermal management solutions.

Beside these well-established variants also some new concepts have been presented. Cavity boards (boards with local depth reduction) show thermal advantages due to a reduced thermal path along the *z*-axis through the board.

Thermal simulations of cavity boards attached with high power light emitting devices show excellent cooling performance. In comparison with the simulation results of state of the art concepts, the cavity board approach shows by far the lowest thermal resistance of the board system and guarantees therefore also the lowest junction temperature for the attached high power component. The realization of test vehicles of these concepts is planned, to verify the simulation data by thermal measurements on these test boards.

Furthermore also the thermal advantages of copper-filled thermal vias in chip carrier boards have been presented. First results of thermal simulations have been shown and discussed. Further simulations and measurements on test vehicles are going on, and the results of these thermal investigations are also planned to be published in the near future.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the financial support from the "Neue Energien 2020" program, project number 827784, of the Austrian Climate and Energy Fund and the Austrian Forschungsförderungsgesellschaft mbH (FFG).

REFERENCES

[1] G. Hanreich, M. Mayer, M. Mündlein, J. Nicolics, *"Thermal Investigation of GaAs Microwave Power Transistors,"* Journal of Microelectronics and Electronic Packaging, 2004, Vol. 1, No. 1, pp. 1-8.

[2] L. Zhou, B. An, Y. Wu, S. Liu, *"Analysis of delamination and darkening in high power LED packaging,"* 16th IEEE Int. Symp. on the Physical and Failure Analysis of Integrated Circuits, IPFA 2009, 6-10 July 2009, pp. 656-660.

[3] P.Z. Shi, P. Arulvanan, A.C.W. Lu, *"Thermal Performance Evaluation of Power SSL Module in LTCC,"* 9th Electronics Packaging Technology Conference, EPTC 2007, 10-12 Dec. 2007, pp. 285-288.

[4] J. Nicolics, M. Franz, V.L. Deepak, G. Weichslberger, *"Innovative printed circuit board technology for heat removal with application to power LED based operating room lamps,"* Proc. of 32nd Int. Spring Seminar on Electronics Technology, ISSE 2009, 13-17 May 2009, pp. 1-7.

[5] 2.5D-technology ® by AT&S AG

[6] P. Krivic, P. Fulmek, F.-P. Wenzl, Ch. Sommer, P. Hartmann, P. Pachler, H. Hoschopf, G. Langer, J. Nicolics, *"A comprehensive study on thermal issues of phosphor converted light-emitting diodes,"* 2nd LED professional Symposium +Expo, LpS 2012, Bregenz, Austria, 25-27 Sept. 2012, pp. 28-35.

[7] M. Weilguni, J. Nicolics, R. Medek, M. Franz, G. Langer, F. Lutschounig, *"Characterization of the Thermal Impedance of High-Power LED Assembly based on Innovative Printed Circuit Board Technology,"* IEEE Proc. of 33nd Int. Spring Seminar on Electronics Technology, ISSE 2010, 12-16 May 2010, Warsaw, Poland, pp. 238-244.

[8] A. C. West, C.-C. Cheng, B. C. Baker, *"Pulse Reverse Copper Electrodeposition in High Aspect Ratio Trenches and Vias,"*J. Electrochem. Soc. 1998, 145(9), pp. 3070-3074.