TOMBSTONING OF 0402 AND 0201 COMPONENTS: "A STUDY EXAMINING THE EFFECTS OF VARIOUS PROCESS AND DESIGN PARAMETERS ON ULTRA-SMALL PASSIVE DEVICES"

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Background

The long-standing trend in the electronics industry has been the miniaturization of electronic components. It is projected that this trend will continue as Original Equipment Manufacturers (OEMs) and Electronic Manufacturing Service (EMS) providers strive to reduce "real estate" on printed circuit boards. Typically, the miniaturization of components can be achieved by integration or size reduction. At present, size reduction is considered to be more cost effective and flexible than integration. Passive components, which are used in limiting current, terminating transmission lines and de-coupling switching noise, are the primary focus in size reduction due to their variety of uses [4].

From a manufacturing stand point, the sizes of the ultra-small components pose significant challenges to the capability of the manufacturing equipment and the control over various process parameters. Plexus Electronic Assembly has investigated some of these issues, particularly associated with 0402/0201 devices and their tendencies to form tombstone defects. The purpose of this paper is to discuss: 1) the mechanism of tombstoning and design considerations, 2) the potential process parameters affecting tombstoning and 3) the results of a multi-level Design of Experiment (DoE) conducted using a Plexus-designed test substrate.

Tombstoning Effect

Of all soldering defects, tombstoning (also known as the Manhattan Effect, drawbridging or stonehenging) is the most common when soldering small passive devices. Tombstoning can be defined as the raising of one end, or standing up, of a leadless component from the solder paste. This phenomenon is the result of an imbalance of the wetting forces during reflow soldering. The self-centering force of the solder which helps to align off center components, is the same force which contributes to the tombstoning effect. In the case of small components, such as the 0402 and 0201 devices, a delicate balance exists between the surface tension of molten solder, the substrate and components. This balance can easily be disturbed with slight changes in solderability of all elements involved and

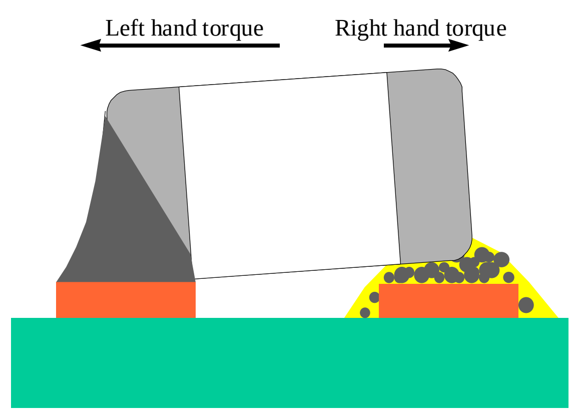


Figure 1: Beginning stages of tombstoning due to the force imbalance caused by temperature differences

by differences in the precise moment at which the solder at each end of the component begins to reflow. Figure 1 illustrates the beginning stages of tombstoning on a small surface mount package.

As Figure 1 indicates, the "right hand torque" refers to the effect of gravitational forces, which keep the component immobile, while the "left hand torque" refers to the forces of surface tension which pull the component upward. An energy balance model can be expressed as follows:

$$EnergyBalance(E_b) = \frac{\left(w \cdot h \cdot st \cdot \sin(theta)\right)}{\left(mg\left(l/2 + x\right)\right)}$$

Where:

w = Width of the component
h = Height of the component
st = Surface tension of solder
mg = Weight of the component
theta = Wetting angle
x = Vertical distance displacement of the component's center of gravity when rotated to its point of balance (see Figure 3)

In order to maintain simplicity, it is assumed that the solder paste on the open side does not have any effect on the component. Figures 2 and 3 illustrate the details of the different terms used in the energy balance equation. The key to understanding the use of the equation is that if the “left-hand” torque forces are greater than unity (E_B>1), then there is sufficient surface tension potential energy to raise the component past the highest potential energy point (see left hand side of figure 3), thus creating the tombstone.

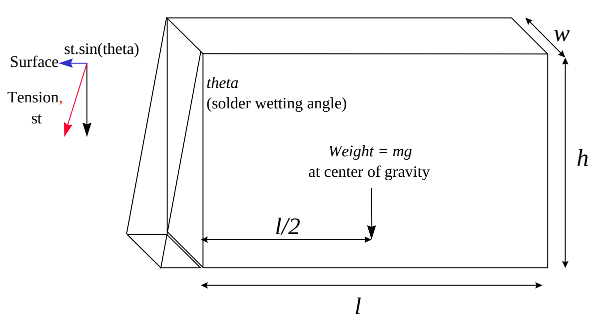


Figure 2: Terms used in the energy balance equation

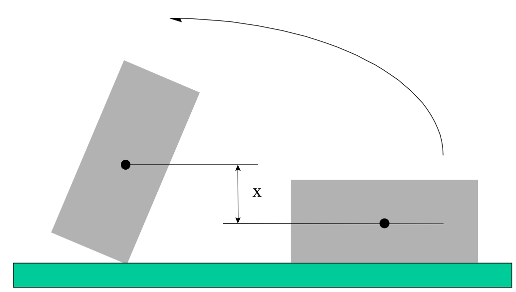


Figure 3: Illustration of the "X" term

Although the energy model is very crude, it is quite clear that as the component's size is reduced, the forces of surface tension become increasingly important, and the possibility of tombstoning increases. The size reduction from an 0402 to an 0201 component results in a reduction to about 1/8 of the volume and about 1/5 of the mass. In addition to the size of the component, the wetting angle of the solder is also an influential variable. The angle is particularly affected by the physics involved in wetting, the volume of solder and the pad geometry. Figure 4 illustrates the effect of size and wetting angle on the energy balance. As indicated, when E_b >1 the occurrence of tombstoning increases.

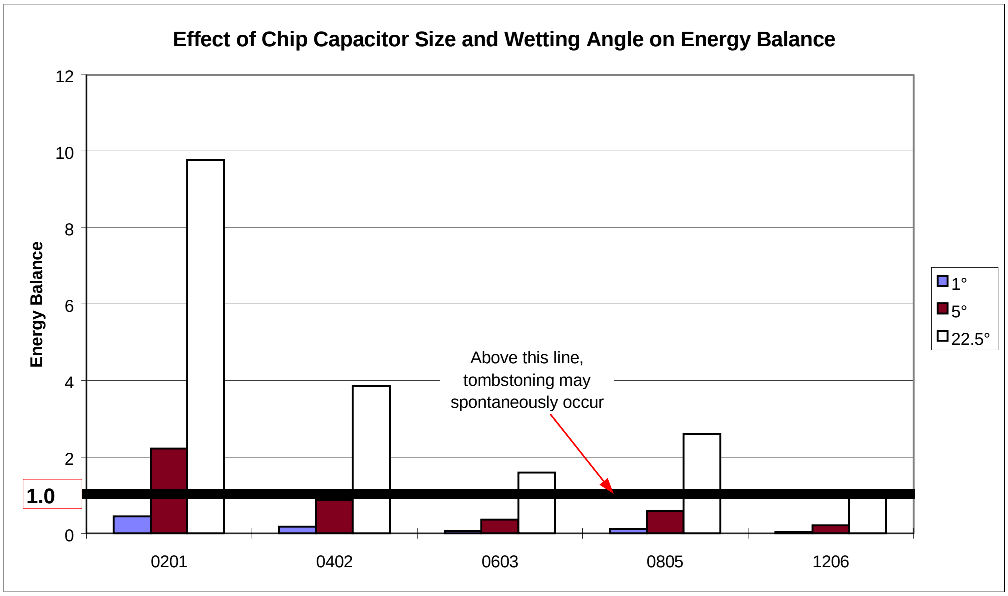


Figure 4: Energy balance for various component sizes

Potential Design and Process Parameters Considerations

Pad Designs

It has been proven that poor footprint design can directly contribute to the occurrence of tombstoning. To counter-balance the left-hand torque caused by the surface tension imbalance, the SMT footprint extension can be reduced to decrease the solder contact angle [5].

Home plate aperture stencil design has been shown to reduce the opportunity of depositing excess solder paste. It is well known that excess paste on the pads usually results in the formation of solder balls or solder beads during reflow. Studies confirm that the use of the home plate design has proven to be fairly efficient in controlling solder ball formation on regular passive devices. Therefore, it may be possible to utilize this same design on ultra-small passive components in order to obtain better control over the amount of paste placed on the respective pads, thereby reducing defects.

Solderability

In all soldering processes, the solderability of the component and the substrate are of prime concern. All surfaces must be readily solderable to ensure that the solder wets thoroughly during reflow. In particular, the type of board finish is considered, in most cases, to be the critical factor. Hot air solder leveling (HASL) has been used for many years as an effective solderable board finish. However, defect levels can be very difficult to maintain or reduce when driving towards smaller terminations due to the uneven topography associated with HASL finishes. As a result, more planar copper-surface coatings have come to the forefront. In recent years, organic solderability protective (OSP) coated circuit boards have become mainstream, along with a variety of metal platings such as old favorites like Au/Ni and newer technologies such as silver, palladium, and tin.

Solder Paste Deposition

Eutectic solder is commonly used in manufacturing due to its low melting point and unmatched physical properties. However, to prevent tombstoning in small components, some in industry suggest using a paste containing silver and antimony. It is speculated that the combination of these two metals can alter the solder paste's reflow characteristics and ultimately lead to decreased tombstone defects.

Other studies suggest that the rate of reflow can be affected by the solder paste particle size. Typically, type III (325-500 Mesh) is used in reflow solder operations. However, type IV may have its own advantages due to the decreased diameter of the solder/flux particles [3].

Reflow Conditions

The key concerns for the reflow process are the profile and soldering atmosphere. When the preheat slope, or ramp rate, of the reflow profile is too fast, the volatiles in the flux could evaporate rapidly causing a shift in the component's placement [5]. This shift in position could increase the likelihood of tombstoning. In addition to movement, the temperature difference along the length of the component, or thermal gradient, also affects the occurrence of tombstoning. It is known that the advantage of using a convection reflow oven over IR is the uniformity of temperature across the component and PCB. However, even with convection reflow, the potential for irregular reflow still exists.

Inerting reflow ovens with nitrogen has become commonplace. The effects of nitrogen during soldering have proven to be beneficial. The main advantage is improved wetting of molten solder and the reduction in the formation of oxides on the metal surfaces to be soldered [7]. However, the acceptable level of oxygen present inside the oven has been under scrutiny for the past several years.

Experimentation

In the past, efforts have been made by experts to develop dynamic mathematical models to capture the essence of the tombstoning phenomenon. Some recent developments involving the use of computer modeling have proven to predict the essential physical and mechanical causes of tombstoning fairly effectively. In spite of such advancements, process and design parameter impacts obtained through "real-world" manufacturing simulations are minimal. For this reason, this experiment was performed to provide such information.

Test Substrate Design

To further investigate the optimum footprint design for reducing tombstone defects of ultra-small components, a test vehicle was developed by Plexus Technology Group. Figure 5 represents the test vehicle developed for this study.

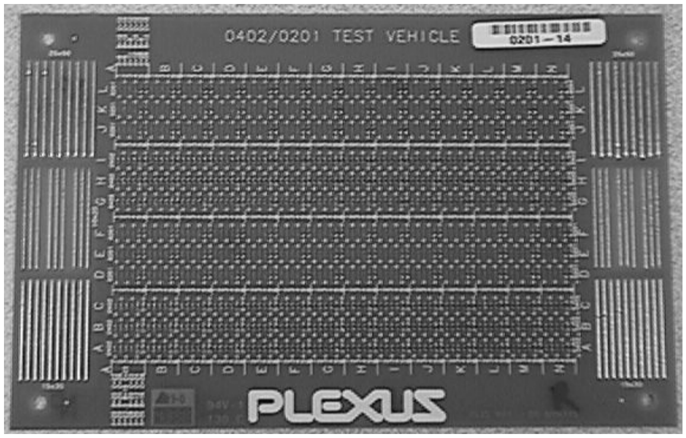


Figure 5: Test vehicle utilizing various pad designs

The test vehicle was designed in an effort to represent potential pad designs for small passive devices. Twelve different combinations of SMT footprint designs were incorporated to quantify the effect of pad design on tombstoning. The length, width and spacing of the pads were modified in accordance with Plexus' PCB design guidelines. Figure 6 summarizes the SMT footprint designs used in the study.

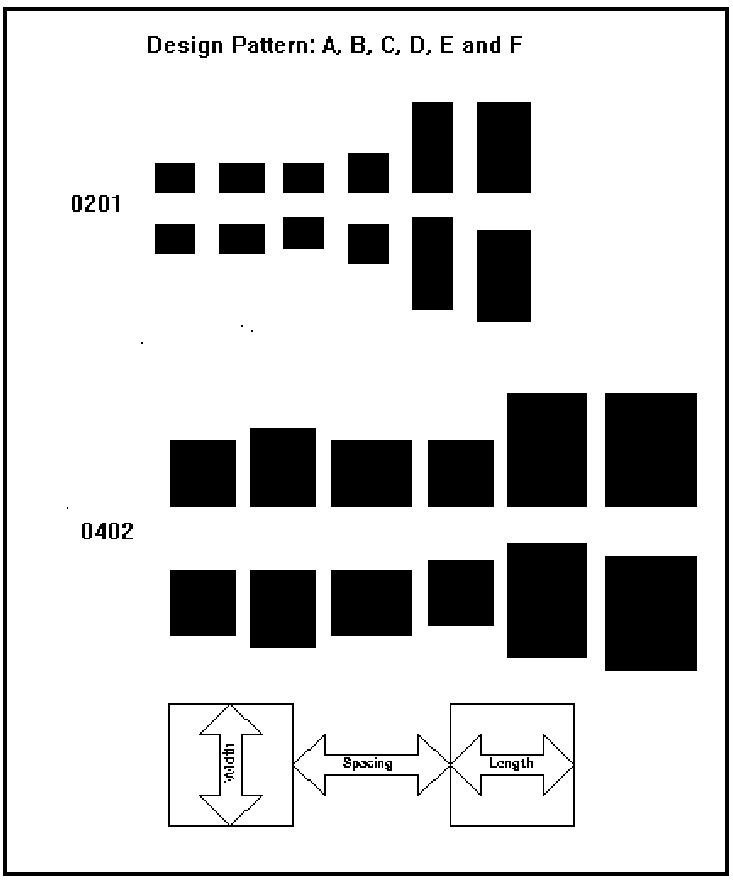


Figure 6: Summary of SMT footprint designs

Figures 7 and 8 illustrate some of the different pad designs, along with solder paste depositions for the 0201 and 0402 components, respectively.

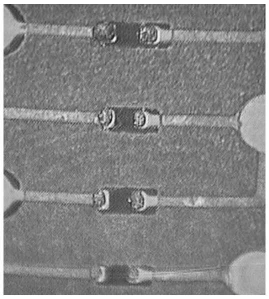


Figure 7: 0201 pad design

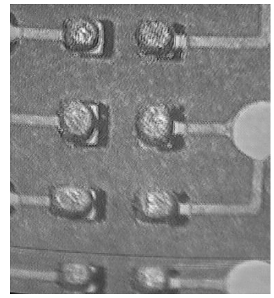


Figure 8: 0402 pad design

Due to the aspect ratio requirements of the stencil design, standard all-side reduction was used on all 0201 pads. Diagrams of all-side reduction and home plate pad designs used in this study can be seen in Figure 9.

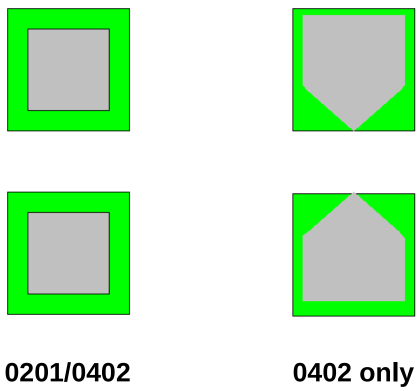


Figure 9: Visual of all-side pad reduction and home plate pad design

Solderability Test

To determine the solderability of the test vehicle, a more 'real-life' solderability approach was developed. This test is based on printing precise deposits of paste onto a series of long, copper-laminate areas bearing OSP coating. The five-mil thick deposits are 25 x 50 mils, 15 x 30 mils, and 10 x 20 mils, respectively, and are in rows separated by distances varying from 10 to 50 mils.

For the 25 x 50 mils and 15 x 30 mils apertures, the solderability data can be quantified by recording the largest gap that had been bridged for each data set. Figure 10 illustrates how the result of 30 mils/20 mils was obtained for the left/right side of the solderability test substrate. The data for the smallest sets of apertures, 20 x 10 mils, was interpreted by counting the number of non-bridged gaps observed, then dividing it by the total number of gaps.

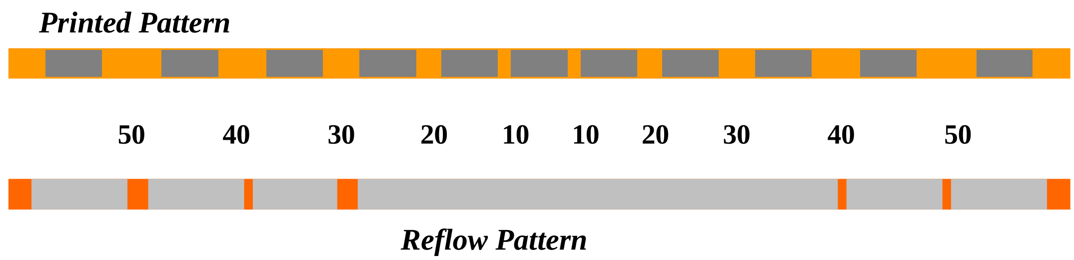


Figure 10: Solderability Determination

Design of Experiment

In order to explore the impact of the aforementioned areas, a full factorial design array was created using parameters and associated levels which were considered to be directly related to tombstoning. Table 1 summarizes the parameters used in this DoE.

Table 1: Parameters and levels used in the DoE

DoE Label	Parameters	Level 1	Level 2	Level 3
A	Preheat Slope	Regular Preheat	Rapid Preheat	N/A
B	Pre-Conditioning	No Reflow	After Single Reflow	N/A
C	Oxygen Level	Air	Medium O_2	Low O_2
D	Paste Type	Type III	Type IV	N/A
E	Solder Paste Brand	Brand A	Brand B	N/A

The parameters include preheat ramp rate, preconditioning of the boards, oxygen level, solder paste type and solder paste. All parameters used in the DoE were considered to be the most critical and the most easily changed in the manufacturing process. In the design, all parameters, with the exception of the oxygen level, were assigned to two levels. As table 2 indicates, oxygen was assigned at three levels. The different levels of each parameter were either determined from the vendors (nitrogen or paste supplier) or by "real-life" production experience.

In this DoE, two levels for the preheat slope were selected. The low and high levels were determined to be approximately 1.25°C/sec ("regular") and 2.3°C/sec ("straight"), respectively. Figures 11 and 12 represent the profiles used in the experiment.

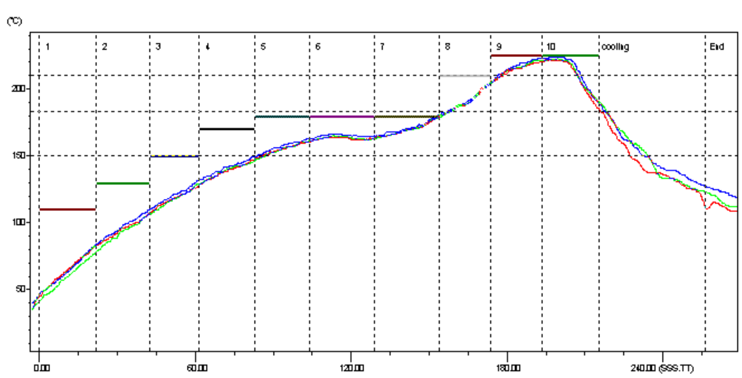


Figure 11: The "regular" profile with a slope of 1.25°C/sec

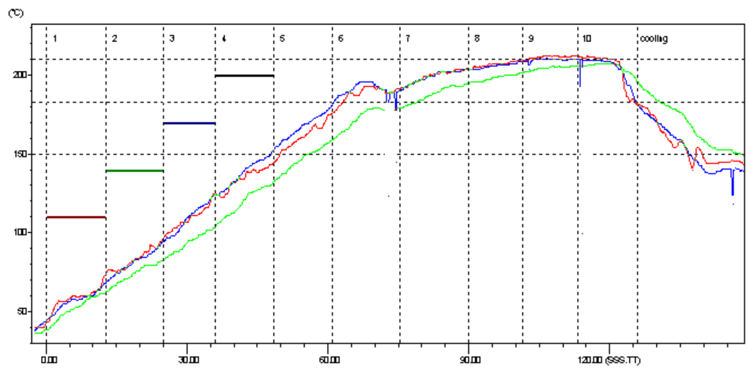


Figure 12: The "straight" reflow profile with a slope of 2.3°C/sec

The next selected parameter is preconditioning. Preconditioning of the boards refers to whether or not they have been exposed to a thermal cycle prior to the SMT process. The low level consisted of not exposing the boards to reflow, while the boards processed at the high level were exposed to one reflow cycle in a nitrogen rich environment. This "preconditioning" step is to best simulate real life situations for boards with double-sided reflow technology.

Since oxygen level is a significant factor affecting soldering, it was included as a parameter with three levels instead of two. Three levels were chosen based on recommendations from Praxair, Inc.: Air (210,000 ppm O_2), 500 ppm O_2, and <100 ppm O_2.

Finally, two pastes with differing metal composition and particle size were used to determine the effects on tombstoning. Paste Brand A is a typical eutectic solder, while paste Brand B contains percentages of silver and antimony. Furthermore, to examine paste deposition characteristics between different solder particle sizes, both type III and type IV pastes of each brand were used.

In this multi-level design, the significant parameters and associated levels were investigated for their effects on tombstone formation. The design array was set up as full factorial (48 test combinations) in order to free the main factors from confounding with any interactions [2]. To obtain a measure of experimental error, two identical sample sets were processed for each test combination. The test substrate, which was discussed previously, was used as the test vehicle for all runs. The full factorial array design is included at the end of this paper.

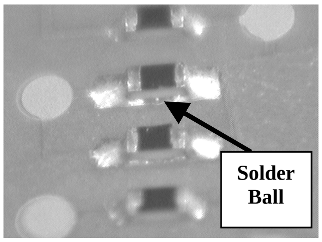
The tests listed in the array were conducted randomly. This randomization reduces or minimizes the experimental error when certain factors not included in the experiment cannot be controlled. A visual inspection of the soldered components was performed upon completion of all test combinations. The visual inspection for component tombstoning was used as the response variable.

Results and Discussion

A total of 48 different test combinations were examined during the experimentation. This resulted in the soldering of approximately 50,000 components. The data collected in this experiment was entered into statistical software for analysis. Results were analyzed and summarized separately between substrate design, solderability testing and DoE analysis.

Effects of Substrate Design

Although it was speculated that home plate stencil design improves process yield of passive devices, the data revealed that there is no significant improvement in process yield. As expected, it was noted that solder balls or beads up to 2 mils in diameter were found nearby some 0402 components without the home plate design. Figure 13 illlustrates the solder beads observed.



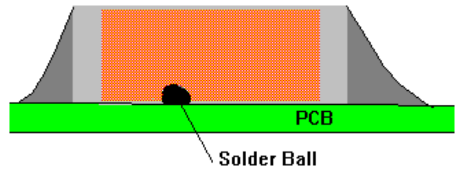


Figure 13: 0402 parts with solder bead

In the case of the 0201 components, grossly oversized pads were found to be the dominating factor for tombstoning. In agreement with the energy equation, and as Figure 14 indicates, the 0201 footprints with extended length appear to be a more tombstone-prone design. Surprisingly, the defect rate of the 0402 components appears to be insensitive to the suggested changes in pad design (see Figure 15).

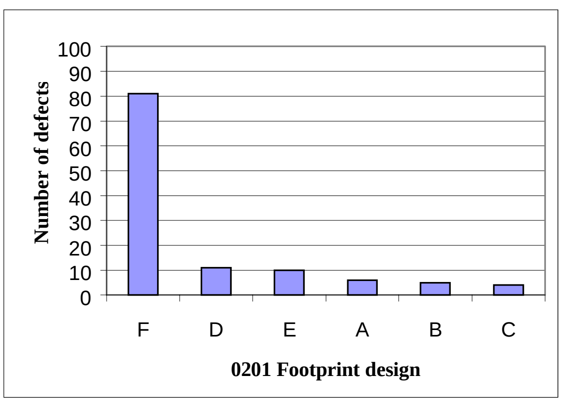


Figure 14: Number of 0201 defects vs. pad designs

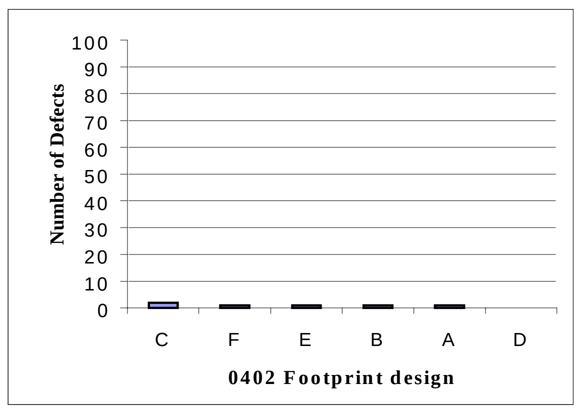


Figure 15: Number of 0402 defects vs. pad designs

Solderability Test Results

The trends observed from the three different types of aperture/gap are very similar. For the sake of brevity, only the results from the 25 x 50 mil apertures will be discussed. However, the data from the other two types of solderability tests showed very similar behavior. Analysis of the extent of solderability onto the OSP surface shows that by far, the most crucial control variable is the oxygen content of the reflow atmosphere. Comparing the average results for all trials conducted at the three oxygen concentrations, it is clear that there is a very large difference between solderability in air and at about 500 ppm oxygen. However, at 500 ppm oxygen, the upper limit of the solderability test method was reached, making it is impossible to differentiate whether there was a further increase in solderability to OSP as the oxygen concentration decreases to below the 100 ppm oxygen level. The effects of preconditioning, profile type, particle size and paste manufacturer/flux showed some slight trends, but the effect of oxygen content was by far the greatest. Table 2 and Figure 16 summarize and illustrate the OSP-solderability trends.

Table 2: Solder ability trends matrix - Mean largest gap wetted out (mils)

Variable	1	2	3
Oxygen Concentration	20.2	49.4	49.4
Paste	39.3	40.0	N/A
Particle Size	39.2	40.1	N/A
Pre-Conditioning	40.2	39.1	N/A
Preheat Slope	38.5	40.8	N/A

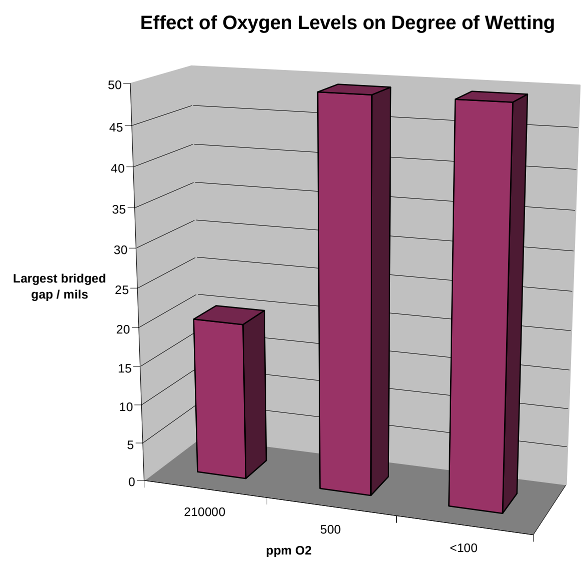


Figure 16: Solderability of 25 x 50 mil apertures as a function of oxygen level

Significant Factors

The DoE data collected from 48 test runs was entered into statistical software for analysis. In order to confirm the assumption of normality, a normal probability plot was developed for the residual values of each observed data set. It should be noted that one particular residual was much higher than the remaining data points. After careful investigation, the outlying response was discarded due to experimental error. An analysis of variance (ANOVA) was conducted to determine the significant factors (p-value ≤ 0.05). The ANOVA revealed that A, B, and D (A = Preheat Slope, B = Pre-conditioning, D = Paste Type) were the significant factors affecting tombstoning in the experiment. The main effects plot shown in Figure 17 suggests that the frequency of tombstoning increases as the preheat slope increases, and also when the OSP finish has been pre-conditioned. In addition, the plot clearly defines solder paste size type IV as having the most significant impact in reducing tombstone defects.

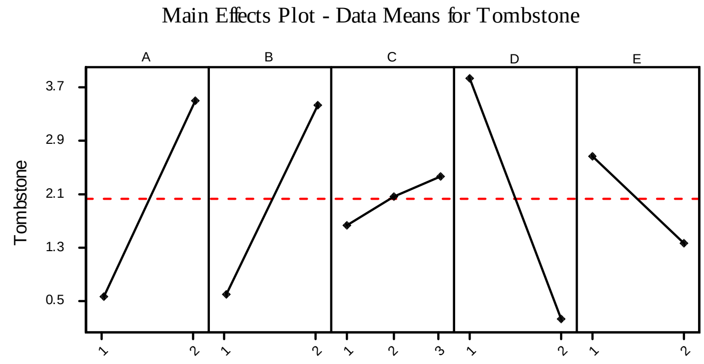


Figure 17: Main effects plot for the parameters tested

An interaction plot was developed to further illustrate the relationship between the factors. This plot can be seen in Figure 18.

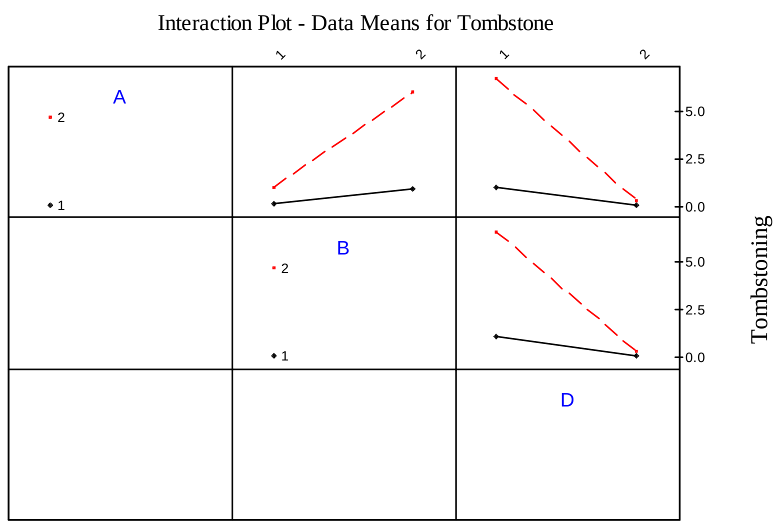


Figure 18: Interaction plot of the parameters

The ANOVA table revealed that combinations of the following parameters reduce the number of tombstone defects:

- ❖ Low preheat and type IV solder paste
- ❖ Good solderability finish and low preheat
- ❖ Good solderability finish and type IV solder paste

It is important to note that all of the given parameters named in the interaction effects analysis were also the significant main effects. Therefore, it appears that the main effects, in combination, affect the tombstone phenomenon profoundly.

Reflow Profile

As expected, the increase in preheat slope appears to be a significant factor in this DoE. This supports the industry belief that the main cause of tombstoning is due to the solder at both ends changing phase from solid to liquid at different times. The data collected shows that the preheat slope of 2.3°C/min plays a pivotal role in the formation of tombstones. As the slope increases, the likelihood for solder to reach the melting point at different times also increases.

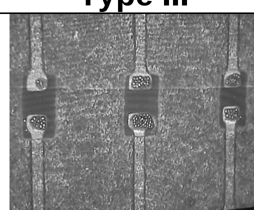
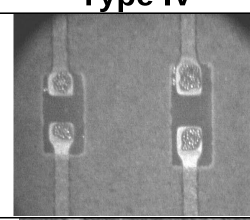
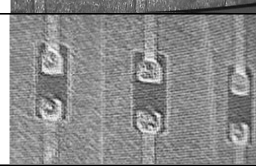
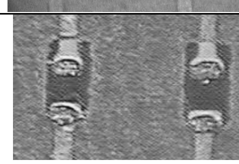
Preconditioning

Even though the OSP finish is designed for multiple reflow cycles, the solderability of the surface finish is reduced as it is exposed to reflow conditions. The result of preconditioning as a significant factor in tombstoning is totally unexpected. This indicates that components on double-sided reflow technology assemblies will have an increased chance of tombstoning.

Type III vs. Type IV Particle Size

Even before all of the test combinations were completed, it was obvious that the print quality of type IV paste is significantly superior to that of the type III paste. Table 3 illustrates some of the print patterns of the 0201 pads. Note that the solder deposition patterns of type III paste were quite irregular.

Table 3: Solder paste deposition comparison for the two pastes

	Type III	Type IV
Solder Paste A		
Solder Paste B		

Solder Paste Brand

Statistically, the solder paste brand containing the silver and antimony was not shown to be a significant factor in this DoE. Therefore, the conclusion that these metals reduce tombstoning by providing a slower and more even paste melt cannot be substantiated by the evidence provided.

Other Observations

In addition to the presence of tombstone defects on select test boards, it was noted that excessive no-clean flux residues were found around some 0402 components (see Figure 19).

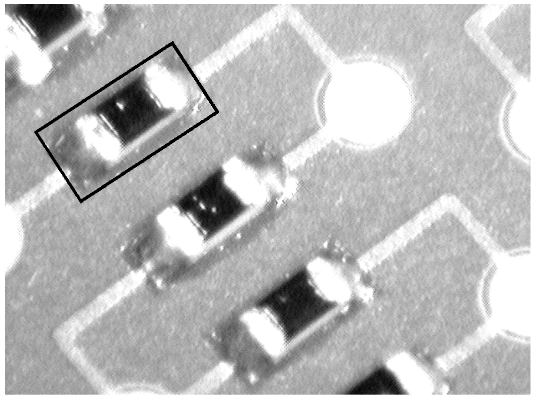


Figure 19: Excessive flux residue on 0402 components

The residue amount detected was found to be more severe on boards that had been reflowed in air. This finding agrees with other nitrogen reflow studies, which indicate that excessive flux residue is primarily associated with rosin and the presence of oxygen.

Conclusion

The results of the DoE suggest that paste type, preheat slope and surface finish conditions are the significant parameters associated with tombstoning. Provided the process parameters are being monitored and controlled properly, the ultra-small passive component placement and soldering process can be very robust. Based on the information gathered from this project, when using ultra-small passive components such as 0402 and 0201, the following practices should be encouraged to prevent tombstoning:

1. Select components and PCBs with consistent solderability.
2. Use solder paste with fine solder particles to increase tackiness and improve print definition.
3. Optimize the thermal profile to reduce the potential temperature differential between terminations.

Although nitrogen was not found to be a significant factor affecting tombstone defects in this study, evidence of increased wetting and reduced soldering residues were observed with the inerted reflow environment. This observation is consistent with several studies conducted by industry experts.

The results of this study will be utilized by Plexus in its manufacturing processes during the assembly of PCAs containing ultra-small passive devices. Furthermore, as with any process, continual improvements and optimization of the equipment and its parameters will occur to produce quality defect free assemblies and to remain on the leading edge of technology.

Future Works

This paper focuses on delivering a process recipe to place and solder ultra-small components free of tombstone defects. During this experiment, additional observations were made regarding process parameters and their effects. Although these observations were not part of this tombstone defect analysis, they are equally important and will need to be further examined in subsequent studies. These issues include:

- Formation of solder ball or solder bead
- Formation of no-clean flux residue
- Component movement
- Correlation of paste volume with aperture opening
- Wetting on OSP finishes

Acknowledgments

The authors would like to thank the following individuals for their contribution to this project: Bill Barthel, Bill Capen, Derek Dettlaff, Nancy Diehl, Steve Donkle, Bill Eck, Andy Hilbert, Gary Lembcke, Mike Pulvermacher, Greg Voss. In particular, we would like to express our gratitude toward the cooperation of our suppliers, the Plexus ProtoCenter™, Jeff Weinstein of Radix and MuRata State College, PA, for their gift of 0201 components.

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Appendix: Full Factorial Array

StdOrder	Reflow Profile	Pre-condition	Oxygen level	Paste Type	Paste brand
30	2	1	2	1	2
40	2	2	1	2	2
2	1	1	1	1	2
41	2	2	2	1	1
48	2	2	3	2	2
42	2	2	2	1	2
27	2	1	1	2	1
14	1	2	1	1	2
16	1	2	1	2	2
15	1	2	1	2	1
19	1	2	2	2	1
9	1	1	3	1	1
34	2	1	3	1	2
22	1	2	3	1	2
46	2	2	3	1	2
45	2	2	3	1	1
36	2	1	3	2	2
32	2	1	2	2	2
7	1	1	2	2	1
17	1	2	2	1	1
1	1	1	1	1	1
29	2	1	2	1	1
21	1	2	3	1	1
38	2	2	1	1	2
35	2	1	3	2	1
20	1	2	2	2	2
23	1	2	3	2	1
25	2	1	1	1	1
10	1	1	3	1	2
44	2	2	2	2	2
31	2	1	2	2	1
39	2	2	1	2	1
18	1	2	2	1	2
26	2	1	1	1	2
13	1	2	1	1	1
6	1	1	2	1	2
11	1	1	3	2	1
5	1	1	2	1	1
28	2	1	1	2	2
12	1	1	3	2	2
24	1	2	3	2	2
33	2	1	3	1	1
8	1	1	2	2	2
43	2	2	2	2	1
4	1	1	1	2	2
3	1	1	1	2	1
47	2	2	3	2	1
37	2	2	1	1	1