Issues and Challenges of Testing Modern Low Voltage Devices with Conventional In-Circuit Testers

Alan J. Albee
Teradyne
North Reading, MA
alan.albee@teradyne.com

Abstract
The popularity of low voltage technologies has grown significantly over the last decade as semiconductor device manufacturers have moved to satisfy market demands for more powerful products, smaller packaging, and longer battery life. By shrinking the size of the features they etch into semiconductor dice, IC manufacturers achieve lower costs, while improving speed and building in more functionality. However, this move toward smaller features has lead to lower breakdown voltages and increased opportunities for component overstress and false failures during in-circuit test.

The chief reason is that testers designed for boards that traditionally operated with a power supply voltage of 5V are still being used on new generation ICs, which operate on 2.5V, 1.5V, or even 0.8V. These traditional in-circuit testers often do not have the accuracy, safety, and reliability features that are required to test low voltage technologies.

This paper discusses the challenges of performing powered-up vector testing of low voltage technologies on traditional in-circuit testers and describes the safeguards that are necessary to ensure that test vectors do not violate the increasingly tight specifications of low voltage parts.

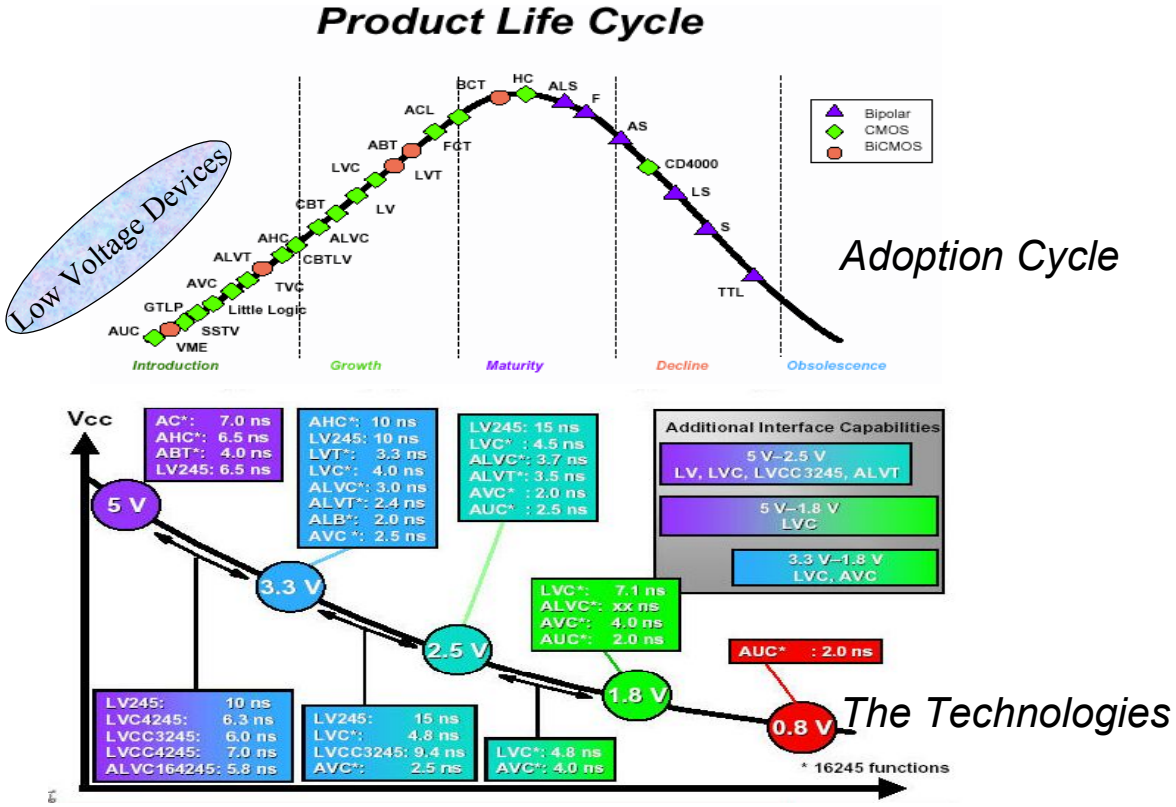
It also describes the in-circuit test features that are most important for testing low voltage technologies: independently programmable, high accuracy driver/sensors; real time dynamic backdrive current measurement, programmable backdrive control, specialized digital controller; and multiple level digital isolation.

Introduction
Low Voltage semiconductor devices have design benefits that include lower power consumption, reduced cooling requirements, and faster processing speeds. These benefits have made it possible for the performance of the PC to increase over 400-fold in the past 18 years, even though the energy consumed by the PC has remained largely unchanged. [1]

The use of 5V VCC had long been the standard for both core and memory logic. However, the increasing complexity and functionality of application-specific integrated circuits (ASICs), microprocessors, and digital signal processors (DSPs), have resulted in modern CMOS manufacturing processes that produce smaller structures where the thickness of the gate oxide of each single transistor is sensitive to electrostatic field strength. Because the field strength is proportional to the supply voltage, the supply voltage must be reduced for reliable operation of the smaller structures.

Put another way, making electronic devices more complex, without enlarging the overall size of the chip area, requires reducing the structure size, which also requires reducing the VCC power supply voltage. The limit for reliable operation at less than 5V is reached at a structure size of 0.6 micron, and the use of a 0.35-micron manufacturing process requires 2.5V VCC for proper operation. Reducing the power supply voltage also produces an exponential decrease in power consumption; therefore, the trend is to reduce power-supply voltages. [2]

The technology roadmaps of the major semiconductor manufacturers show that logic voltage thresholds have been steadily declining over the past decade. Figure 1 shows the progression of low voltage components introduced by Texas Instruments over the last decade from 5V to 3.3V to 2.5V, all the way to 0.8V. It also shows that the majority of their low voltage components fall into the Introduction and Growth product life categories, while their higher voltage components generally fall into the Maturity and Decline product life categories.

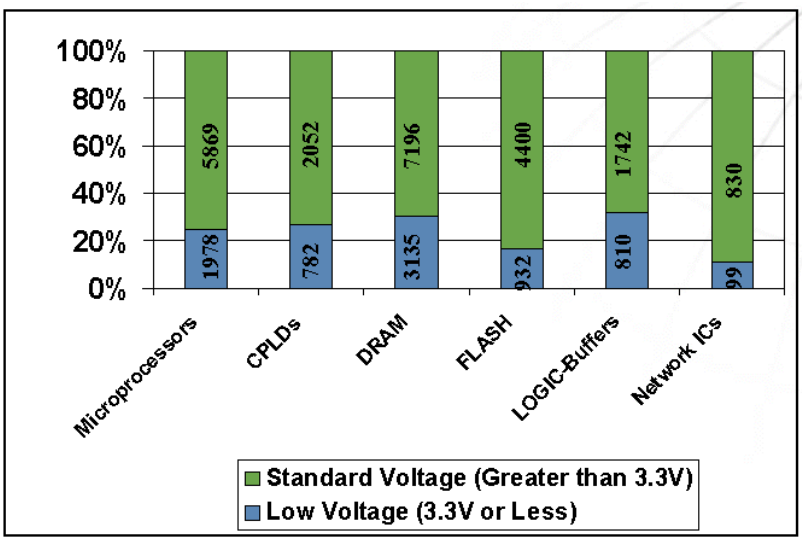


Source : Texas Instrument Technology Roadmap

Figure 1: Logic Level Technology Trends

This trend is likely to continue in the industry as Intel has announced that they are working on 90nm and 45nm processes for their next generation processors and chipsets. These small processes are likely to make low voltage components even more susceptible to damage from over-current and over-voltage test conditions.

Figure 2, based on data from the 2003 IC Master, shows that low voltage components are available in every IC product category, and that they make up a significant percentage of the total number of commercial IC components that are being actively sold. Finally, Table 1 shows that 4 different low voltage logic levels are currently being used by Intel's Pentium chipset.



Source: 2003 IC Master (www.icmaster.com)
Obsolete ICs not included in device totals

Figure 2: Number and Percentage of Commercial Low Voltage Components by Category

Table 1: Common Logic Levels used on Intel PC Architecture

Intel PC Bus	Logic Level
Front/Processor Side Bus	1.2V
AGP 3.0	1.5V
Hub Interface	1.5V
DDR SRAM	2.5V
Rambus	1.8V

Challenges of Testing Low Voltage Technologies with In-Circuit Testers

In-circuit testers rely on bed-of-nails type fixtures that give the tester instruments electrical access to every node (or net) of the printed circuit board (PCB). Using this access, the tester takes a "divide-and-conquer" approach, testing each component as if it were the only component on the assembled PCB. If all the individual component tests pass, then it is likely that the board is free of assembly faults and will function correctly in its target application. This test strategy is possible because the tester uses techniques like ***disables*** and ***inhibits*** to isolate the component being tested from the unwanted electrical effects of the components that surround it.

To perform powered-up vector testing of digital components, the tester uses driver/sensor (D/S) pins capable of driving the input pins to the required logic states and sensing the resulting logic states of the output pins. The digital pin drivers are designed as low impedance voltage sources that can typically source or sink 600mA or more of current. This voltage source momentarily forces nodes on the board to the logic levels required by the test. This technique of temporarily overdriving component outputs to force a node to its opposite logic state is commonly referred to as ***backdriving.*** [3]

These powered-up vector testing techniques have been successfully used by in-circuit test equipment for more than 20 years. However, today's new low voltage technologies are increasingly difficult to accurately, reliably, and safely test using traditional in-circuit testers. The reasons for this are related to the inaccuracy of traditional in-circuit D/S pin designs, and the greater likelihood of violating increasingly tight maximum voltage and current specifications of low voltage technologies.

Drive and Sense Accuracy

To successfully test low voltage technologies, in-circuit drivers must be accurate enough to supply the logic high and low voltages that are expected by the device input pins. Likewise, the in-circuit sensors must be accurate enough to detect the difference between logic high and logic low voltages on the device output pins.

Most conventional in-circuit testers use a D/S design that consists of a rail driver and a simple comparator (like the AM26C32). This is a simple design that is low cost and easy to engineer because it consists of readily available commercial off-the-shelf parts. The rail driver design typically exhibits an output impedance of approximately 5 ohms and a no-load driver error of approximately 150mV. The sensor in this design will typically exhibit greater than 300mV of voltage input error.

More accurate in-circuit testers utilize a closed loop, custom ASIC design that greatly improves the accuracy of the driver and sensor resources in the tester. These designs are higher cost and require greater engineering effort, but they typically exhibit much lower output impedance (1 ohm or less) and smaller driver/sensor error (100mV or less).

Either D/S design is capable of adequately testing voltage technologies greater than 1.2V under no-load current conditions, however it can become impossible to test voltage technologies that are lower than 1.2V with the simple design due to the inherent inaccuracies in the pin sensor. Even higher voltage technologies become untestable with the simple design under backdriving conditions because of the high output impedance of the rail driver pin design.

Accuracy Under Backdrive Conditions

As previously mentioned ***backdriving*** occurs during digital in-circuit testing whenever an in-circuit driver needs to supply current to temporarily overdrive a component output that is in the logic state opposite to what the pin driver is trying to achieve. Backdriving is common and can occur due to circuit design conditions, fault conditions on the board, or missing isolation code in the test program.

An analysis of a typical in-circuit test program of a PC motherboard found that backdriving occurred during 17 of the 56 digital device tests and that a total of 156 backdriving events required greater than 50mA of backdriving current. The median backdrive current was 176mA, the highest backdrive current event required 600mA of backdrive current, and the longest backdrive duration was 2.5mS.

Backdriving of this magnitude can be problematic on in-circuit testers that use high output impedance rail drivers. This is because the voltage inaccuracy of the pin driver increases dramatically as backdriving current increases. Figure 3 shows the relationship between backdrive current and driver inaccuracy for both the high output impedance, rail driver pin design and the low output impedance, custom ASIC pin design.

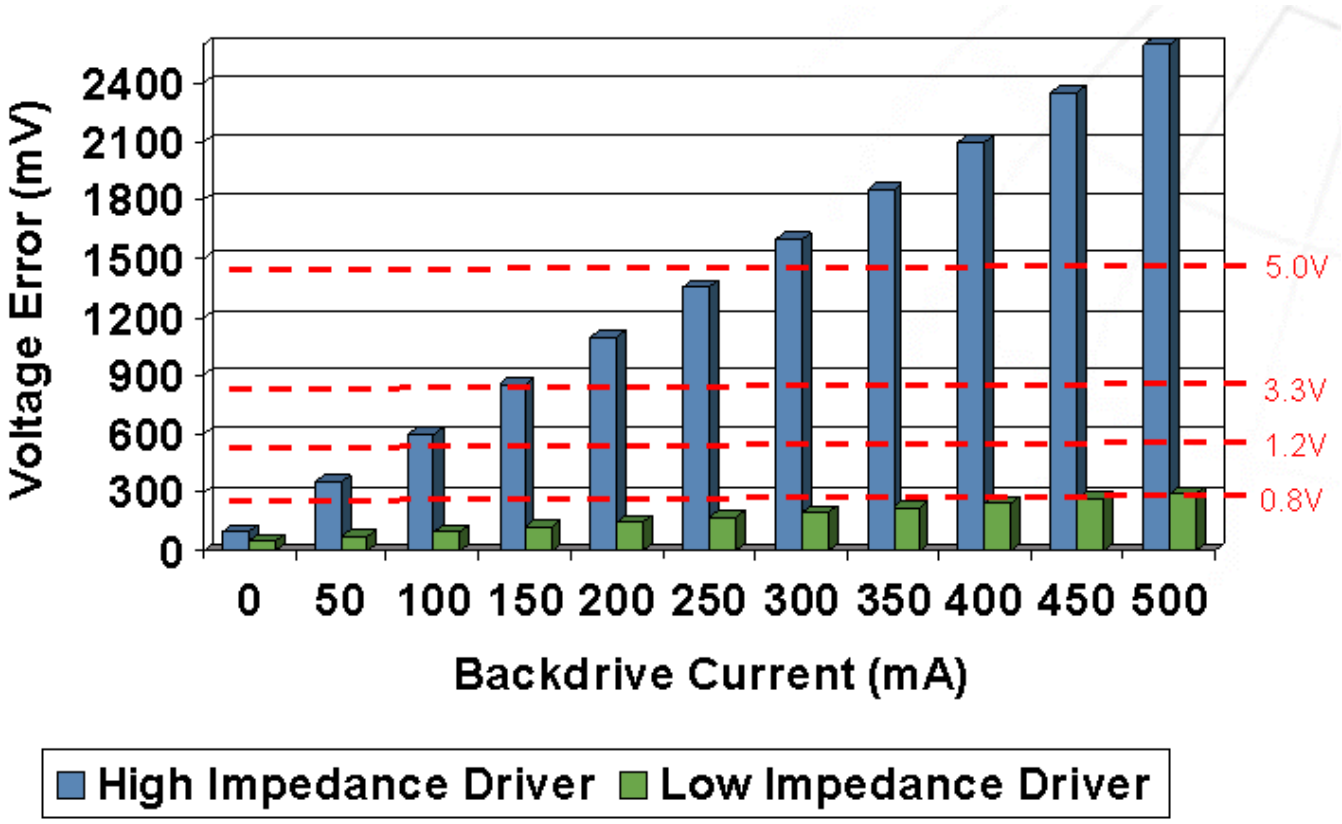


Figure 3: Driver Inaccuracy Increases as Backdrive Current Increases

The high impedance driver design loses voltage accuracy rapidly as backdrive current increases. At 100mA of backdrive current the driver is no longer accurate enough to test 1.2V logic technologies. At 200 mA of backdrive current the driver can no longer accurately test 3.3V technologies. When backdrive current exceeds 300mA the driver is not even accurate enough to test 5V technologies. At 500mA backdrive current the high output impedance driver exhibits over 2 volts of error. In contrast the low output impedance driver is accurate enough to test 0.8V logic technology even at backdrive currents up to 400mA.

Figure 4 demonstrates the performance of both high output impedance and low output impedance drivers captured in a lab experiment under backdrive and non-backdrive conditions. The waveforms show that the high output impedance driver programmed to drive 1.2 volts only achieves 0.58 volts when it is subjected to a 6 ohm load. In contrast, the low output impedance driver is able to achieve 1.07V under the same 6 ohm load conditions.

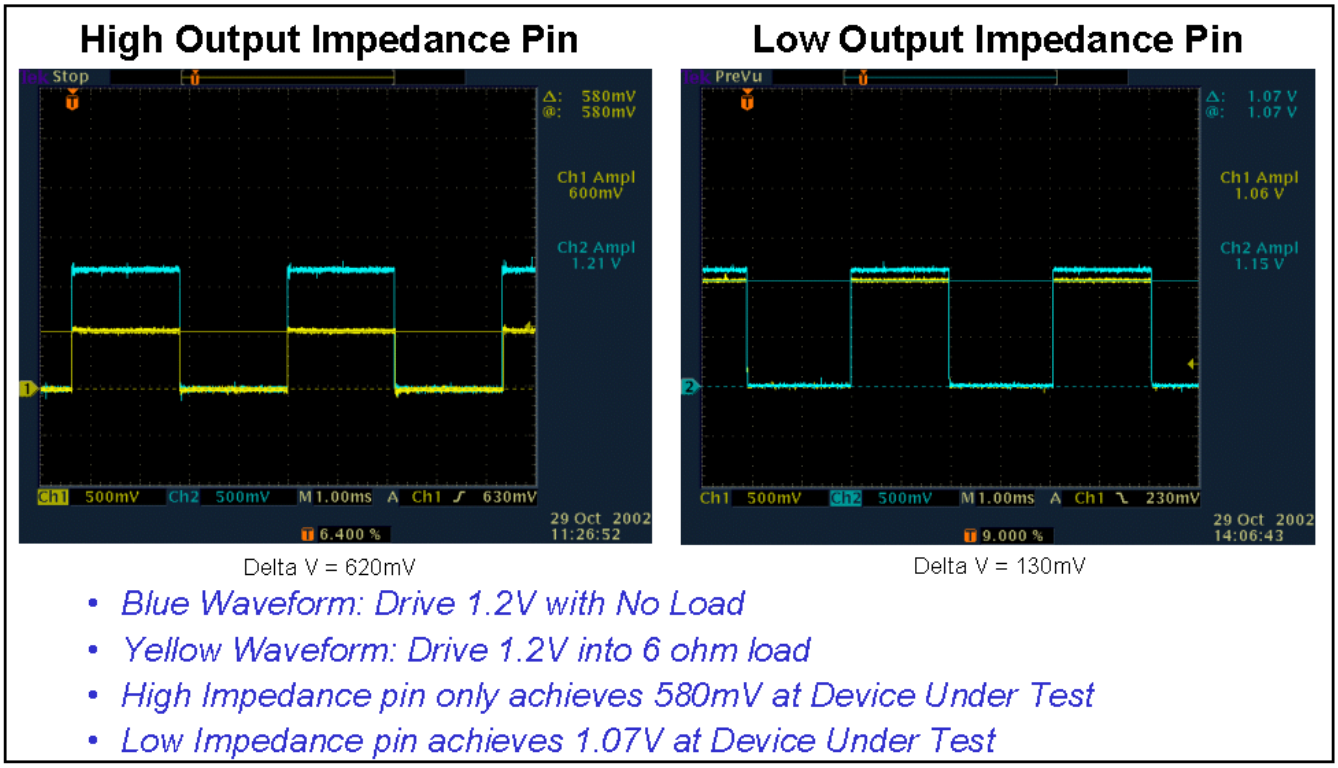


Figure 4: Driver Accuracy Comparison

Greater Susceptibility to Damage

Because of smaller device sizes and lower maximum voltage thresholds, low voltage technologies are more susceptible to the following types of failures.

Gate Oxide Breakdown

The smaller transistor gate oxide thickness required of low voltage technology components makes them more susceptible to damage when they are exposed to over-voltage conditions. The failure mechanism is known as TDDB (time dependent dielectric breakdown) and it is an interaction between time, temperature, voltage, and gate oxide width.

Gate oxide breakdown can occur when a device pin is driven to a voltage greater than its maximum specified rating. For example, the max specified voltage rating of Intel's FSB/PSB bus is 1.75V. If device pins on this bus are driven to voltages greater than 1.75V for an extended duration, then damage to the transistor gate oxide will occur.

Most traditional in-circuit testers are designed such that groups of D/S pins must share the same logic level assignments (groups of 16 or 32 pins are forced to use the same logic levels). This design is inexpensive, but it can lead to problems when D/S pins in the same group are connected to pins of different voltage technologies. When this occurs, programmers are forced to use common logic level assignments for all pins in the group, which can result in some low voltage device pins being driven beyond their maximum specified voltage ratings.

Overvoltage conditions are also more likely to occur on in-circuit testers that use high output impedance drivers because programmers may increase programmed voltages to try and compensate for the voltage inaccuracies that occur when a pin driver is backdriving. Figure 5 shows an example of an application where this could occur.

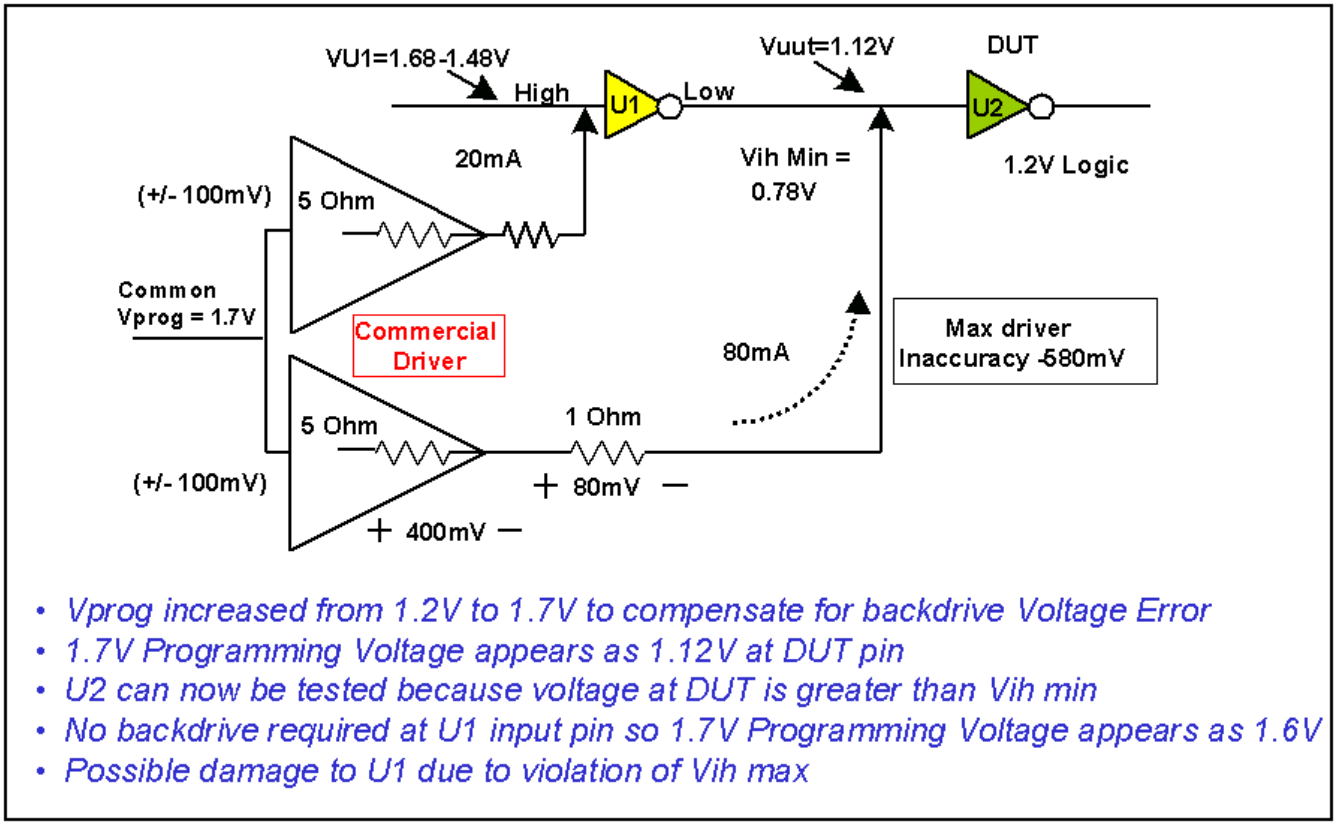


Figure 5: Shared Logic Level Assignments Causing Overvoltage Condition

More sophisticated in-circuit testers avoid these potential problems by having more accurate D/S pins and by designing the drivers so that assigned logic level thresholds can be programmed independently for each pin. This per-pin programmability eliminates test compromise situations that can cause device pins to be inadvertently driven beyond their maximum voltage ratings, and it ensures that each pin on the device is being driven to the exact logic level thresholds that are required by that device.

ESD Diode Overstress

ESD diode overstress is a failure mechanism that can occur on low voltage technologies when the ESD protection diodes are subjected to backdrive currents beyond a specified maximum. Some device manufacturers recommend that ESD diodes not be overstressed beyond 100mA of current. Exceeding these ratings can cause ESD diode damage that goes undetected by factory testing and can be source of latent failures in the field. Devices with ESD diode damage lack protection from Electrostatic Discharge that can degrade the performance of a device and eventually cause a catastrophic failure. [4]

Identifying and avoiding ESD diode overstress situations is impossible for most in-circuit testers. Only one in-circuit tester on the market has the capability to measure real-time dynamic backdrive currents, report where backdriving is occurring on the PCB, and program maximum backdriving current and time limits. Figure 6 shows an actual backdrive report from this tester that the operator can use to identify potentially harmful backdrive conditions.

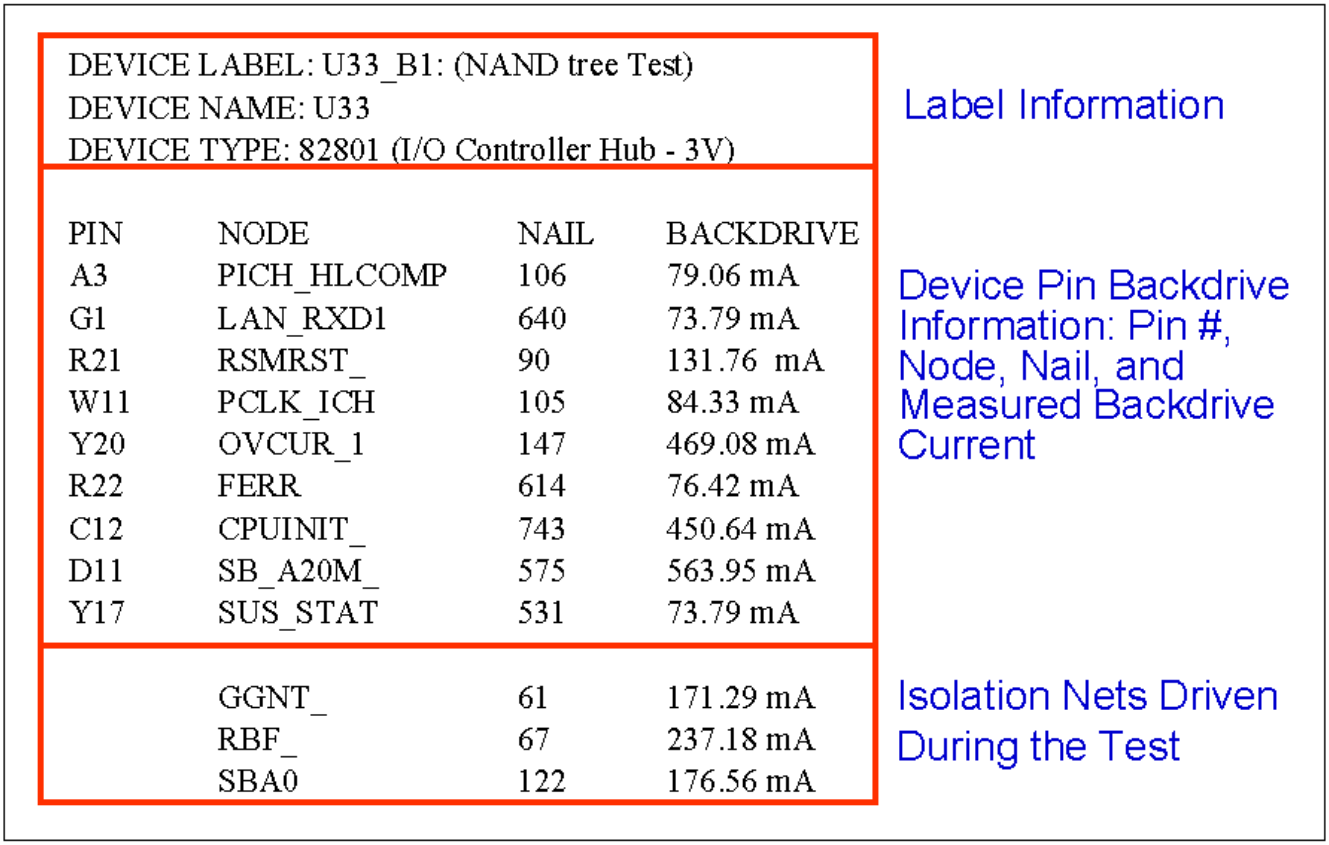
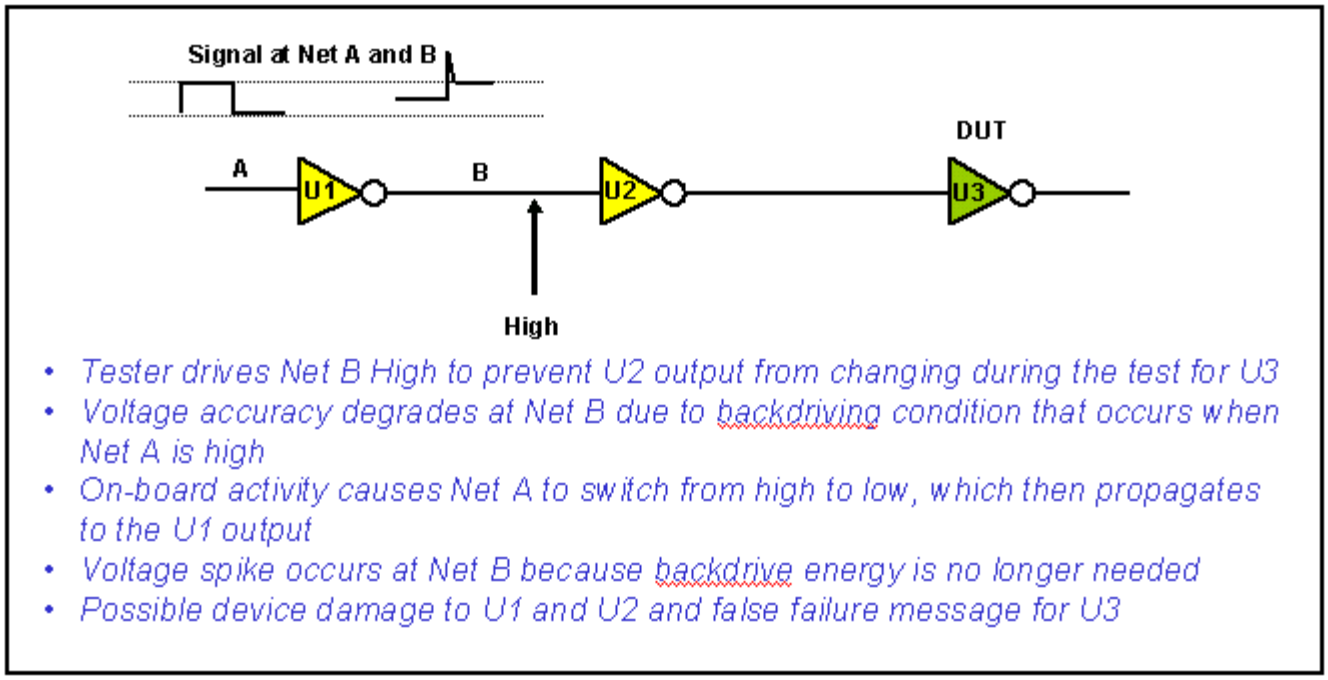


Figure 6: ICT Report Showing Backdrive Currents

CMOS Latchup

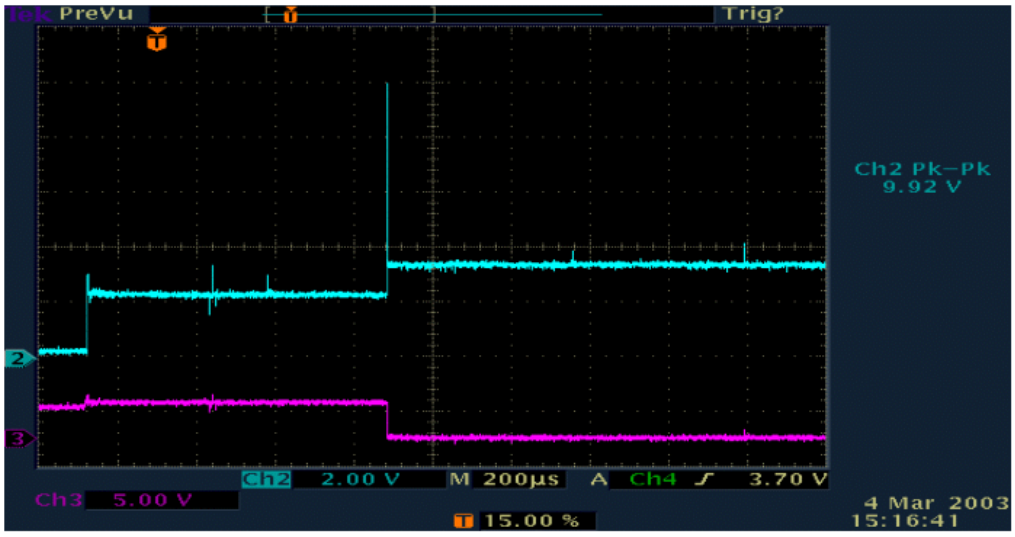
CMOS latchup is a failure mechanism that occurs when a pair of transistors forms a PNPN or NPNP silicon-controlled rectifier (SCR) type structure. This results in a low impedance, high current, path from power to ground in the device which can cause the device to malfunction or be permanently destroyed. Latchup is usually induced by the application of a fast rise or fall voltage spike to the inputs of the CMOS device. This can occur due to electrostatic discharge or during in-circuit testing when an output suddenly changes its logic state while it is being backdriven.

Figure 7 shows an application example that can cause voltage spikes to occur on device inputs during an in-circuit test. Figure 8 is a digital storage scope picture that shows the large voltage spike that can occur when outputs change logic state when they are being backdriven and how this can adversely affect the reliability of the test and the device itself.



- *Tester drives Net B High to prevent U2 output from changing during the test for U3*
- *Voltage accuracy degrades at Net B due to backdriving condition that occurs when Net A is high*
- *On-board activity causes Net A to switch from high to low, which then propagates to the U1 output*
- *Voltage spike occurs at Net B because backdrive energy is no longer needed*
- *Possible device damage to U1 and U2 and false failure message for U3*

Figure 7: Voltage Spike Caused by Output Switching During Backdrive



- *Trace 2 (Net B) shows high impedance Driver attempting to keep net high*
- *Trace 3 (Net A) starts out high, causing a backdrive condition on Net B*
  - *Net B driver fails to reach its programmed voltage because of backdrive condition*
- *On-board activity causes Net A to switch from high to low*
  - *Backdriving no longer required at Net B*
  - *Voltage spike of over 9V occurs on Net B due to stored Backdrive energy*
  - *Net B then returns to its programmed voltage value*

Figure 8: Voltage Spike Resulting from Output Changing During Backdrive

To prevent these potentially harmful voltage spikes from occurring during digital in-circuit testing, multiple level digital isolation techniques are required. The multiple level isolation techniques make sure that all outputs on a net are controlled and are in a known state prior to connection of a digital driver. Some in-circuit testers only isolate outputs that are directly connected to the inputs of the device under test, but as Figures 7 and 8 show, this is inadequate in preventing voltage spikes that could occur on nets that are not directly connected to the device under test.

Test Duration

Current flowing through a backdriven component increases the temperature of the component's output junction and bondwires. The maximum safe backdrive time for an IC is a function of the number of pins on the IC being backdriven, the current level, duration, packaging, and technology. Long backdrive times may cause a failure in a bondwire if it raises its temperature above the melting point or it may activate a fatigue mechanism in the bondwire that can cause latent defects and early life component failures. [5]

Therefore, it is important that in circuit testers keep test duration to a minimum whenever backdriving is occurring. Some in-circuit testers are designed with specialized digital controllers and memory behind the pin architectures that are very efficient at applying test vectors quickly and with precise timing. Less sophisticated in-circuit testers require longer test duration because test vectors are transferred from PC memory during the test. Timing for these testers is very unpredictable because it depends on the type of PC being used, the amount of data being transferred, and whatever else may be running on the PC. An experiment performed to measure the relative performance of the two approaches demonstrated that a tester without a specialized digital controller required 520 times longer than a tester with a specialized digital controller to execute 1000 test vectors (104ms compared to 0.2ms). This reduction in test execution time results in less stress on backdriven components and lowers the opportunity for occurrence of voltage spikes related to on-board activity.

Potential Impact of Low Voltage at ICT

There are many situations, as described above, where traditional in-circuit testers do not have the accuracy, safety, and reliability to test low voltage technologies. Manufacturers who choose to use these less capable in-circuit testers when testing low voltage technologies must deal with these adverse side affects.

Reduced Fault Coverage

If the ICT D/S pins are not accurate enough to drive and sense the low voltage technology pins, the manufacturer may decide not to test the component or they must use an alternative un-powered vectorless test technique like analog capacitive opens or diode junction tests to detect faults. These techniques are inferior to digital vector testing because they increase test time, increase test fixture cost and complexity, and cannot detect if the part is bad or malfunctioning.

Reduced Diagnostic Accuracy and Increased Chance of False Failures

Because of the inaccuracy of the drivers and sensors of traditional in-circuit testers, and the shrinking margin of error between logic high and low thresholds, there is an increased chance that good low voltage components will be indicted as bad. Figure 9 shows a faulty board condition that causes a traditional tester to incorrectly diagnose 3 good devices as bad, while at the same time failing to indict the real PCB fault. False failure diagnostics such as this increase manufacturing repair costs and cause unnecessary rework that could cause further damage to the PCB.

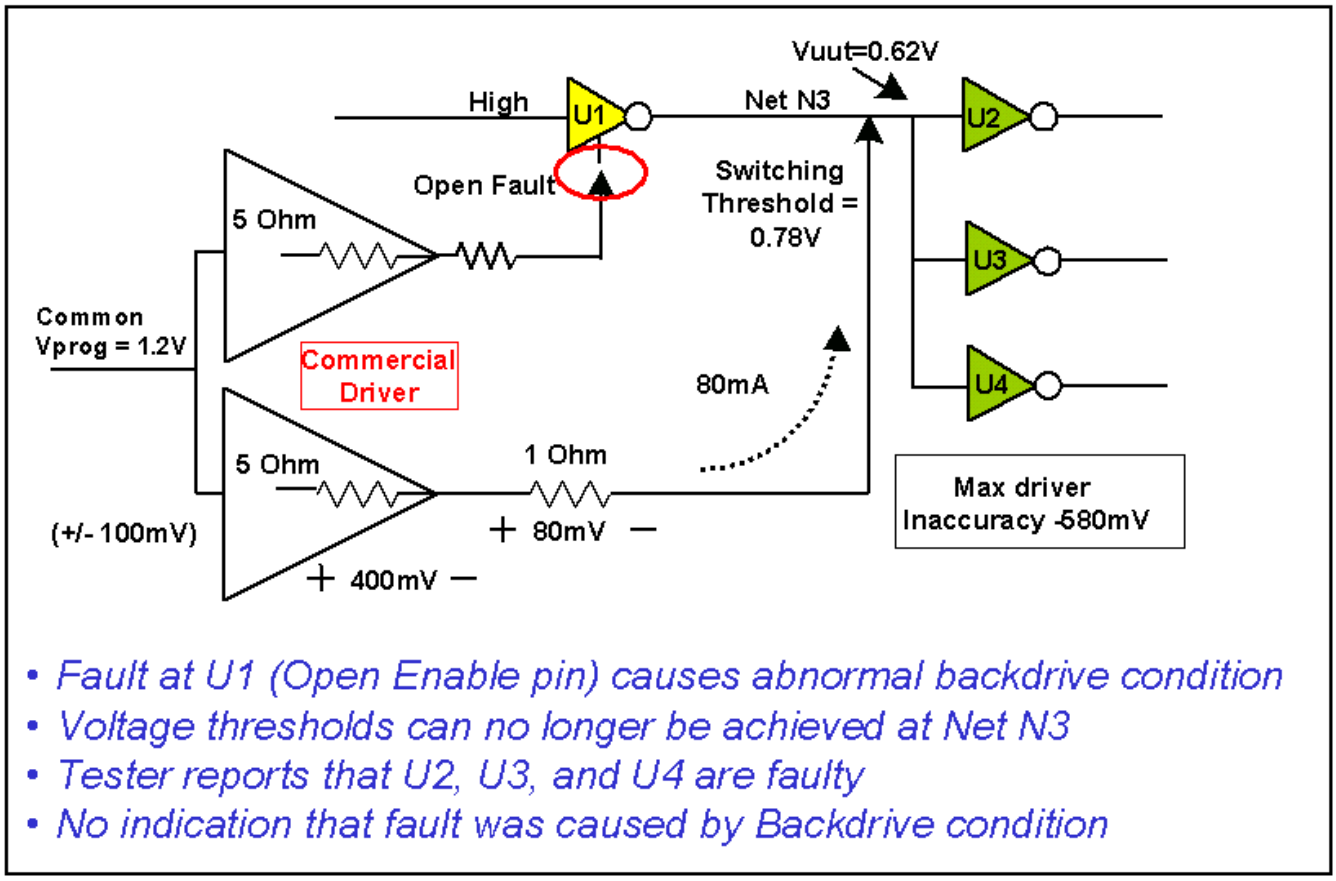


Figure 9: Fault Condition Causes False Failure Diagnostics

Safe Testing ICT Protection Technologies

Manufacturers who want to accurately, safely, and reliably test Printed Circuit Boards with low voltage technologies, should look for in-circuit test equipment that has the following capabilities.

Closed Loop, Low Output Impedance Drivers

In-circuit testers should have a specified driver accuracy below 100mV and output impedance of less than 1 ohm. This will guarantee the driver is capable of testing low voltage technologies as low as 0.8V and will ensure that the driver is accurate under no-load and backdrive conditions.

Accurate Sensor Resolution

In-circuit testers should have a voltage input error of less than 100mV. This will allow the tester to successfully distinguish between a high and low logic output for low voltage technologies below 1.2V.

Real-Time Backdrive Current Measurement Capabilities

In-circuit drivers should be able to perform real time measurements of backdrive currents and duration. This feature allows the tester to identify test conditions that require unusually large backdrive currents and it highlights areas of the test program that have missing or inadequate device isolation steps.

Programmable Backdrive Currents and Duration

In-circuit programmers should be able to set the maximum backdrive current and time that is allowed on each device pin during its test. This can be used to protect sensitive device technologies from being overstressed when there is a fault condition on the board. This feature can also be used to identify faults that are not normally detected by traditional in-circuit testers (like faulty enable pins and marginal output transistors).

Per Pin Programmable Logic Level Assignments

In-circuit D/S pins should allow individual, rather than group, programming of logic level thresholds, backdrive limits, and slew rates. Per pin programmable D/S capabilities allow the programmer and test generation software to assign logic levels that are appropriate for each pin on the device and avoids test compromises like those shown in Figure 5 that can occur on in-circuit testers that must share logic level assignments.

Specialized Digital Controller and Timing

In-circuit testers should have dedicated digital controller hardware that is capable of quickly executing digital test vectors with consistent and repeatable test timing. Testers with specialized digital controllers benefit from faster digital test throughput, less component backdrive stress, and more repeatable test results.

Multi-Level Digital Isolation

Finally, in-circuit testers should have test generation and circuit analysis software that automatically disables or inhibits any outputs on the PCB that are connected to nets that are being driven. This capability is critical to avoiding potentially harmful voltage spikes shown in Figure 8 that occur when an output being backdriven suddenly changes its logic state.

Figure 10 shows how multi-level digital isolation software would analyze a circuit and then condition it so that the device under test can be safely tested.

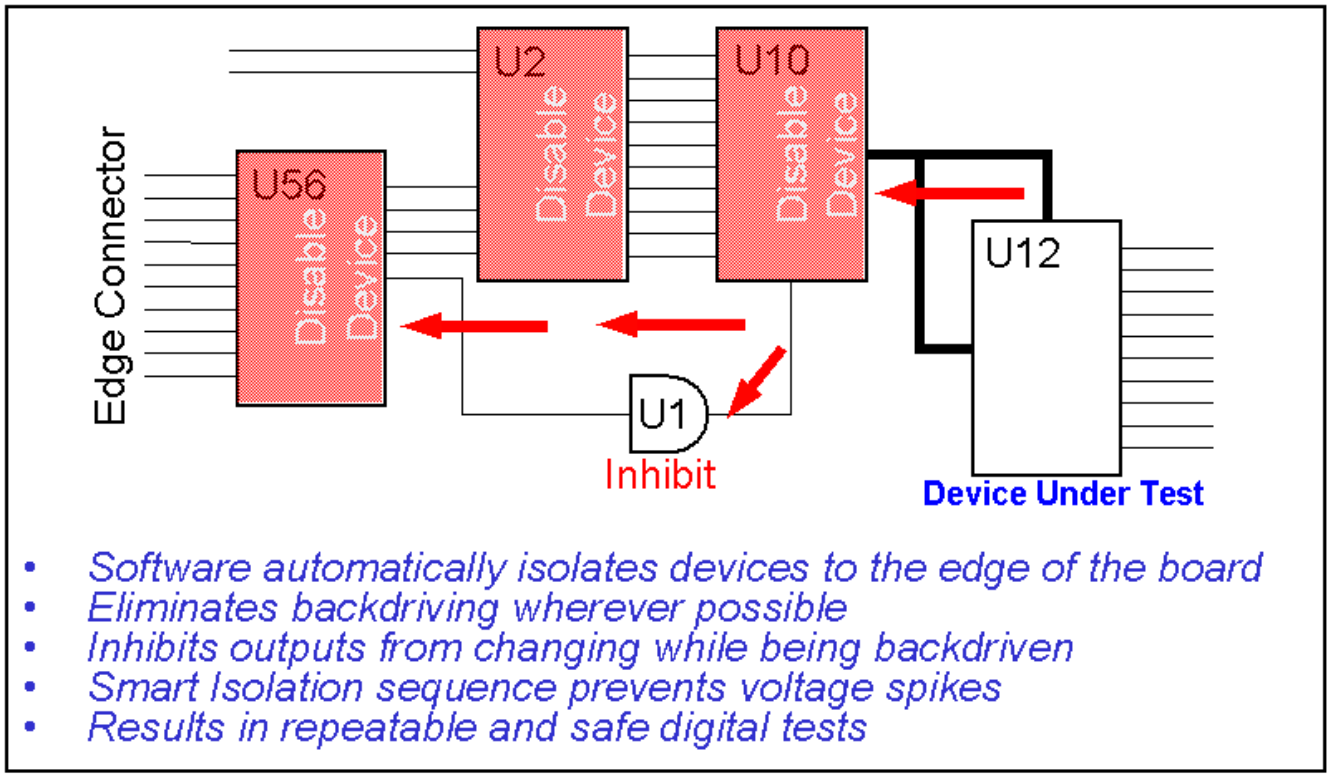


Figure 10: Multi-Level Digital Isolation

Conclusions

Performing powered-up in-circuit vector testing of today's lower voltage technologies is challenging and cannot be performed by most traditional in-circuit test equipment. To accurately, safely, and reliably test low voltage technologies requires an in-circuit tester with independently programmable, high accuracy driver/sensors, real time backdrive current measurement and control capabilities, specialized digital controller, and multiple level digital isolation capabilities.

Acknowledgements:

The author wishes to acknowledge Jim Ficaro, Doug MacAloney, and Tony Suto of Teradyne for their contributions to this paper and for their guidance on this topic.

References:

[1] Intel 2002 White Paper – PC Energy Efficiency Trends and Technologies

[2] Texas Instruments 1999 Application Report – Benefits and Issues on Migration of 5V and 3.3V Logic to Lower Voltage Supplies

[3] Albee, Backdrive Current-Sensing Techniques Provide ICT Benefits, Evaluation Engineering, February 2002

[4] Diep and Durvary, Electrostatic Discharge(ESD), 2001 Texas Instruments Application Report

[5] UK Ministry of Defense (MOD), "Safe Operating Limits for Backdriving", Int Def Stan 00-53/1, November 15, 1991