

Embedded thermoelectric cooling

Thin film thermoelectric devices offer a fundamentally new operating regime for integrated, active cooling solutions and localized thermal management, yet the assembly methodology used to implement these devices is fully compatible with existing surface mount approaches.

In order to take advantage of these unique characteristics, thin film thermoelectric devices need to be designed for the appropriate thermal and form-factor environments, with system-level constraints carefully considered as an integral part of the overall design process.

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**Keywords: Thin Films,
Thermoelectric Cooling**

Thermoelectric devices

The core component of a thermoelectric module is a thermocouple. A thermocouple consists of an n-type and a p-type semiconductor connected together by a metal plate. Electrical connections at the opposing ends of the p- and n-type material complete an electric circuit.

Thermoelectric cooling (TEC) occurs when current is supplied, in which case the thermocouple cools on one side and heats on the other by what is known as the Peltier effect.

Thermoelectric generation (TEG) occurs when the couple is subjected to a thermal gradient (i.e., the top is hotter than the bottom), in which case the device generates current, converting heat into electrical power by what is known as the Seebeck effect.

Thermoelectric modules

A thermoelectric module (Figure 1) is made up of a number of thermocouples connected electrically in series; that is, the electrical current flows from one thermocouple to the next, until it has traversed all of the thermocouples in the module. From a thermal perspective, the thermocouples are in parallel as the heat flows through all of the devices at once – from the top plate to the bottom plate in the module.

A temperature difference, ΔT , is generated between the top and bottom plates, depending on both the magnitude of the current flowing through the thermocouples and the amount of heat being pumped across the device.

The most basic representation of thermoelectric cooling performance is a load line (Figure 1). A load line represents the ΔT and Q_{pumped} conditions possible for a given TEC drive current. At the maximum drive current for the module, the load line is generated from two key parameters: 1) the maximum power the device can pump, Q_{max} ; and, 2) the maximum temperature difference that the device can sustain between its top and bottom plates, ΔT_{max} .

ΔT_{max} is obtained when there is no external heat load (zero Q condition) and can be theoretically obtained from Equation 1.

$$\text{Equation 1. } Q_{\text{max}} = \frac{\alpha^2 T_c^2}{2R} = \frac{A\alpha^2 T_c^2}{2\rho L}$$

where α is the Seebeck coefficient; κ is the

thermal conductivity; ρ is the electrical resistivity; T_c is the cold junction temperature; K is the thermal conductance; and R is the resistance.

On the other hand, Q_{max} is obtained when there is no temperature difference between the top and bottom plate (Equation 2) where A is the area of the device and L is the length (thickness) of the thermoelectric material.

Equation 2.

$$\Delta T_{\text{max}} = \frac{\alpha^2 T_c^2}{2KR} = \frac{\alpha^2 T_c^2}{2k\rho}$$

The two parameters are graphed on a chart (ΔT_{max} at $Q = 0$; Q_{max} at $\Delta T = 0$) to provide a load line (Figure 1) and the resulting load line connecting these two points is the best way to compare TEC performance.

Conventional vs. thin film thermoelectric modules

In practical applications a large number of P- and N-type pellets are cut from hot-pressed thermoelectric material and thermocouples are assembled together (electrically in series, thermally in parallel) to form a TEC or a TEG. Conventional modules are referred to as 'bulk' modules because of their size and fabrication approach.

More recently, a significant amount of development has been focused on thin-film thermoelectric devices. Thin-film thermoelectric materials can be grown by conventional semiconductor deposition methods, and devices can be fabricated using conventional semiconductor micro-fabrication techniques. The resulting devices are much smaller than conventional offerings and show promise for direct integration into modern manufacturing methods.

For reference, a thin-film TEC is shown relative to a conventional bulk TEC in Figure 1. In this example, the thin-film TEC is ~6x smaller in its x-y dimensions and ~18x smaller in the z dimension. Thus, on a volume basis the thin-film TEC is ~110x smaller in size.

The thin film advantage: Q_{max}

Whereas ΔT_{max} is not theoretically expected to change as material thickness changes (although it does somewhat because of losses incurred by making the device thinner), Q_{max} is inversely proportional to the thickness (L), and therefore increases substantially as the material is made

thinner.

Thin film devices typically have material thicknesses of 10-20 μm . This small value for L allows exceptionally high heat fluxes and low thermal resistances. As a result, thin film TECs can support much higher power densities than conventional thermoelectric modules. This is clearly evident in Figure 1, where the thin film power pumping density is more than 30x larger than that of the conventional TEC. Although ΔT in thin film devices is still somewhat lower than bulk TECs, no TEC can operate to the right of its maximum current load line. Consequently, thin film TECs are uniquely capable of addressing applications that have high power densities.

Thin-film thermoelectric device fabrication and implementation

A thin film thermocouple is fabricated by attaching n-type and p-type material to a metal sub-mount. The thin film thermocouple can then be attached, by way of solder bumping, to any substrate that has an isolated metal trace (Figure 2). The thermocouples themselves can be engineered to add as little as 100 μm to the height of the package.

This surface mount fabrication method enables a new approach to thermal management where these small, solid-state cooling devices can be embedded directly into a package to achieve a custom cooling solution. Figure 3a shows a thermocouple bump bonded to an isolated metal trace on Silicon. Figure 3b shows 16 thermocouples, this time each with a mini header, implemented in a standard TEC design for low profile, low power cooling. Figure 3c shows 84 thin film thermocouples, embedded in 100 μm of copper, to form a very low profile cooler with a very high power pumping capability.

Applications for Embedded Cooling

One of the drawbacks of thermoelectric devices is that in order to cool they consume power. This power adds to whatever power is being pumped out of the cooling zone, so at the larger, system level more heat has to be dissipated with a TEC in operation than without one.

An important consideration is the efficiency or coefficient of performance (COP) of a TEC which is defined as Equation 3.

Equation 3.

$$COP = \frac{Q_{\text{pumped}}}{P_{\text{in}}}$$

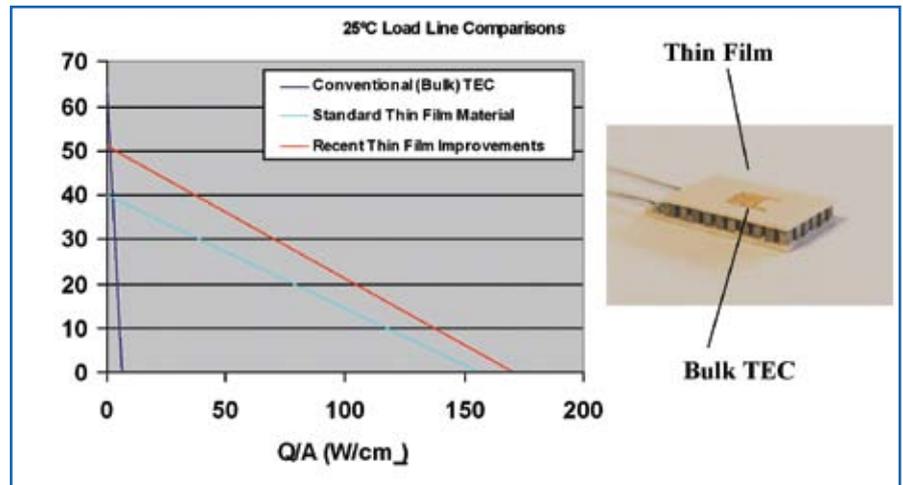


Figure 1. The load line for Nextreme's thin film device are compared to a conventional TEC built with bulk thermoelectric pallets. The thin film TEC is shown on top of the bulk TEC for comparison.

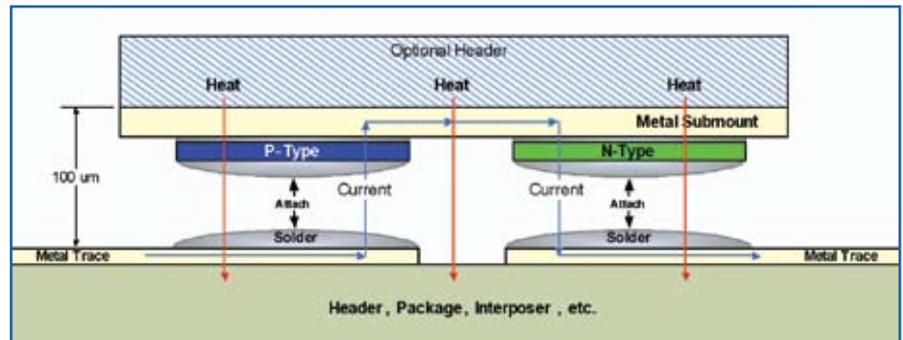


Figure 2. This fabrication approach for the thin film thermocouple forms the basic building block for all thin film thermoelectric modules.

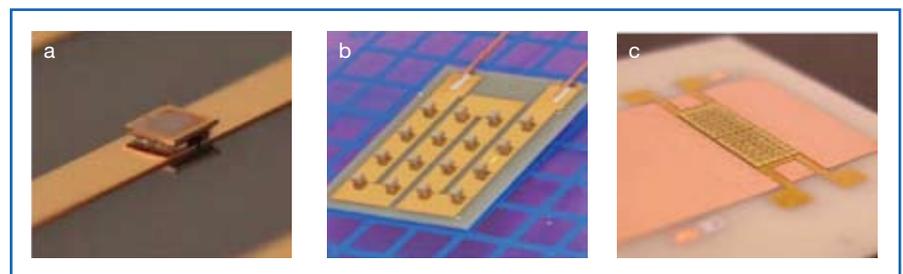


Figure 3. a) a single element thin film thermoelectric device is as small as 300 μm x 300 μm x 100 μm high; b) these devices can be distributed to cool a larger surface area; c) for very high power pumping density, high packing fractions are used. The module in c) is 7.0 mm x 3.0 mm x 0.1 mm in size and contains 84 elements.

A TEC will pump a certain amount of heat, Q, and add an additional amount of heat, P_{in} ($=Q/\text{COP}$). As a result, bulk TECs are often sold as systems that include the TEC and a heat transfer device such as a fan, heat sink, heat pipe, etc. The value of the TEC in this case is that it can deliver sub-ambient temperatures and provide active temperature control at the cost of increasing the system level heat transfer problem.

The value of the thin film TEC,

however, is that it can unobtrusively be integrated into a device or a device package to locally enhance or enable operation. Adding an additional heat transfer system defeats the purpose of the integration. As such, careful attention has to be paid to the characteristics of the heat transfer problem, the design of the thin film TEC solution and the design of the device package. When these three issues are addressed in tandem, ideally at the time of product development,

significant performance improvements can be achieved. Two example applications are discussed below.

Hot spot cooling

The challenge of removing heat from integrated circuits (IC) has increased in significance during the rapid evolution of IC design, where ever faster, higher density circuits are generating more heat. The electronics industry has responded to this challenge with innovative improvements in the basic thermal management components, including heat sinks, fans, heat pipes, heat spreaders, thermal interface materials, cold plates, etc., all primarily aimed at uniformly cooling the IC. However, with the emergence of nanoelectronics (90 nm feature size process technology going to 32 nm by the end of the decade), localized areas of high heat flux are becoming more pronounced. These localized high heat flux areas create hot spots that are significantly above the average die temperature, putting a constraint on the IC's performance, reliability and yield.

It is feasible to address hot spots in the IC package by integrating a thin film TEC into the package (Figure 4). The embedded thin film thermoelectric cooler (eTEC™) is integrated into the copper heat spreader lid to cool the area directly over the hot spot. Figure 4 shows the eTEC embedded on a heat spreader, which forms the lid of a packaged IC. The hot side of the eTEC is soldered bumped to a passivated surface on the heat spreader and a thermal interface material is used to interface the eTEC to the back of the IC die.

In a demonstration of this concept, a 3.5 mm x 3.5 mm eTEC was used to cool a 2 W hot spot on a thermal test vehicle. The chip background power was 60 W, for a total power (hot spot + background) of 62 W. The hot spot generated 1250 W/cm² on the front side of the die and the eTEC was placed directly over the hot spot on the back side of the die (Figure 4). With this approach, more than 10°C of cooling was achieved at the hot spot (Figure 5).

It should be noted that this is an ideal application for an embedded thermoelectric device. The eTEC pumps a total of 3-4 W as it cools the hot spot as well as a small portion of the background. Because of its very high power pumping capacity (Figure 1), the eTEC can operate under these conditions at a COP of 1-2 and therefore adds only ~3W (<5%) to the overall power coming off the chip. Whereas the thermal test vehicle initially generated 62 W of power, the chip and the operating eTEC now generate ~65 W. Thus, 10°C

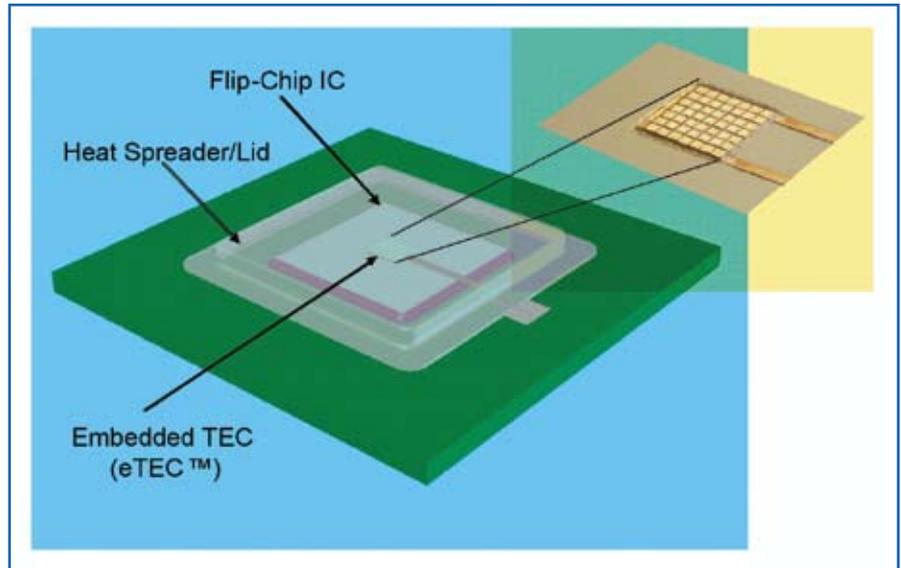


Figure 4. A thin film TEC is embedded into the heat spreader lid (inset) to cool a 2 W hot spot generating 1250 W/cm² at the silicon surface.

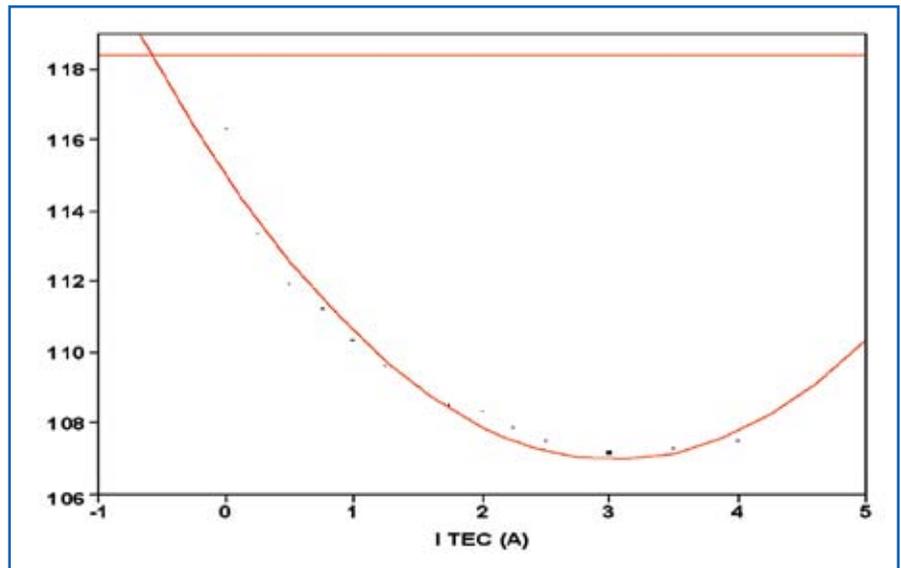


Figure 5. The eTEC™ reduces temperature by 10°C at a 2W hot spot generating 1250 W/cm².

of localized cooling is achieved without a significant impact at the system level (i.e., no improvement is needed at the system level – fans, heat sink, etc.).

In a less challenging application the extra power added by the eTEC to the system can necessitate improved system level cooling, washing out the eTEC cooling advantage. For example, using an eTEC to cool a 5 W hot spot on a 20 W background would require ~8 W (hot spot + some background heat) pumped by the eTEC. At a COP of 1, this would add an extra 8 W to the 25 W already being generated by the chip (a 32% increase!) resulting in 33 W of total power that now needs to be managed.

Consequently, the value proposition manifests itself most clearly in high performance chips (microprocessors, graphics processors, ASICs and other high-performance CMOS ICs) at high power non-uniformities – something that is likely to become more prevalent as CMOS scales to 32 nm and beyond.

Laser diode cooling

Laser diodes have long been the purview of thermoelectric coolers as precision temperature control is a critical aspect of laser diode performance. A major trend in photonics, however, has been the move to smaller, more integrated and cheaper

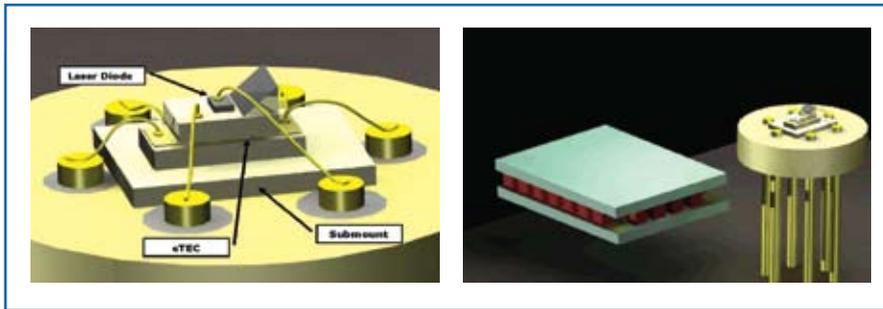


Figure 6. Integration of an eTEC into a TO-56 package with a laser diode. The TO-56 packaging solution is shown relative to a typical bulk thermoelectric cooler. Smaller bulk TECs are available, but become increasingly difficult to implement and, as a result, few TO-56 packages include active cooling.

packaging in order to enable lower cost structures and high volume manufacturing. In the course of this transition, conventional TEC solutions have become increasingly difficult to implement as size and power densities cannot effectively be addressed with bulk thermoelectric technology.

Figure 6 shows a laser diode in a TO-56 packaging solution. In general, bulk thermoelectric technology (also shown for comparison in Figure 6) is too large and does not have the performance required to address this application. For example, a low power laser diode might generate as little as 0.09 W of power; however, the diode itself is only ~300 μm x 200 μm in size. This then equates to a device producing ~150 W/cm²! Even if that power is spread by a factor of 30 (to 5 W/cm²) it still falls outside the operating regime of a typical bulk TEC, especially within the constraints of the package size.

Using the 'standard' thin film load line in Figure 1 it can be demonstrated that an 8 element (8 thermocouple) eTEC, with a total footprint of 2 mm x 1.5 mm x 0.35 mm high, can pump 0.15 W (5 W/cm²) at a ΔT of 25°C and a COP of 0.35. Accounting for losses incurred by heat spreader material between the laser diode and the eTEC, the ΔT achieved at the laser diode will be ~15°C. With improved materials (see the load line for material improvements in Figure 1) the eTEC operating ΔT can be increased to 30-35°C, which translates directly into 5-10°C improvement in ΔT at the laser diode.

More traditional optoelectronic packages, like the TOSA (transmit optical sub assembly), are in fact large enough to accommodate miniature versions of bulk TECs. In these applications ΔT_{max} values of 60-70°C are often desired, which is still outside the performance regime of thin film TECs (Figure 1). However, higher laser powers and shrinking power budgets are driving product engineers towards more

efficient solutions. Because thin film TECs have higher power pumping capability, they also operate at higher efficiencies, relative to bulk devices, at higher powers and moderate ΔT . Consequently there is emerging interest for eTECs even in these larger packaging solutions.

Summary

Thin film thermoelectric devices offer a fundamentally new operating regime for integrated, active cooling solutions. Furthermore, the assembly methodology used to implement these devices is fully compatible with existing surface mount approaches.

As coolers, thin-film thermoelectric devices deliver unprecedented power-pumping density with ΔT performance approaching that of the best available technology. Because they are so small, the devices can be integrated directly into a semiconductor or optoelectronic package to achieve localized cooling and temperature control – something never before available to product engineers in these industries. At the same time the devices are small enough and pump enough power to enable new applications in electronics, photonics, medical devices and instrumentation.

In order to take advantage of these unique characteristics, thin film thermoelectric devices need to be designed for the appropriate thermal and form-factor environments, with system-level constraints carefully considered as an integral part of the overall design process.

Jesko von Windheim, CEO of Nextreme Thermal Solutions, helped spin Nextreme out of RTI International, where he was entrepreneur in residence and VP of commercialization. Jesko holds a bachelor's degree in chemistry and physics, a master's degree and a Ph.D. in physical chemistry, and an MBA from the Kenan-Flagler business school.



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