WAFER-LEVEL PACKAGED MEMS SWITCH WITH TSV

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ABSTRACT
A miniaturized wafer-level packaged MEMS acceleration switch with through silicon vias (TSVs) was fabricated, based on technologies suitable for harsh environment applications. The high aspect ratio TSVs were fabricated through the silicon-on-insulator (SOI) substrate prior to the fabrication of the MEMS structures. Doped polysilicon was used as the conductor for the TSVs, which has the advantage of a thermal coefficient of expansion that matches that of the silicon substrate material. The fragile MEMS structures were protected from the environment by wafer-level bonding of a glass cap using benzocyclobutene (BCB). The BCB layer which was spray-coated onto the patterned glass wafer provides a good bond strength and temperature stability. As opposed to having lateral interconnects at the interface between the cap wafer and the device wafer, the use of TSVs significantly reduces the footprint and allows flip-chip bonding of the devices onto a substrate. The bare MEMS chips were mounted directly onto a printed circuit board (PCB) thereby avoiding an entire packaging level and reducing the system complexity and cost. This was done using an isotropic conductive adhesive (ICA) based on metalized polymer spheres, which is believed to be an interconnect technology more suitable for harsh environments than metal-based BGA and CSP technology. The initial characterization of completed chips mounted on a PCB shows promising results.

Keywords: through silicon via, TSV, MEMS switch, wafer-level packaging, ICA

INTRODUCTION

MEMS Acceleration Switch

An acceleration switch (or inertia sensor) is a device that closes (or opens) a circuit above a certain acceleration threshold. The numerous designs presented in literature may be roughly classified as either intermittent [1,2] or persistent [3,4] type switches. The persistent type acceleration switches employ a mechanism (e.g. mechanical latch, electrostatic actuation etc.) to remain in the changed state when the acceleration is reduced below its original threshold.

The fundamental characteristics of acceleration switches means that they may be used to monitor acceleration levels while not consuming power. They are as a result attractive in health monitoring systems for long lifetime systems. Another potential application of acceleration switches is in safety and arming devices (SADs) in smart ammunition fuzes. The tasks of a SAD are to insure the ammunition is safe during storage, handling (including accidental mishandling) and launch, and to reliably arm the ammunition. Arming may only occur after two separate and independent environmental stimuli have been detected [5,6].

Ammunition fuzes are subjected to a number of demanding environmental conditions. The ammunition used as a testbed in this work is subjected to a setback acceleration pulse with an amplitude exceeding 60 000 g (1 g = 9.81 m/s^2) and a centripetal acceleration that increases radially to 9000 g/mm. Severe shocks and vibrations may also be generated from the metal to metal contact between the projectile and the barrel, as well as when the projectile exits the barrel. In many cases, the fuze must also operate after the projectile has penetrated a hard target. The fuze and its electronics must also be capable of remaining safe and operational in severe

climatic conditions where temperatures may range from -54 to 71 °C [7].

Given the limited volume in an ammunition fuze the potential reduced size of a MEMS based SAD is an important motivation for this work. However, new functionality offered by low cost and rugged MEMS devices in the fuze are also important.

The acceleration switch presented here is designed to detect when the centripetal acceleration exceeds a threshold of 13800 g. The acceleration causes a freestanding MEMS structure to move in the lateral plane and make contact with a neighbouring structure, thereby closing a circuit. Two intermittent switches are integrated on the same MEMS chip together with two persistent (mechanical latching) acceleration switches designed to detect the setback acceleration during launch. The persistent switches will however not be discussed here.

Through Silicon Vias

Vertical through silicon vias are extremely useful for encapsulated silicon MEMS devices, as they allow to connect the electrical structures that are enclosed in a MEMS cavity to the outside [8,9]. While it is possible to have lateral interconnects at the interface between the cap wafer and the device wafer combined with wire bonding pads along the periphery of the MEMS device, this solution results in a large footprint. Vertical TSVs allow the use of flip-chip bonding techniques instead of wire bonding, which contributes to a significant miniaturization.

When fabricating TSVs through the cap wafer, an electrical interconnect has to be realized between the cap wafer and the electrical structures on the device wafer [8], which can result in an increased process complexity and cost. Therefore it will often be preferable to fabricate the TSVs in the MEMS device wafer instead, as was done in the present work. Another advantage of having the TSVs in the device wafer is that even after flip-chip mounting of the MEMS chips it is possible to visually inspect or optically interface the devices, if a glass cap is used.

Since the processes needed to fabricate the TSVs cannot be applied after the fragile MEMS structures have been etched and released, the vias must be fabricated first. This approach has the advantage of allowing the use of high temperature thermal oxidation and polysilicon deposition for filling the vias. Those are extremely conformal processes which can be applied to vias with very high aspect ratio. Although etching small (or narrow) TSVs through the complete wafer thickness can be challenging, it makes the subsequent filling of the vias easier and results in a smaller footprint. Gas phase doping of the polysilicon allows to reduce the via resistance to a level that is sufficiently low for most DC applications [10]. As opposed to metal filled TSVs, polysilicon filled vias also have the additional advantage of a thermal coefficient of expansion that matches that of the silicon substrate material.

Wafer-level Packaging

Wafer-level packaging is used increasingly as a promising technology to reduce the total MEMS packaging costs. It is especially attractive when a wafer is populated with a large amount of small devices, as it allows for all devices to be packaged simultaneously in a single step. Another inherent advantage of wafer-level packaging is that the encapsulation at wafer level protects fragile MEMS devices during the wafer dicing process.

A wide variety of wafer bonding techniques have been used for wafer-level encapsulation, including direct bonding [11], anodic bonding [12], solder bonding [13], eutectic bonding [14], thermocompression bonding [15], low-temperature melting glass bonding [16] and adhesive wafer bonding [17]. Adhesive wafer bonding is an extremely robust, very low-cost and CMOS compatible process. It does not provide hermetic sealing of the cavities in terms of gas-tightness [17] but it does protect the packaged devices from liquids, particles and dust. A number of approaches for wafer-level sealing of cavities with adhesive wafer bonding have been proposed. Glass-lid encapsulation in combination with chip-to-wafer placement and bonding has been demonstrated with b-stage epoxy [18] and with photosensitive benzocyclobutene (BCB) [19]. However, the disadvantage of those capping techniques is that each lid is individually positioned and glued and thus the full potential of simultaneously packaging all devices is not utilized.

When adhesive wafer bonding is used for wafer-level encapsulation, the adhesive is typically patterned such that it is only left locally on the wafer areas to be bonded. This can be done by using photosensitive polymer adhesives or by pattering the adhesive using masking and etching processes [20]. Patterning of a thermosetting polymer adhesive, like photosensitive BCB, typically requires partially curing (cross-linking) the polymer during the patterning process. The partially cross-linked polymers reflow less during bonding, which results in a reduced bond strength and reduced bond yield if topographies are present at the wafer surface [20]. As a result the process window for bonding with photosensitive polymer adhesives is relatively narrow. Other methods to place the polymer adhesive only on the wafer areas to be bonded are local dispensing, screen-printing, stamping, contact-printing of a liquid polymer precursor and chemical vapour deposition of conformal coatings on a structured wafer surface [17]. However, most of these methods have limitations with respect to the thickness control of the adhesive polymer layer and the dimensional control of the

pattern in the polymer adhesive and/or are difficult to implement in a semiconductor processing environment.

In this paper we present an extremely simple and robust process scheme for wafer-level sealing of the MEMS acceleration switches using adhesive wafer bonding with a thin spray-coated BCB layer as bonding material [21]. In this process, no patterning of the BCB polymer adhesive is needed.

Direct Mounting on PCB

In order to fully exploit the advantages offered by the TSVs, one of the numerous flip-chip or bumping interconnect technologies must be used [22].

In this work the MEMS chips were mounted using a novel isotropic conductive adhesive (ICA) containing metal-coated polymer spheres [23]. To reduce the overall size and complexity of the packaged system, the MEMS chips were mounted directly on a printed circuit board (PCB).

EXPERIMENTAL PROCEDURE

Fabrication of TSVs

A schematic overview of the complete process sequence used to fabricate the MEMS switches with TSVs is shown in Fig. 1.

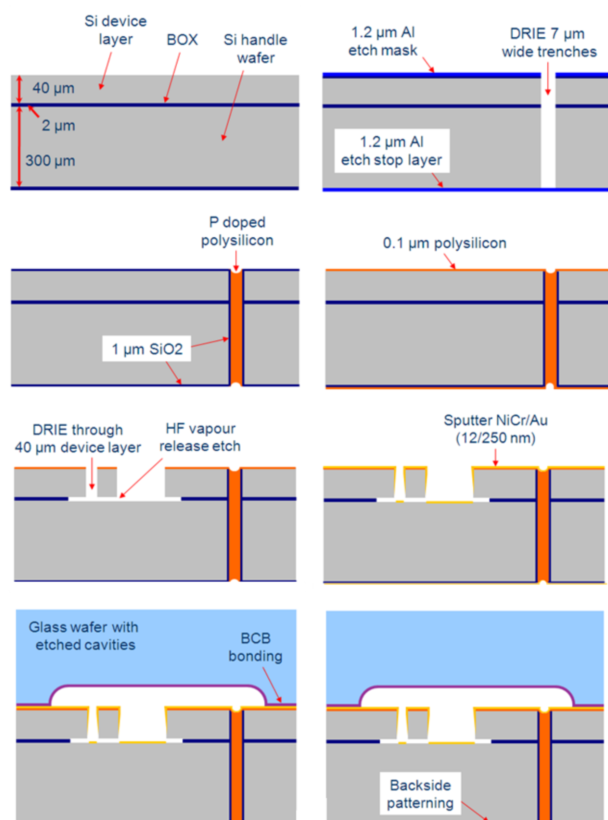

Figure 1. Process sequence for the wafer-level packaged MEMS acceleration switch with TSV.

The TSVs were fabricated prior to the MEMS structures themselves. SOI wafers with a 100 mm diameter were used as the substrate material, with a 40 µm thick silicon device layer, separated from a 300 µm thick silicon handle wafer by a 2 µm buried oxide (BOX) layer. A 1.2 µm aluminium layer was sputtered on both sides of the wafers. The aluminium on the device layer side was patterned in order to serve as a hard mask for the via etch, while the aluminium on the backside of the wafers served as an etch stop layer. The rectangular via holes were 7 x 70 µm in size, meaning that the TSVs had an aspect ratio close to 50:1 (in one direction). Keeping the width of the via holes relatively narrow (7 µm) made the subsequent filling of the vias faster. At the same time the 70 µm length of the via holes made the through wafer etch considerably easier than what it would have been for e.g. 7 x 7 µm via holes. The TSVs were etched consecutively through the device layer, BOX layer and the silicon substrate, all using the same aluminium hard mask. All etches were done on an Alcatel AMS200 SE I-Productivity etch tool. The silicon device layer etch as well as the etching through the silicon handle wafer were done using an optimized Bosch deep reactive ion etching (DRIE) process [24]. The extremely high aspect ratio of the TSVs was only possible by changing the etching conditions at different points during the etch [25]. After etching the silicon device layer, the 2 µm thick BOX layer had to be etched, before the silicon etch could continue through the handle wafer.

After etching the via holes through the SOI wafers, the aluminium was stripped from the wafers by wet etching. A 1 µm thermal oxide was then grown to isolate the TSVs from the bulk silicon material. The vias were filled using four consecutive chemical vapour depositions of 1 µm undoped polysilicon. In between each deposition step the polysilicon was heavily doped with phosphorus using $POCl_3$ gas phase doping. After the vias were filled, the excess polysilicon that had been deposited on the wafer surface was removed by reactive ion etching (RIE) from both sides of the wafer. At this point, the main part of the TSV process was completed and some pilot wafers were sputtered on both sides with a 1 µm aluminium layer that was subsequently patterned. This allowed to verify the success of the TSV fabrication, before continuing the processing on the actual process wafers.

Fabrication of MEMS Switches

Once it was established that the TSV processing had been successful, the processing of the actual MEMS structures was started. First, the thermal oxide was stripped from the device layer side by wet etching, and a 100 nm polysilicon layer was deposited by chemical vapour deposition. This was done in order to protect the oxidized sidewalls of the TSVs from being etched during the subsequent release etch of the MEMS structures. As the release etch was done using a single sided process, the polysilicon could at this point be removed from the backside of the wafers by RIE. Next, a 2.6 µm thick HiPR6517 photoresist was spin-

coated and patterned on the device layer side in order to define the MEMS structures. The TSVs were protected from the subsequent device layer etch by the resist. The device layer was etched using the same process as the one that had been used to etch the device layer for the vias, with the buried oxide acting as an etch stop layer. After stripping the photoresist and polymer residues from the DRIE etch by O_2 plasma stripping, the sacrificial buried oxide below the movable silicon structures was etched away using a 1 hr HF vapour release etch done at 35 °C. This was done on a single wafer etching tool with a fixture that prevents the backside of the wafer from being etched. The thin undoped polysilicon layer that protected the sidewalls of the vias during the release etch was then removed by doing a short RIE etch, as it would otherwise have contributed to an increased contact resistance between the subsequent metallization and the doped polysilicon from the TSVs.

The wafers were metalized by sputring 150 nm NiCr / 250 nm Au on the backside, and 12 nm NiCr / 500 nm Au on the device layer side. The metal on the device layer side did not need any patterning. The reason for that is that at the same time as the MEMS structures were being defined by the device DRIE step, trenches were etched in order to electrically isolate different parts of the device layer from each other. After the release etch, a 2 µm space exists at the foot of the silicon structures in the device layer, which prevents the sputtered metal from connecting the device layer to the handle wafer. Therefore no patterning of the metal was needed on the device layer side. The metal on the backside of the wafers was patterned after the encapsulation of the MEMS structures.

Wafer-level Encapsulation

The processing of the glass cap wafers started with the sputtering of 20 nm TiW / 1 µm Au on both sides of the wafers followed by the patterning and wet etching of TiW/Au in KI/I_2 and H_2O_2 to provide an etch mask for the cavity etching. The etching of the cavities was carried out using 49 % HF at room temperature. The etching time to reach a cavity depth of 20 µm was 3 min. The TiW/Au layer was completely removed after the glass etch. The wafers were then spray-coated using Cyclotene 3022-35 (BCB) with an airbrush pressurized with dry N_2. The resulting BCB thickness was 1.4 µm. The wafers were then baked on a hotplate at 110 °C for 90 sec to remove solvents.

The glass cap wafers were then aligned to the MEMS wafer using a Suss BA6 bond aligner. Spacers were not used in the bonding process. The bonding was performed in a Suss SB6 thermo-compression bonder. First, the bonding chamber was evacuated. The wafers were pre-heated to 150 °C for 5 min for dehydration. The wafers were then brought together with a pressure of 300 mbar, and heated to a temperature of 250 °C, which was maintained for 1 hr. The bonded substrates were then allowed to cool down prior to the removal from the bonder.

After bonding, the bond pads on the backside of the device wafer were defined by patterning the NiCr/Au layer using a 6 µm thick AZ4562 photoresist and wet etching. Finally, the wafers with the completed MEMS acceleration switches were diced using conventional blade dicing.

Direct Mounting on PCB

For testing and characterization, the completed MEMS chips were mounted directly on a FR-4 PCB using an ICA containing highly uniformly sized metal-coated polymer spheres. The process consisted of fist depositing the ICA on the bond pads of the PCB using a Dima HS-100 stencil printer with a metal stencil fabricated by HP Etch. The MEMS chips were then accurately placed using a MyData My-9 pick and place machine. Finally, the ICA was cured at 150 °C for 60 sec.

EXPERIMENTAL RESULTS

Fabrication of TSVs

After etching the 7 µm narrow trenches through the 40 µm thick device layer, a slight (less than 0.7 µm) lateral etching of the silicon was observed at the bottom of the trenches. This was caused by notching, which is a well-known phenomenon that occurs when etching high aspect ratio structures and stopping on a buried oxide layer [26]. When exposed to the etching plasma, the BOX layer gets charged by the positive ion flux that is directed towards the substrate, which causes the ion trajectories to be distorted in the vicinity of the BOX layer.

Etching through the 2 µm thick BOX layer at the bottom of the trenches proved to be challenging. Using a conventional oxide dry etching recipe with radio frequency (RF) substrate bias was not successful for etching oxide at the bottom of the trenches that had an aspect ratio of more than 5:1. Increasing the RF substrate bias, tuning the process pressure and gas flows, or increasing the etching time did not improve the result. Virtually none of the 2 µm thick buried oxide was being etched and in the centre of the trenches a build up of polymer residues could even be observed on top of the oxide (Fig. 2). At the same time severe notching occurred, which resulted in more than 3.6 µm sideways etching of the silicon. As the limitations of a RF substrate biasing scheme became obvious, a new etching recipe based on pulsed low frequency (LF) biasing was developed. Although a long etch time was required, the new recipe made it possible to etch through the 2 µm BOX layer. Fig. 3 shows the etch result after applying the LF etch for 35 min. The oxide is etched through and the silicon underneath has also started to etch, indicating that the etch time could be reduced somewhat.

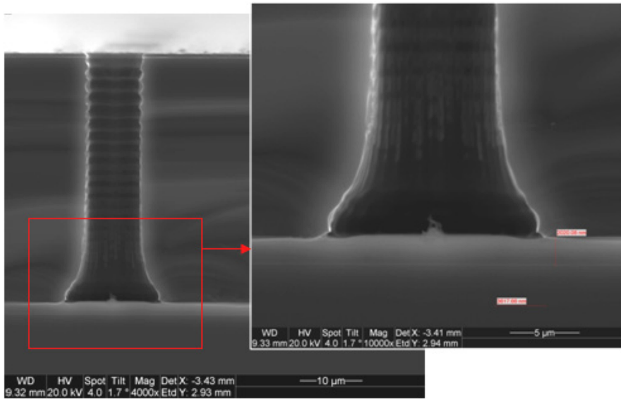

Figure 2. Etch result after etching the 2 µm thick buried oxide with a RIE recipe based on a RF substrate bias.

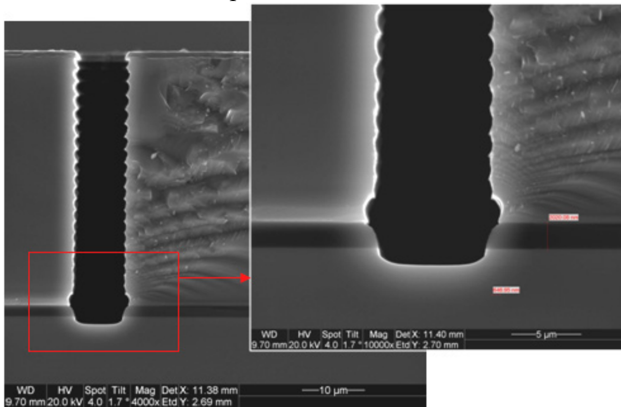

Figure 3. Etch result after etching the 2 µm thick buried oxide with a RIE recipe based on pulsed LF substrate bias.

The multi-step Bosch DRIE etching recipe that was used to etch through the 300 µm thick handle wafer resulted in a very straight etching profile. Using aluminium as an etch stop layer on the backside of the wafers meant that there were no problems with notching at the bottom of the TSVs.

Fig. 4 shows a cross-section of an array with six TSVs after the TSV processing had been completed. The vias appear to be completely sealed towards the top, but further down a void can be seen which indicates that the polysilicon deposition did not fill the TSVs completely. At the wafer surface, a slight recess is seen in the polysilicon, which was caused by the removal of the excess polysilicon from the wafer surfaces by RIE.

Fabrication of MEMS Switches

The DRIE process used to etch through the device layer resulted in vertical sidewalls with small scallops resulting from the Bosch process that was used. A Zygo white light interferometer was used to check the planarity of the released structures after the release etch and after NiCr/Au sputtering. Measurements done on a cantilever structure that is part of the switches with mechanical latching showed that the structure bent about 140 nm upwards. After NiCr/Au sputtering, the same structure bent up with about 550 nm, which indicates a small tensile stress in the metal layer. Considering the 40 µm thickness of the device layer, the bending that was observed was considered to be acceptable. Fig. 5 shows a SEM image of the switches after metallization.

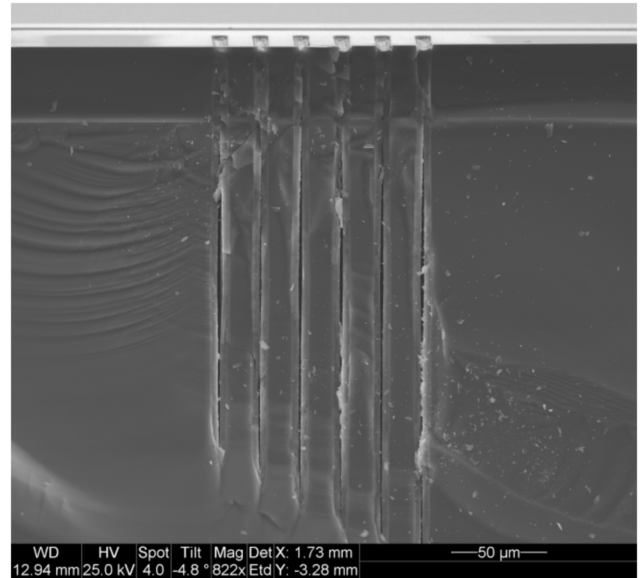

Figure 4. SEM cross-section of an array of six TSVs through the SOI substrate. The vias are completely sealed towards the top, but lower down a void can be seen in the center of the vias.

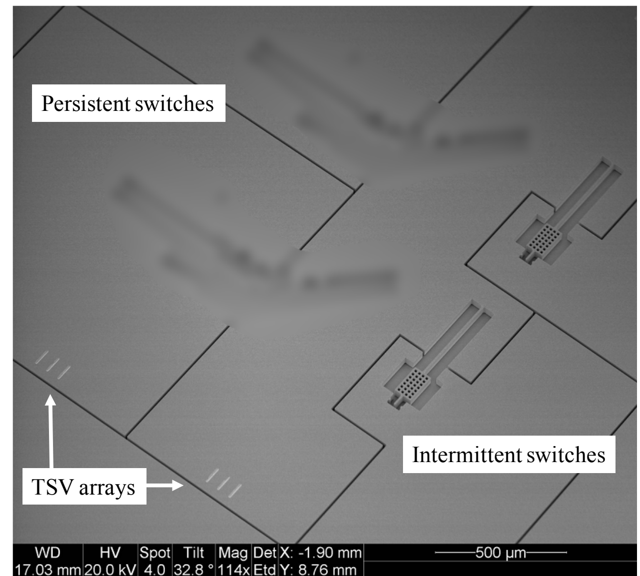

Figure 5. Detail of the MEMS switches after NiCr/Au metallization. The two devices on the left (blurred) are persistent mechanical latching switches. The devices on the right are the intermittent centripetal acceleration switches. Two groups of 3 TSVs can be seen in the bottom left corner of the image.

Wafer-level Encapsulation

All MEMS devices were efficiently sealed by the BCB bonding layer. Particles and defects, in particular on the glass wafers, were fully embedded in the bond seal. To achieve a well aligned bond the spacers on the bond fixture, which hold the wafers apart prior to bonding, were not used in the bonding procedure. Excessive reflow and redistribution of BCB into the cavities was successfully controlled by selecting the right combination of BCB thickness, width of the bond seal, and cavity depth of the glass wafers. Fig. 6 shows two completed chips after bonding and dicing, one seen from the front side and one from the backside.

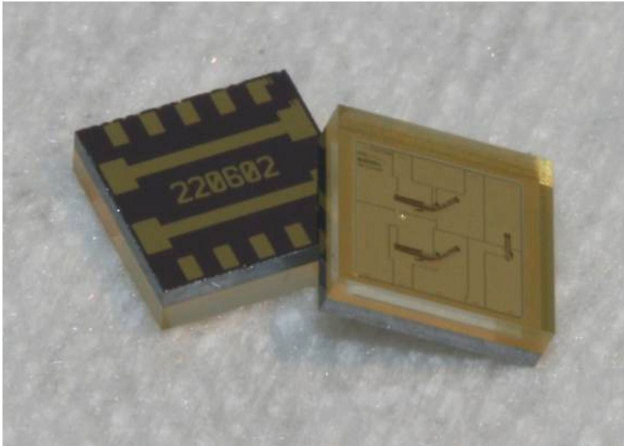

Figure 6. Two completed chips. On the left, the gold bond pads from the backside of the die can be seen. On the right, the MEMS switches can be seen through the glass cap.

Direct Mounting on PCB

Fig. 7 shows a picture of two of the chips with MEMS switches mounted with ICA to a PCB for testing and characterization. This was implemented with the setup used in [23], yielding repeatable results with the 250 x 440 µm pad size and 600 µm pitch.

The rheology of the ICA matrix and the design of the stencil are two factors amongst others that are important to achieve accurate pattern placement and correct amount of adhesive to form the ICA interconnects. Optimising these parameters is part of related work which at the time of writing has just started.

Characterization of the TSVs

Dedicated test structures for the electrical characterization of the TSVs were included on the process wafers. Kelvin structures as well as daisy chains with up to 180 vias were tested on an automatic probe station, before dicing. The average via resistance was 4.5 Ohm, with a yield of more than 95 % (Fig. 8).

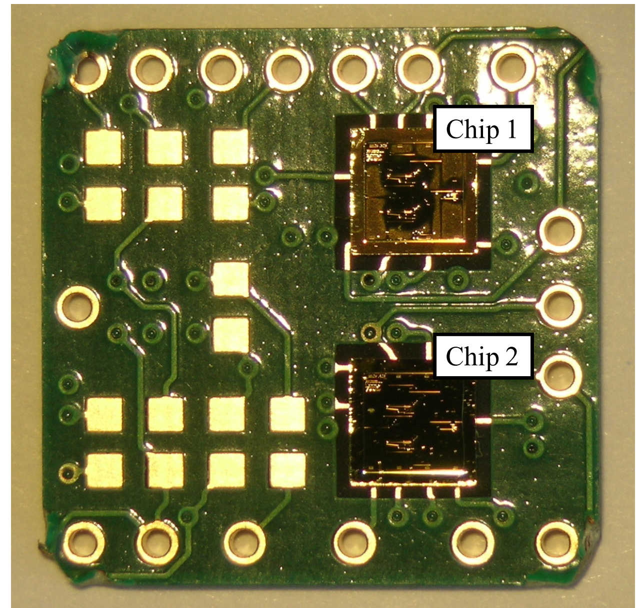

Figure 7. Microscope picture of two MEMS chips mounted with ICA on a PCB for testing and characterization.

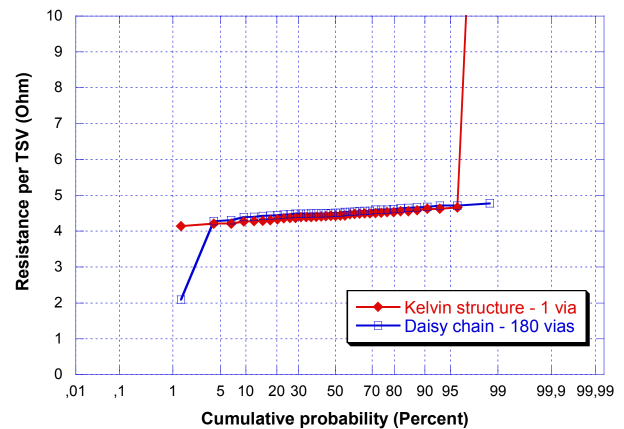

Figure 8. Cumulative probability plot of the TSV resistance measured on a completed process wafer.

Characterization of the MEMS Switches

As an initial test the threshold acceleration of some of the intermittent centripetal acceleration switches was established using a Sorvall WX80 Ultra centrifuge. This allowed us to perform a quasi static high-g test.

To monitor the response of the acceleration switch, when in the centrifuge, the test PCB was integrated with a data logger in a plastic framework which fits in the centrifuge's sample holder. The system is then potted/encapsulated using a powder consisting of 40 to 80 µm glass beads to insure sufficient support for the system. After testing the glass powder can easily be removed e.g. for debugging. A picture of the complete system is shown in Fig. 9.

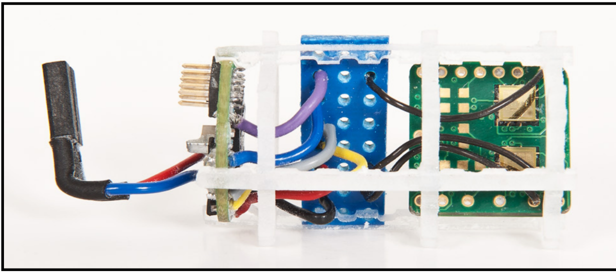

Figure 9. Photograph of the Ø 20 x 35 mm test system. From the right to the left are the test PCB with two MEMS chips, the interface PCB and the datalogger (battery not shown).

A plot of the generated acceleration and the voltage across the switch as a function of time is shown in Fig. 10. At t= 280 sec the acceleration has reached 11800 g and the switch closes and grounds the circuit. The opposite occurs at t= 340 sec when the acceleration has been reduced to 10500 g. Analyzing the second acceleration peak reveals approximately the same acceleration thresholds.

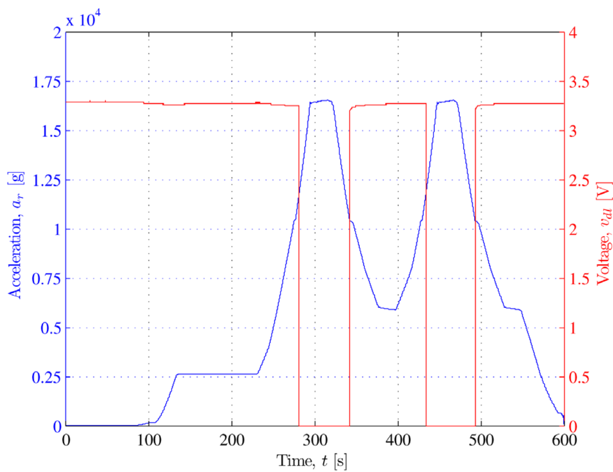

Figure 10. Plot of the generated acceleration and the voltage across the switch as a function of time.

DISCUSSION

Fabrication of TSVs

The newly developed oxide dry etching recipe based on pulsed LF substrate biasing was key to the successful fabrication of the TSVs through the SOI substrates. This process will be very valuable for future MEMS processing, as it makes it possible to do an anisotropic dry etching of buried SiO_2 layers even at the bottom of high aspect ratio structures. With a conventional RF substrate bias, excessive charging of the oxide occurs, which causes the ion trajectories to diverge towards the sidewalls of the structures. This not only results in a significant amount of notching, but it also reduces the ion bombardment onto the oxide and therefore the etch rate. The use of a pulsed LF bias addresses the root cause of the problem by allowing the build-up charge enough time to discharge during the "off" time of the pulse.

The total etch time for etching through the device layer, buried oxide and the handle wafer, was 119 min/wafer. The etch time for etching small structures through SOI wafers strongly depends on the total SOI wafer thickness as well as the individual thicknesses of the device layer and buried oxide. For instance, the total etch time would be reduced to 80 min/wafer for SOI wafers with 40 µm device layer, 0.5 µm BOX and 260 µm handle wafer thickness. Another way to reduce the etch time for the TSVs would be to increase their width, although in that case more polysilicon would have to be deposited in order to fill the vias.

The etch back of the excess polysilicon from the wafer surface results in a recess at the top and bottom of the TSVs. Because of the topography that this creates, this could potentially be a reliability concern. It is essential that the thin metal layer which is sputtered on top of the vias covers this topography properly, in order to insure a reliable contact with the TSVs. In order to avoid potential problems related to the recess of the polysilicon, one could consider to replace the dry etching of the excess polysilicon by chemical mechanical polishing.

Fabrication of MEMS Switches

As a further improvement of the process that is presented here, one could consider to keep the polysilicon layer that was deposited to protect the sidewalls of the TSVs during the release etch. By doping it with the same doping type as the polysilicon and the device layer, one could obtain an even more reliable contact between the TSVs and the device layer. This could however not be done in the present case, because the device layer had a p-type doping while the vias had an n-type doping, which would have resulted in an unwanted pn-junction. Therefore, in this case the 100 nm polysilicon layer was etched away after the release etch.

Etching trenches down to the buried oxide at the same time as the actual MEMS structures were being etched, allowed to electrically isolate different parts of the MEMS device. This resulted in a very simple fabrication scheme for the MEMS structures, with no patterning of the metal on the device layer side. For this approach to work, it is important that the sputtered metal does not bridge the gap that is created between the device layer and the handle wafer by the release etch. The non-conformal nature of the sputtering process, combined with a sufficient device layer thickness and BOX layer thickness are key to the success of this approach.

Wafer-level Encapsulation

The reflow of BCB must be taken into account when designing the glass cap wafers. An approximate design

rule is that almost all of the BCB is squeezed out of the contact area between the glass cap and the silicon MEMS wafer and gathers around the edge of the glass cap (Fig. 11). In order to leave room for the reflow of BCB, there should be a sufficient distance between the edge of the cavities and the MEMS devices.

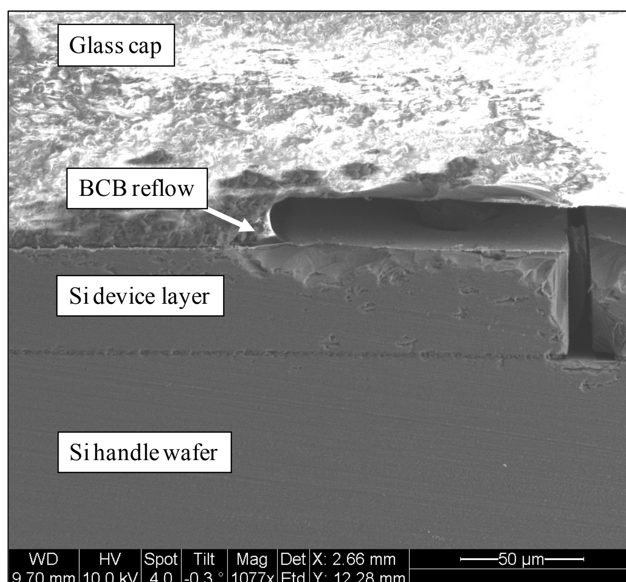

Figure 11. The reflow of BCB yields a thick seal along the foot of the glass cavity, further ensuring the strength of the bonding.

The best result for the wafer-level encapsulation was achieved when the spacers from the bond fixture were not used as part of the bonding process. When spacers are used, there is a risk that the alignment is ruined as the spacers are pulled out during bonding. The wafers were instead simply clamped together by the fixture prior to being loaded into the bonder. The clamps were kept in place throughout the bonding to reduce the chance of misalignment. It is essential that the bonding chamber is free from moisture and oxygen in order for the BCB curing to work. All air must be removed, also from the wafer cavities and in between the wafers to be bonded. It is assumed that the rough BCB surface which is a result of the spray coating helped with the evacuation of the MEMS cavities when the wafers were clamped together without the use of spacers.

A key feature of the encapsulation scheme was the choice of the adhesive. BCB is a thermosetting polymer and has the advantage of not releasing any by-products in the curing process, which could otherwise lead to voids in the bonding layer. Moreover, as the temperature is raised gradually towards the curing temperature of 250 °C the viscosity of BCB remains low in the initial phase of the cross linking process. This allows the adhesive to reflow and to level out the surface roughness of the wafers being bonded. Using this technique, even topography such as metal lines can be planarized and embedded in the bond layer. The reflow allows a strong and void free bond to be formed. The glass transition temperature of BCB eventually reaches a level of more than 350 °C when fully cured, which makes the capped devices compatible with standard flip-chip mounting techniques. Additional advantages of BCB are low moisture uptake (< 0.2 %) and inertness to most chemicals.

The wafer-level encapsulation process is fully compatible with standard semiconductor processing environments and does not involve lithographical pattering or stamping procedures of the polymer adhesive. No photosensitive polymers are required, which are more expensive and more difficult to handle than non-photosensitive polymer adhesives. This low-cost wafer-level cavity sealing method is also suitable for non-hermetic packaging of devices such as CMOS imaging sensors, surface acoustic wafer devices, RF devices and micro fluidic components, including inkjet print heads.

Direct Mounting on PCB

The ICA interconnects have shown no changes in their characteristics after the high-g testing in the centrifuge, which confirms the results from previous work [23]. Further investigation of the novel ICA interconnect method is ongoing.

Characterization of the TSVs

The resistance of the polysilicon vias is directly dependent on the wafer thickness and the via size. While the resistance might be too high for RF applications, for most DC applications the obtained resistance value is acceptable. The high yield of the daisy chains with 180 vias indicate a good manufacturability for the TSV process. Because of the folded layout of the daisy chain structure, the results also show that there are no significant amount of shorts observed for this structure.

Characterization of the MEMS Switches

The closing threshold acceleration of the intermittent switches was established to be around 11800 g, which is 15 % lower than the designed threshold. This could for instance be the result of a slight negative profile for the cantilever beams. As the stiffness of the beam is proportional to the third power of its width (in the bending plane), an underetch of only 0.2 µm is sufficient to cause this effect.

The discrepancy of 1300 g between the closing and opening threshold acceleration can probably be attributed to stiction.

CONCLUSIONS

Miniaturized wafer-level packaged MEMS acceleration switches with TSVs were successfully fabricated and tested, using a simple and robust process scheme. A via

first process based on doped polysilicon vias in the device wafer was used. A new dielectric etch process based on pulsed LF substrate bias was successfully applied for etching through the buried oxide at the bottom of high aspect ratio trenches. The wafer-level encapsulation was done by bonding a glass cap wafer to the silicon device wafer using a non-photosensitive BCB adhesive. The chips with acceleration switches were mounted directly onto a PCB using an isotropic conductive adhesive. The successful fabrication and mounting of the devices was confirmed by the initial characterization of the switches.

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