Improved QFN Reliability by Flank Tin Plating Process after Singulation

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ABSTRACT
The process of singulating IC packages such as Quad Flat Pack No-Lead (QFNs) by either a sawing or punching operation results in exposed copper on the sidewalls. This exposed copper surface can oxidize leading to poor or no solder wetting up the sidewall during the assembly operation. The consequence of this oxidized copper surface is either incomplete or no solder fillet formation during the PCB mounting operation resulting in solder joint reliability concerns. Currently, JEDEC and IPC assembly standards do not specify a toe fillet for assembly. However, several component manufacturers have requested a toe fillet solderability process which would improve current QFN reliability by ensuring toe fillet solder coverage.

A process whereby tin is plated on the copper sidewall of the QFN after singulation has been developed to improve toe fillet solderability. Several assembly studies have been conducted which demonstrate improved QFN reliability due to the use of this toe fillet solderability process. The plating process, toe fillet inspection and improved QFN reliability after assembly due to the use of this toe fillet solderability is described.

INTRODUCTION
As printed circuit designs move to higher density, the industry thought the use of Ball Grid Arrays (BGAs) would replace QFN components especially by this time in IC history. Many have realized that some of the difficulties associated with BGAs could be avoided with QFNs yet still achieve the desired electrical performance. BGAs introduce higher cost with some manufacturing and assembly challenges which are beyond the scope of this paper. Instead, we will focus solely on the QFN devices and how their current reliability can be improved.

Quad-flat no-leads (QFNs) packages are one of the fastest growing package excluding flip-chip chip scale [1]. The advantages and disadvantages offered by QFNs are well understood. Benefits include reduced lead inductance, small footprint, thin and light-weight with good thermal and electrical properties [2]. Now, with a high volume of QFN usage, there is greater attention being paid to design, reliability and performance of these components. Many are working toward stronger industry wide specifications to ensure the performance and reliability of this component style.

QFNs are in the family of bottom termination components (BTC). Specifically, the Joint Electronic Device Engineering Council (JEDEC) describes Small Outline No-lead (SON) as a “no-lead rectangular semiconductor package with metalized terminals on two sides of the bottom surface of the package.” QFNs are defined as “no-lead semiconductor packages with metalized terminals on four sides of the bottom surface of the package [3].” The leads of these components are used to make direct contact with the printed circuit board. Often a QFN will have a die attach paddle (DAP) feature which is used to enable direct thermal interface to the mating circuit board.

A copper foil lead frame is pattern etched or punched for the package assembly process. During the assembly of the package, a die is attached to the lead frame. The dies are then wire bonded. After wire bonding, parts are overmolded and ultimately singulated. The tool designed for singulation can be either punched or sawn. It is during the simulation process that copper edges are exposed leaving the component terminations susceptible to oxidation which can degrade solderability during component assembly to the mating circuit board.

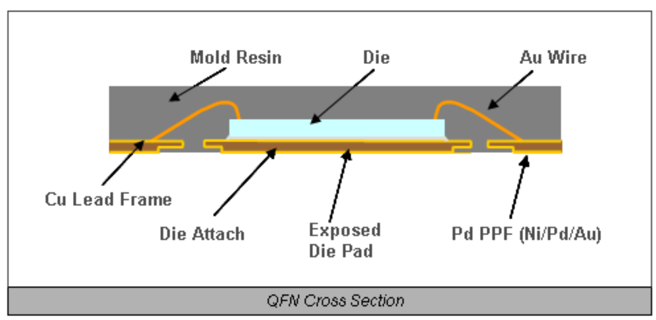

Figure 1: Sawn QFN

Designers must consider that some devices may develop oxidation on the termination ends which will not “wet” (figure 2) during assembly [4].

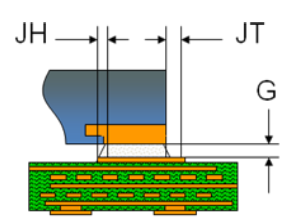

Figure 2: Bare copper terminal end

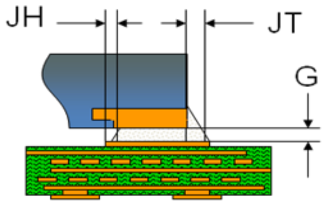

Figure 3: Plated terminal end

The exposed copper terminal end surfaces formed during the singulation process historically have not been required to be solderable. Hence, a toe fillet is not a requirement. Many factors related to assessment of assembly are defined in IPC-A-610E [5], the dimensional requirement for solderjoint thickness is not defined, wetting of course is a necessity but the toe fillet is not a requirement. The JEDEC standards state that wetting is to be evident but toe fillets are not required [3].

As discussed, the usage of QFNs is increasing and so is the diversity of end use markets which rely on these components. Those with higher reliability requirements are now seeking increased solder coverage for enhanced performance reliability and to enable automatic optical inspection..

INDUSTRY REQUIREMENTS

Currently there is no toe fillet solder requirements offered through IPC or JEDEC. End users and component manufactures understand that having a soldered edge would increase the reliability and ease of assembly inspection. Research conducted by Amkor has reported that "simulations and actual test data generated by customer have shown that fillets – if formed – can improve board level reliability as much as 2x for a package with large die to package size ratio [6].

INSPECTABILITY AND RELIABILITY

Currently, the small outline no lead devices create an electrical connection to the circuit board solely underneath the component. X-ray inspection is required to view and assess the solderjoint created. Since oxidation of the exposed copper on the punched or sawn sides prevents solder from wicking up the component edges, there is no solder on the component edge for visual inspection. Having a soldered toe fillet would enable some visual inspection capabilities on the assembly floor and not all assessment would require additional X-ray observation.

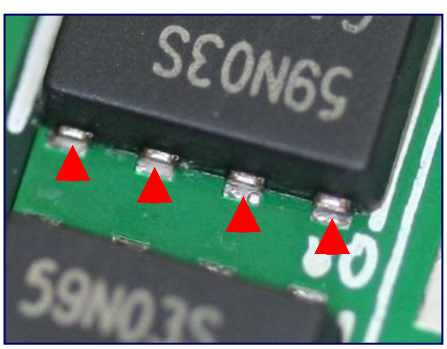

Figure 4: Location for solder toe fillet

Consequently, solder in the toe fillet area would increase the real estate of the solder joint. Concerns over cracking would be eased as the propagation of the crack would have a longer solder joint to transverse. Also, the added solder on the fillet would contribute to a stronger bond in cases of drop and vibration. Overall, increased solder in the connection of the component to the board would result in increased reliability.

WETTABLE FLANK PLATING PROCESS

We propose a chemical plating process which will provide a metallic solderability preservative to copper edges. The chemistry is flexible and can be applied vertically, horizontally or in barrel machines. The cycle is short and easy to control at the component fabrication level. The plated metal will help to ensure a solder fillet on the side wall of the singulated QFN package. The proposed process will clean the edges and make a more uniform plating surface for tin plating. Flank plating can be performed on parts after singulation either mounted on tape or in singulated form. After the plating process, no appearance or morphology change is observed to the original electroplated tin as viewed in figure 5 at 100x magnification.

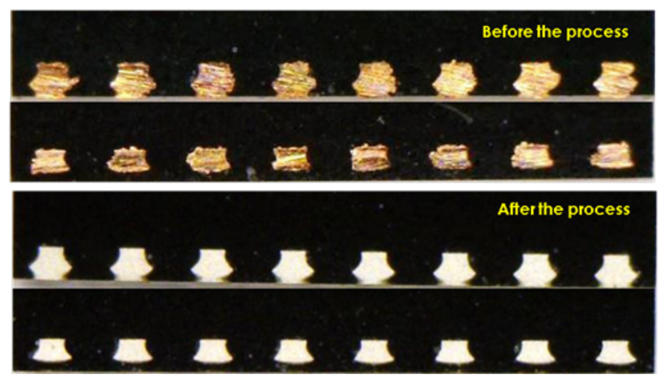

Figure 5: Comparison of QFN before and after flank plating

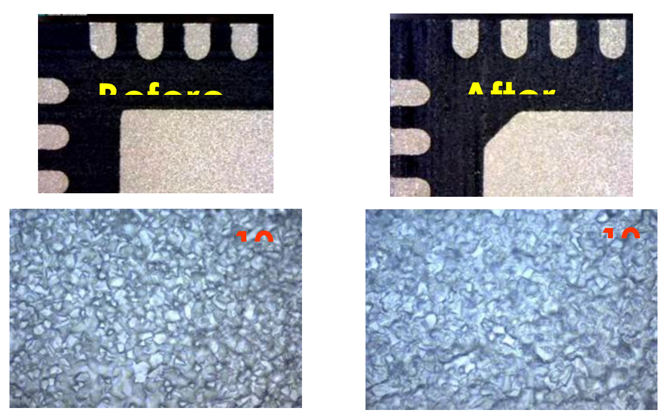

Figure 6: QFN electroplated tin before and after flank plating showing no attack of DAP and Lead terminals

The freshly plated metal is more resistant to oxidation caused by open air exposure than an untreated copper edge. The resultant tin plating will accept solder and create a soldered surface which will then enhance the integrity of the connection of the component to the circuit board. The solderjoint will then extend from the underside of the component as is standard today, then travel up the side of the component offering additional surface area of connected solder to the component. The advantage of the proposed plating process which will cover the entire side of the fillet equates to potential solder coverage of 95 to 100% edge of the QFN. This is not the case with alternative solutions such as dimple plating. A dimple plating process enables solder to wick up about 50% of the fillet. Determining the required percentage of solder needed to flow up the fillet for high reliability applications would need to be addressed by an industry group.

PERFORMANCE ASSESSMENT AND SOLDERABILITY TESTING

During development, we employed a methodical path to assess solderability. Initial testing was conducted using IPC J-Std 003 Test F, wetting balance. On copper test panels, this enabled us to screen various plating processes and refine the plating bath formulations.

From there, development was transitioned to dip and look assessment on actual components. Testing the actual components was also important as the base metal can vary from component manufacture to component manufacture. This revealed the importance of the preclean processing steps for such an application. Again using the MUST II wetting balance, we followed the JEDEC Solderability Standard JESD22-B102E [7] with a controlled dip time, location, speed and temperature.

<u>Solder Pot Method</u>

- Solder alloy: Sn96.5 Ag3.0 Cu0.5
- Solder temperature: 245°C
- Flux type: ROL1
- Immersion time in flux: 5-10 sec.
- Flux drip dry ~ 10 sec. before dipping into the solder
- Immersion time at solder: 5 sec.
- Use tweezers to grasp two corners of testing unit and dip the whole unit at 90° into the solder

Solderability of the plated flanks compared to copper only was evaluated after Steam Aging and high temperature bake by "Dip and Look." For steam aging, parts were placed in a ASTM certified steam age chamber for 8 hours of exposure. A second set was dry baked in a convection oven for 16 hours prior to solderability testing. Results on plated flanks as plated and after heat conditioning can be seen in figure 7.

PreConditioning	Toe Fillet Qty	Non Wetting or <75%	Solderability Pass (%)
As Received	256	0	100
After 8 hours Steam Age	256	1	99.6
After 16 hours Dry Bake	256	1	99.6

Figure 7: "Dip and Look" testing of plated QFN flanks after steam and bake aging

Ultimately, production simulation was conducted in conjunction with the Electronic Packaging Laboratory (EPACK Lab) of Hong Kong University of Science and Technology (HKUST). The test included full lead-free solder paste application, component placement by automatic pick and place machines and then convection reflow soldering. These results are reported in top images of figures 9 and 10.

PreConditioning	Toe Fillet Qty	Non Wetting or <75%	Solderability Pass (%)
As Received	256	0	100
After 8 hours Steam Age	256	10	96.1
After 16 hours Dry Bake	256	5	98.1

Figure 8: PCB Assembly testing of plated QFN flanks after steam and bake aging

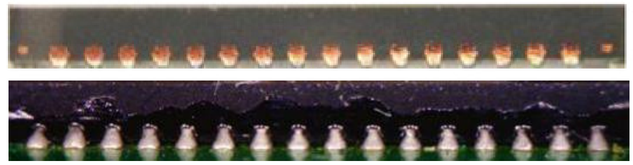

Figure 9: Visual comparison of unplated (copper) vs. plated QFN flanks as received.

All testing conducted on the edge components without treatment show no solder wetting as illustrated in figure 8.

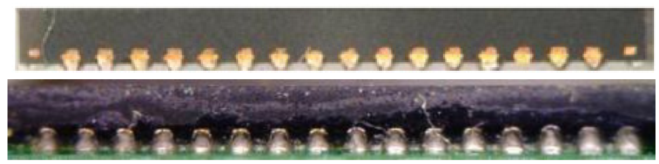

Figure 10: Visual comparison of unplated (copper) vs. plated QFN flanks after 8 hours steam aging

The plated flanks showed a large increase in wettability over the non-plated flanks and also showed a higher area coverage of the flank vs. the plated "dimple" flank approach [8].

Another concern is the possibility of package delamination due to the chemical tin plating process attack on the molding compound interfaces. CSAM analysis of the plated parts after solder shock will also be presented showing excellent adhesion as illustrated in Figure 11.

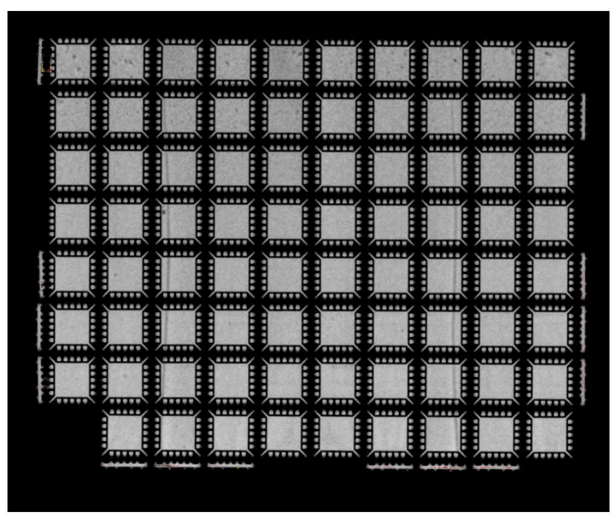

Figure 11: CSAM of flank plated molded parts after solder shock showing no delam areas in 80 unit array.

CONCLUSIONS

In conclusion, we have described a process that can provide a solderable flank after component molding and singulation which should provide significant advantages in inspectability and solder joint reliability.

Testing and further evaluations are ongoing with key OEMs and assembly houses and we hope to report these results as they progress. An industry consensus of required preconditioning to determine shelf life prior to assembly is needed for further qualification of this and other potential solutions.

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