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reliability designed, reliability delivered

Using Physics of Failure to Predict System Level Reliability for Avionic Electronics

IMAPS New England Conference

May 7, 2013

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Agenda

- Introduction
- Avionic Applications
- Common Issues
- Failure Mechanisms
- Virtual Qualification Approach
- Automated Design Analysis Solution

Avionic Applications

ARINC 429-Mil-Std-1553 Module

Gardner Aviation UniLink LRU

Cobham-Carson Sikorsky Suite

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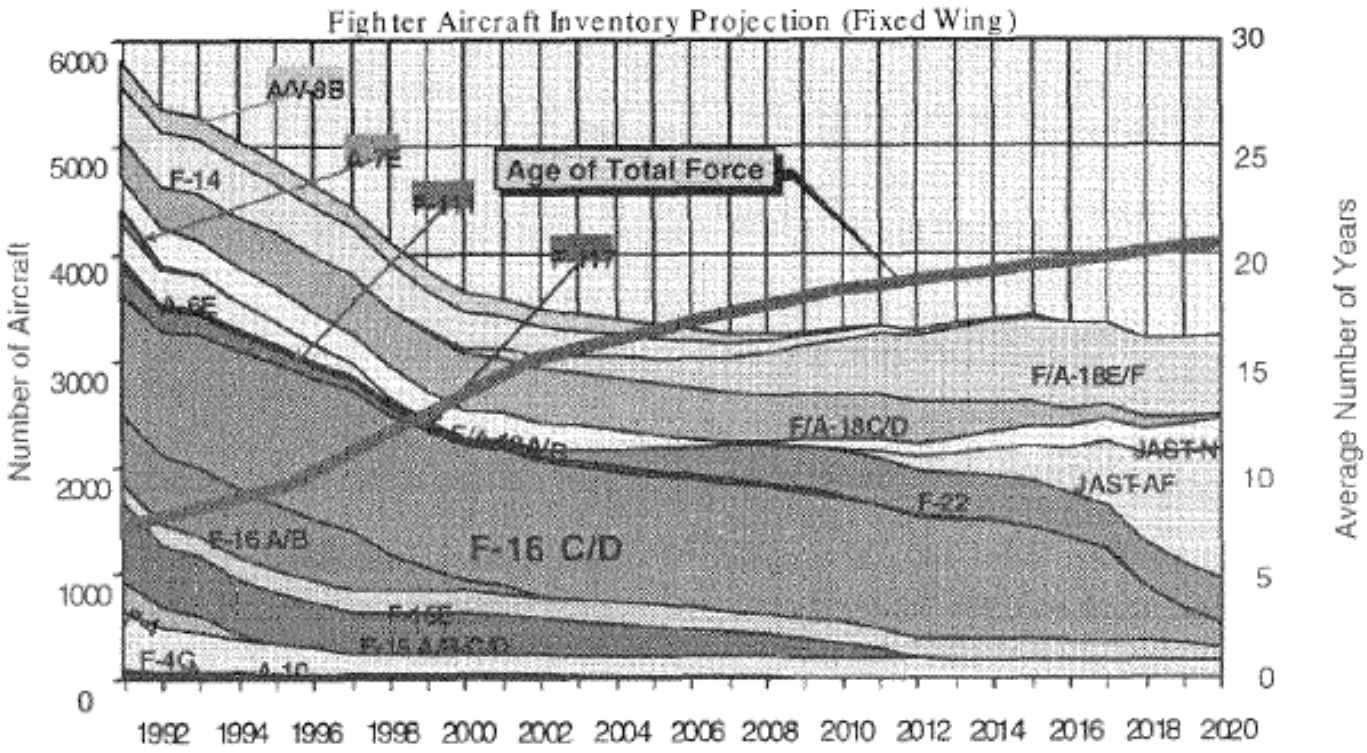
Aging Fleet



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What Do they All Have in Common?

- High Temperature Environments
- Vibration (flight, gunfire) and Shock (Landing) Environments
- Temperature and Power Cycling Environments
- High Current Flows and Thermal Transfer Requirements
- A variety of materials forming the product

Stringent Environmental Conditions

- Being used at varying temperatures or temperature extremes
- Having a temperature range of -55°C to 125°C
- Being used in an application having a medium to high shock, pressure, vibration, or moisture environment
- Being stored for later usage (over 10 years)
- Having an application life span of greater than 30 years

Failure Mechanisms

- Thermo-mechanical fatigue induced failures
  - CTE mismatch
  - Temperature swings
- Bond Wire Fatigue
  - Shear Stresses between bond pad and wire
  - Repeated flexure of the wire
  - Lift off (fast temperature cycling effect)
  - Heel Cracking
- Die Attach Fatigue
- Solder Fatigue
  - Voids
- Device Burn Out

How Can We Resolve these Issues During the Design Phase of a Product?

- Utilize an Automated Design Analysis Approach Because:
  - Mil-HBK-217 actuarial in nature
  - Physics based algorithms are too time consuming
  - Need to shorten NPI cycles and reduce costs
  - Increased computing power
  - Better way to communicate

PoF: the Complexity Roadblock

$$\tau_{HCI} \propto \exp\left[\frac{b_{HCI}}{V_D}\right] \cdot \exp\left[\frac{E_{aHCI}}{kT}\right]$$

$$L = L_r\left(\frac{V_r}{V_0}\right) \times 2^{\left(\frac{T_r - T_A}{10}\right)}$$

$$T_f \propto \exp\left(\frac{\sim 0.51eV}{kT}\right) \times \exp(\sim -0.063\%RH)$$

$$\tau_{TDDB} \propto \exp[-b_{TDDB} \cdot V_G] \cdot \exp\left[\frac{E_{aTDDB}}{kT}\right]$$

$$N_f^{-0.6} D_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785\log\frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

$$\tau_{NBTI} \propto \exp[-b_{NBTI} \cdot V_G] \cdot \exp\left[\frac{E_{aNBTI}}{kT}\right]$$

$$\tau_{EM} \propto (J)^{-n} \cdot \exp\left[\frac{E_{aEM}}{kT}\right]$$

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2-\nu}{9 \cdot G_b a}\right)\right)$$

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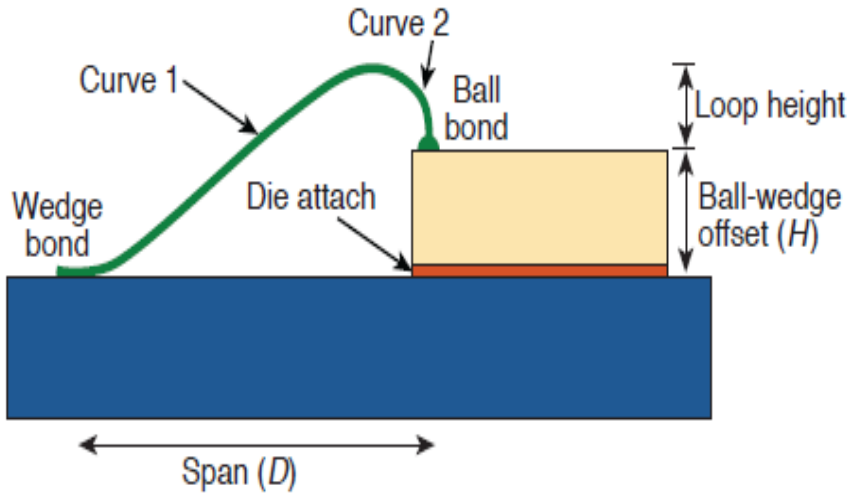
Common Failure Modes

Wire Bonds

Wire bonding has been the most common interconnect for IC packages for over 50 years. The most common materials are gold, aluminum, and more recently copper. The most common bond pad material is aluminum.

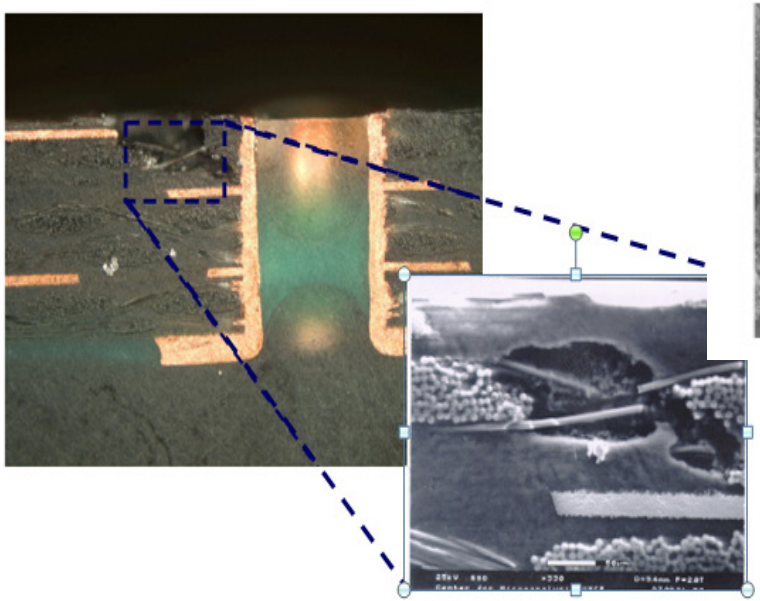


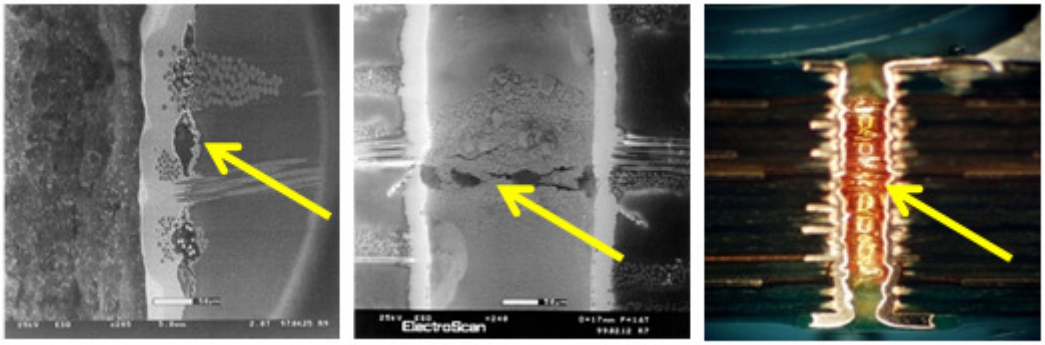
Wire bonds tend to fail if exposed to elevated temperatures (intermetallic formation), exposure to elevated temperature and humidity (corrosion) and exposure to temperature cycling (low cycle fatigue).

Common Failure Modes: PCBs

- Printed Wiring Boards have several failure modes that are detrimental to reliable operation. Failures in PCBs can be driven by:
- Size (larger boards tend to experience higher temperatures)
- Thickness (thicker boards experience more thermal stress)
- Material (lower Tg tends to be more susceptible)
- Design (higher density, higher aspect ratios)
- Number of reflow exposures

Common Failure Modes: PCBs





Plated Through Hole Failure Mechanisms: voids (left), etch pits (center) and barrel cracking from fatigue (right)

Conductive anodic filament (CAF), also referred to as metallic electromigration, is an electrochemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field. CAF can cause current leakage, intermittent electrical shorts and dielectric breakdown between conductors in printed wiring boards.

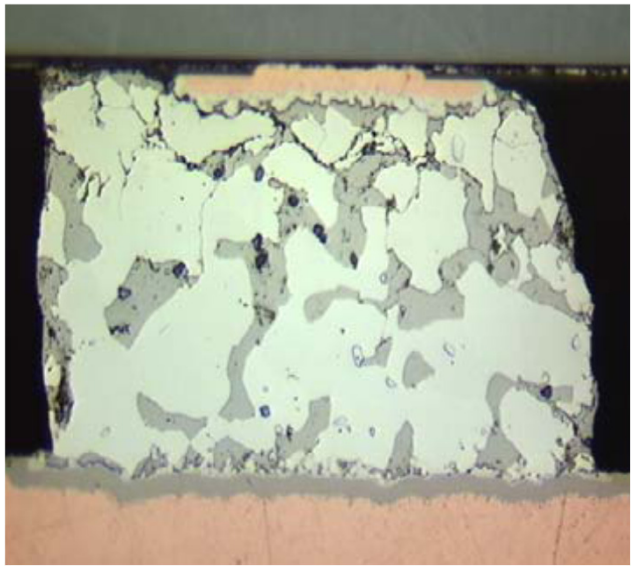
PTH voids can cause large stress concentrations, resulting in crack initiation.

Etch pits are due to either insufficient tin resist deposition or improper outer-layer etching process and rework.

Overstress cracking can occur in the PTH due to a Coefficient of Thermal Expansion (CTE) mismatch which places the PTH in compression.

Common Failure Modes: Solder Fatigue

- Thermo-Mechanical Fatigue of solder joints is one of the primary wear-out mechanisms in electronic products. This is especially true in products used outside of commercial/ consumer environments where a longer lifetime is required and more severe operating conditions exist. The analysis assesses the fatigue of the solder joints as a function of the stresses applied during its lifetime and provides insight into whether joints are susceptible to failure.



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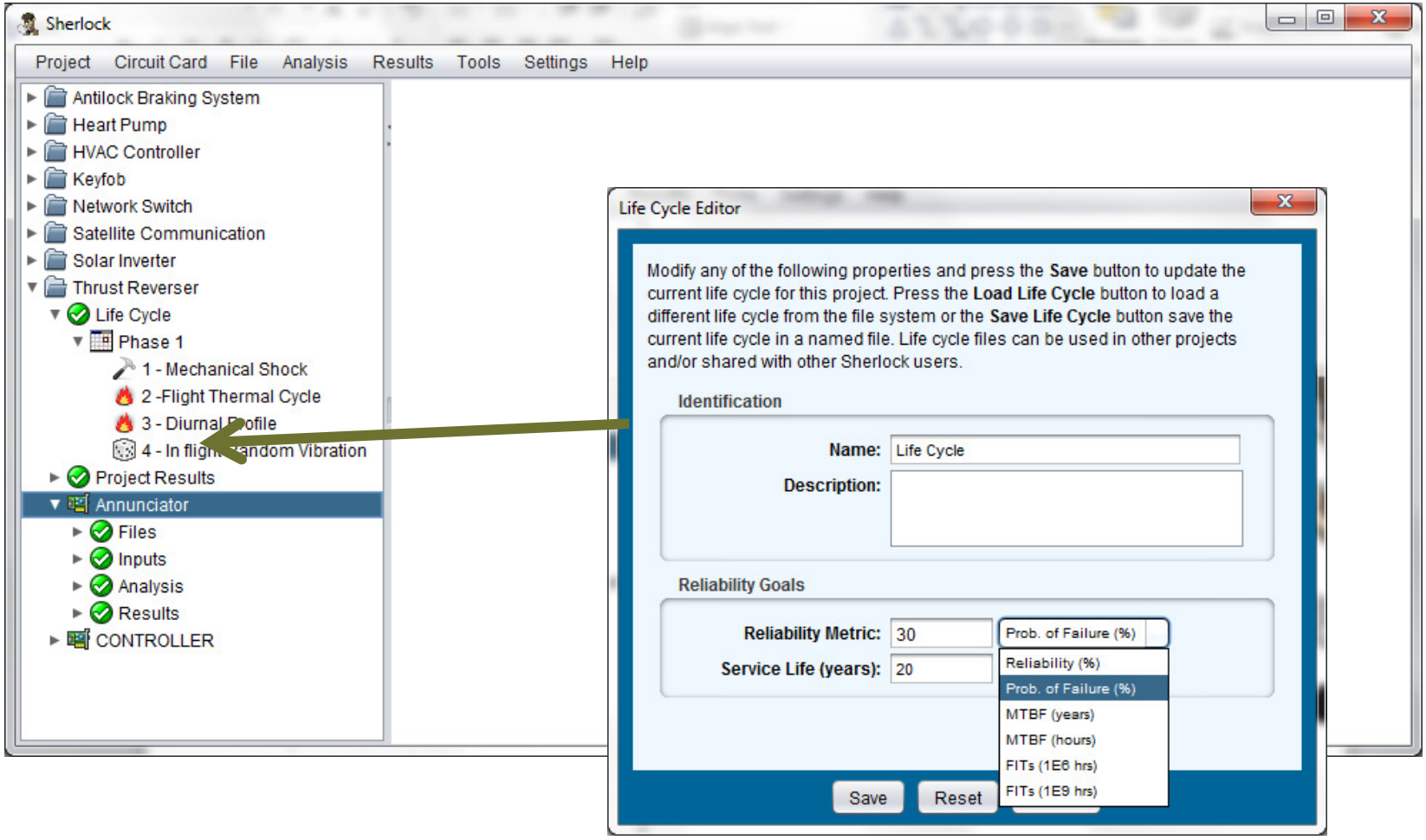
Automated Design Analysis Attributes

- Easy to Utilize
- Easy to Locate commands
- Industry Terminology
  - Parts List
  - Stack-up
  - Pick and Place
  - ODB++
  - GERBER

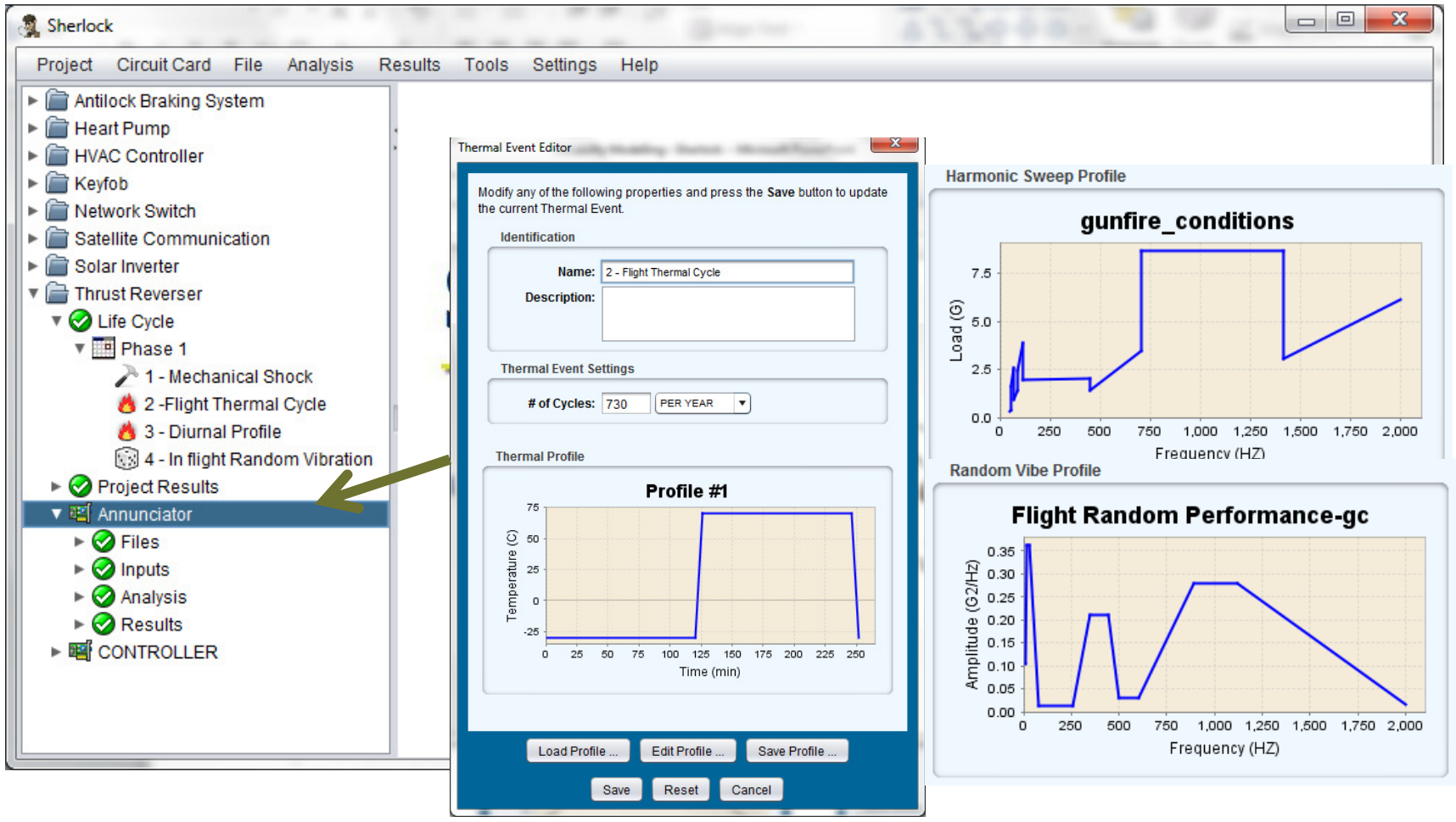
Automated Design Analysis

- There are several high levels steps involved in performing an automated design analysis. They are:
  - Define Reliability Goals
  - Define Environments
  - Add Circuit Cards
  - Import Files
  - Generate Inputs
  - Perform Analysis
  - Interpret Results

Reliability Goals

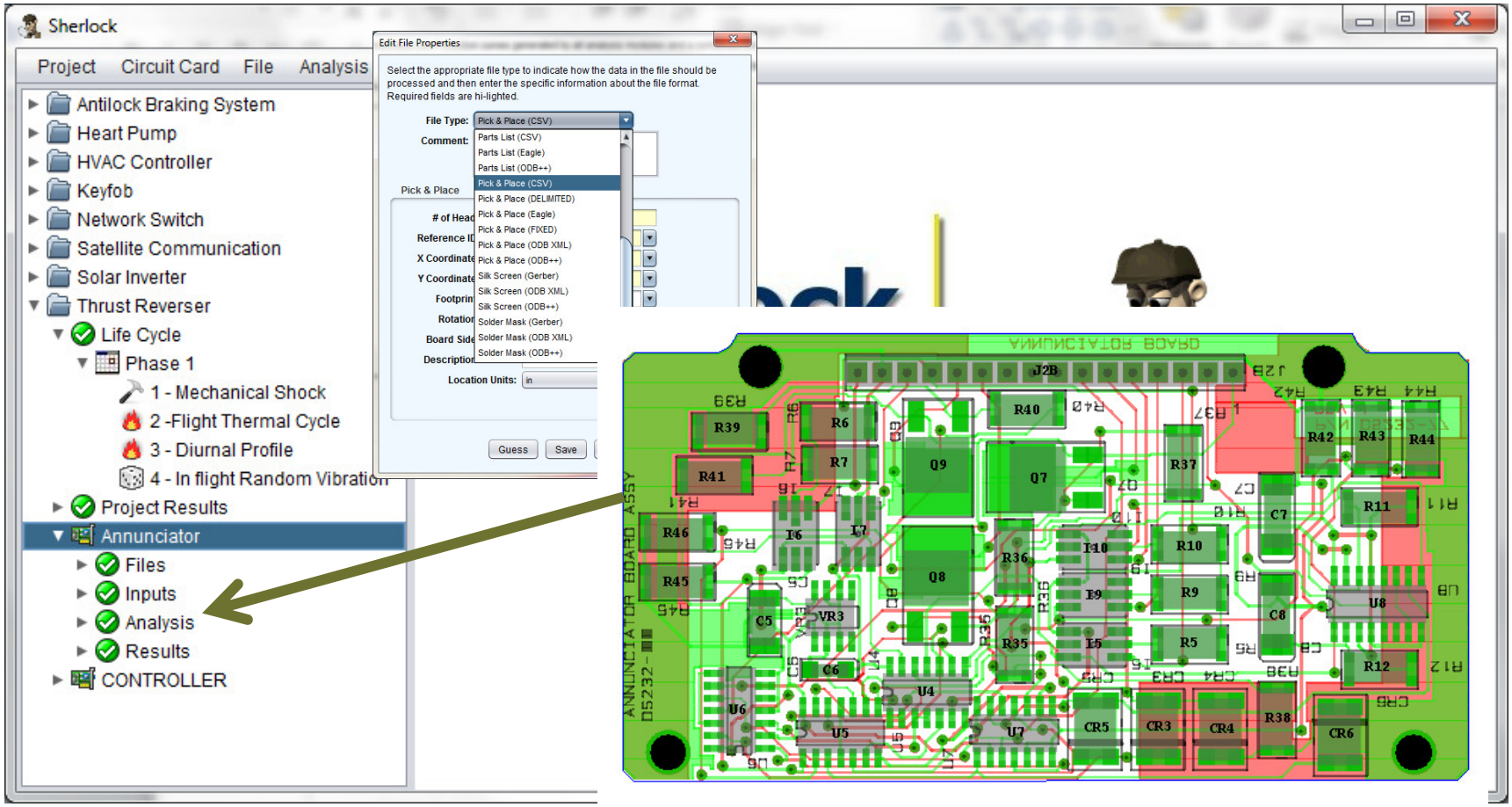


Ambient Environment



Handles Very Complex Environments

Input Design Files



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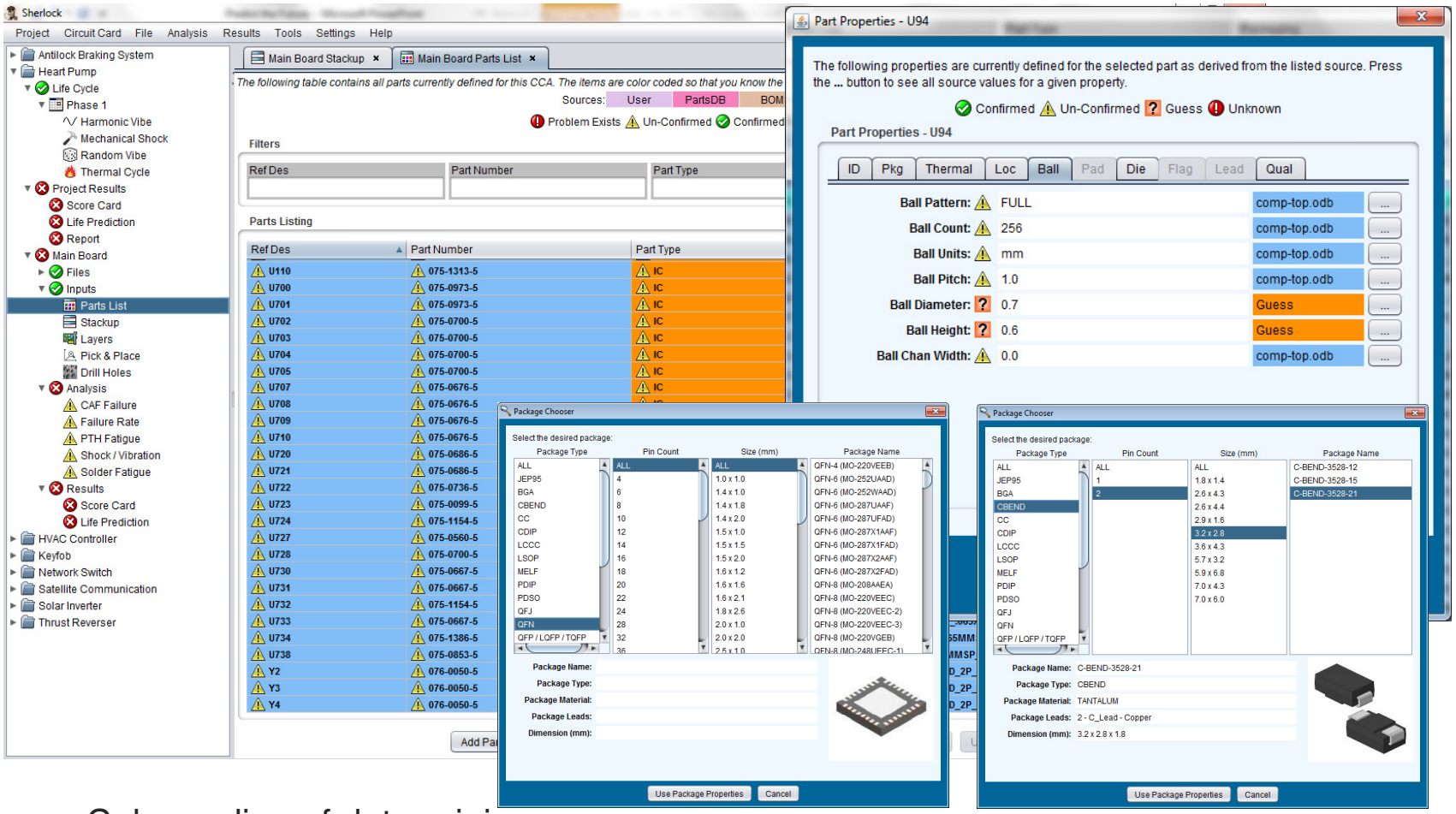
Input: Parts List



- Color coding of data origin
- Minimizes data entry through intelligent parsing and embedded package and materials database

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Inputs: Stack-Up

Stackup Properties

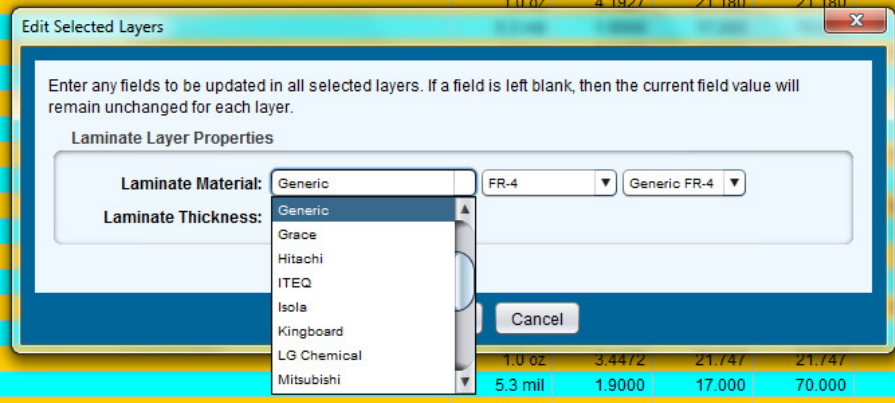
The following board properties are based on the currently defined board outline and the individual layer properties shown below:

Board Size:	370 x 178 mm [14.6 x 7.0 in]	**CTExy:**	17.519 ppm/C
Board Thickness:	1.6 mm [62.0 mil]	**CTEz:**	58.646 ppm/C
Board Density:	2.8515 g/cc	**Exy:**	35,743 MPa
Copper Layers:	10	**Ez:**	4,379 MPa

Stackup Layers

Double click any row to edit the properties for that layer **or** select one or more rows and press the **Edit Selected** button below to edit properties for a batch of layers. Press the **Generate Stackup Layers** button to replace all layers using a given PCB thickness and default layer properties.

Layer	Type	Material	Thickness	Density	CTExy	CTEz	Exy	Ez
1	POWER	COPPER (33.7%)	1.0 oz	4.1927	21.180	21.180	45,838	45,838
2	Laminate	Generic FR-4					24,804	3,450
3	POWER	COPPER (92.2%)					05,099	105,099
4	Laminate	Generic FR-4					24,804	3,450
5	POWER	COPPER (50%)					62,350	62,350
6	Laminate	Generic FR-4					24,804	3,450
7	POWER	COPPER (92.2%)					05,099	105,099
8	Laminate	Generic FR-4					24,804	3,450
9	POWER	COPPER (91.1%)					03,984	103,984
10	Laminate	Generic FR-4					24,804	3,450
11	POWER	COPPER (19.9%)					31,859	31,859
12	Laminate	Generic FR-4					24,804	3,450
13	POWER	COPPER (92.2%)					05,099	105,099
14	Laminate	Generic FR-4					24,804	3,450
15	POWER	COPPER (23.2%)	1.0 oz	3.4472	21.747	21.747	35,202	35,202
16	Laminate	Generic FR-4	5.3 mil	1.9000	17.000	70.000	24,804	3,450
17	POWER	COPPER (92.2%)	1.0 oz	8.3462	18.021	18.021	105,099	105,099
18	Laminate	Generic FR-4	5.3 mil	1.9000	17.000	70.000	24,804	3,450
19	POWER	COPPER (20.9%)	1.0 oz	3.2839	21.871	21.871	32,872	32,872



- Automatically generates stackup and copper percent (%)
- Embedded database with almost 400 laminate materials with 48 different properties

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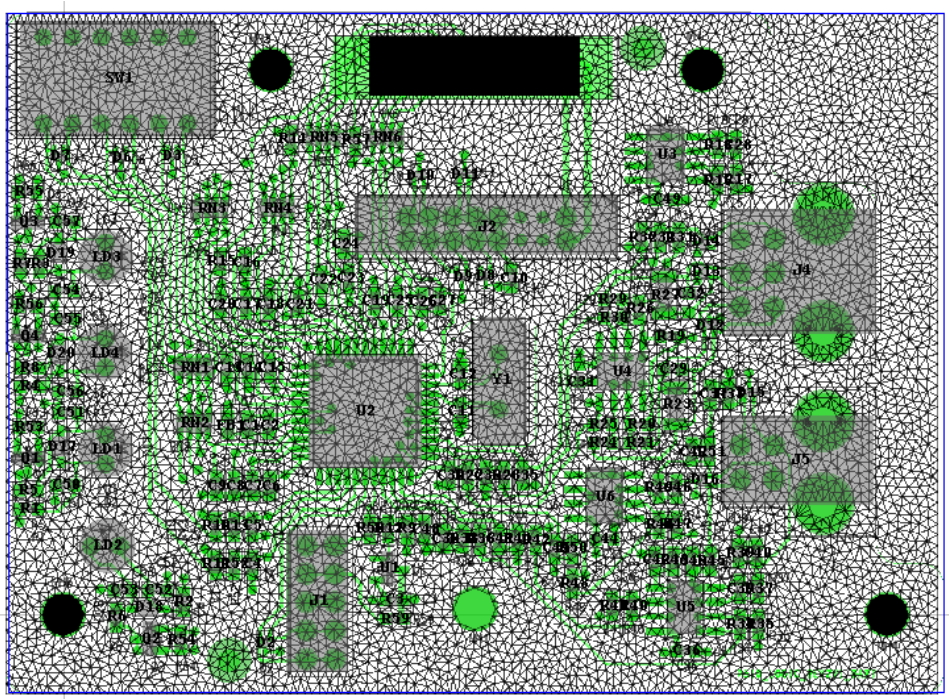
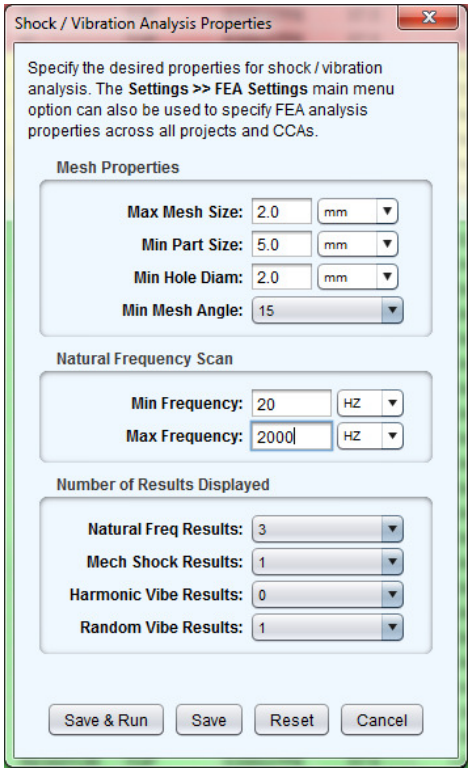
Analyses

- Eight different analyses can be performed. They are:
  - CAF – Conductive Anodic Filament Formation
  - Plated Through Hole Fatigue
  - Solder Joint Fatigue
  - Finite Element Simulations
  - ICT Impact
  - DFMEA
  - Vibration Fatigue - Natural Frequencies
  - Mechanical Shock

Results: Automated Mesh Generation





- Identifies optimum mesh density based on board size
- Expert user no longer required; model time reduced by 90%

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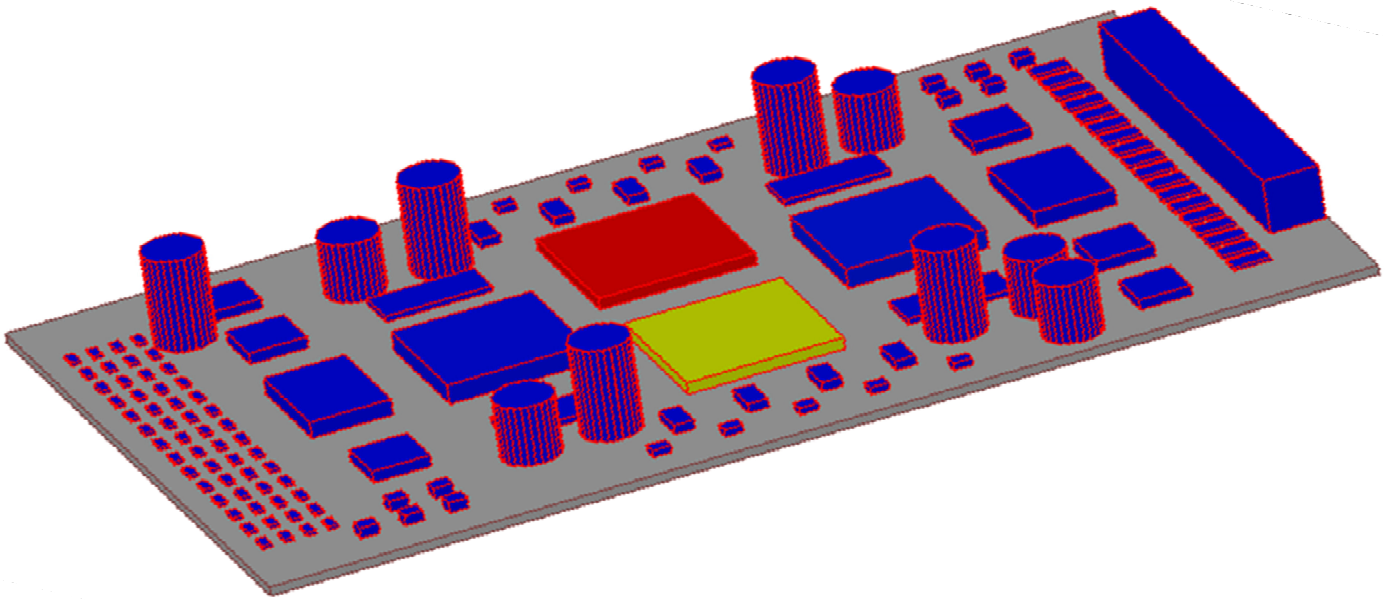
3D Output

The analysis can also establish 3D models by creating a mesh structure and the model from the data input to the analysis.



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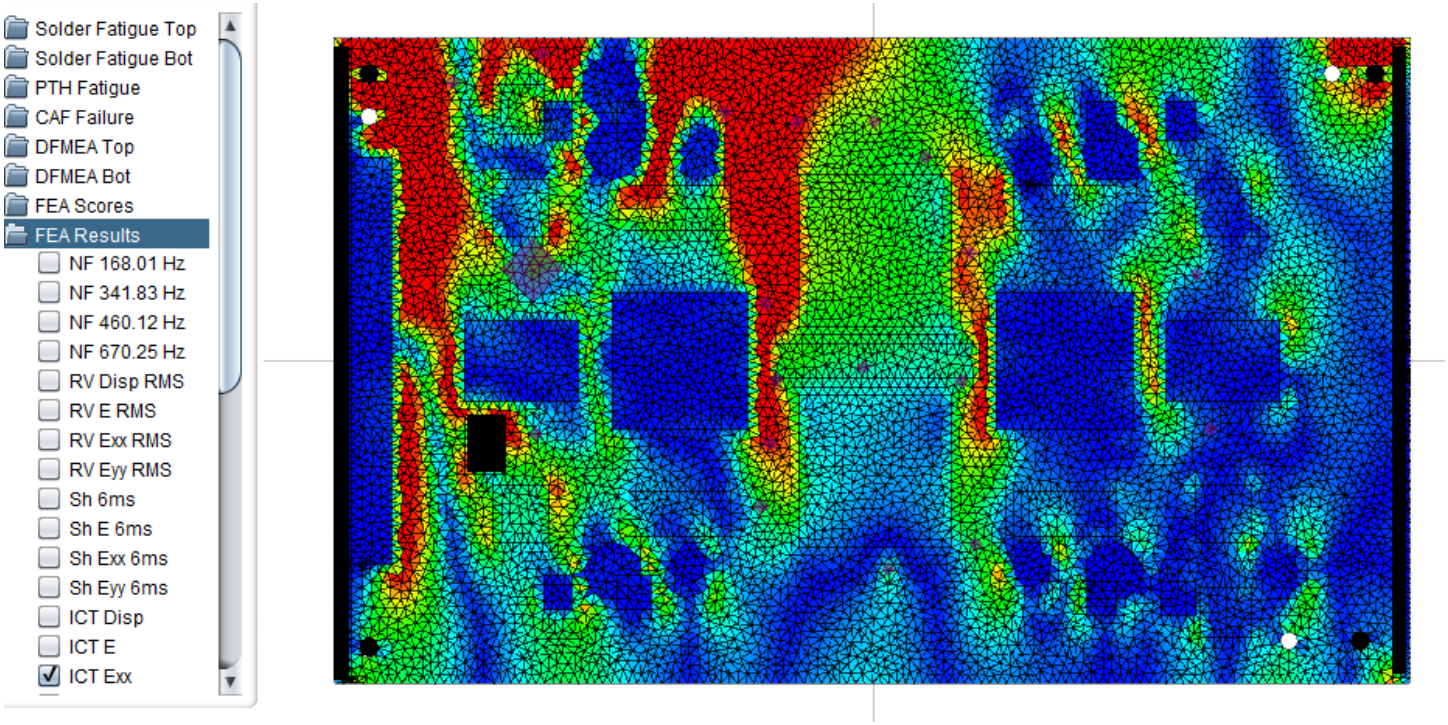
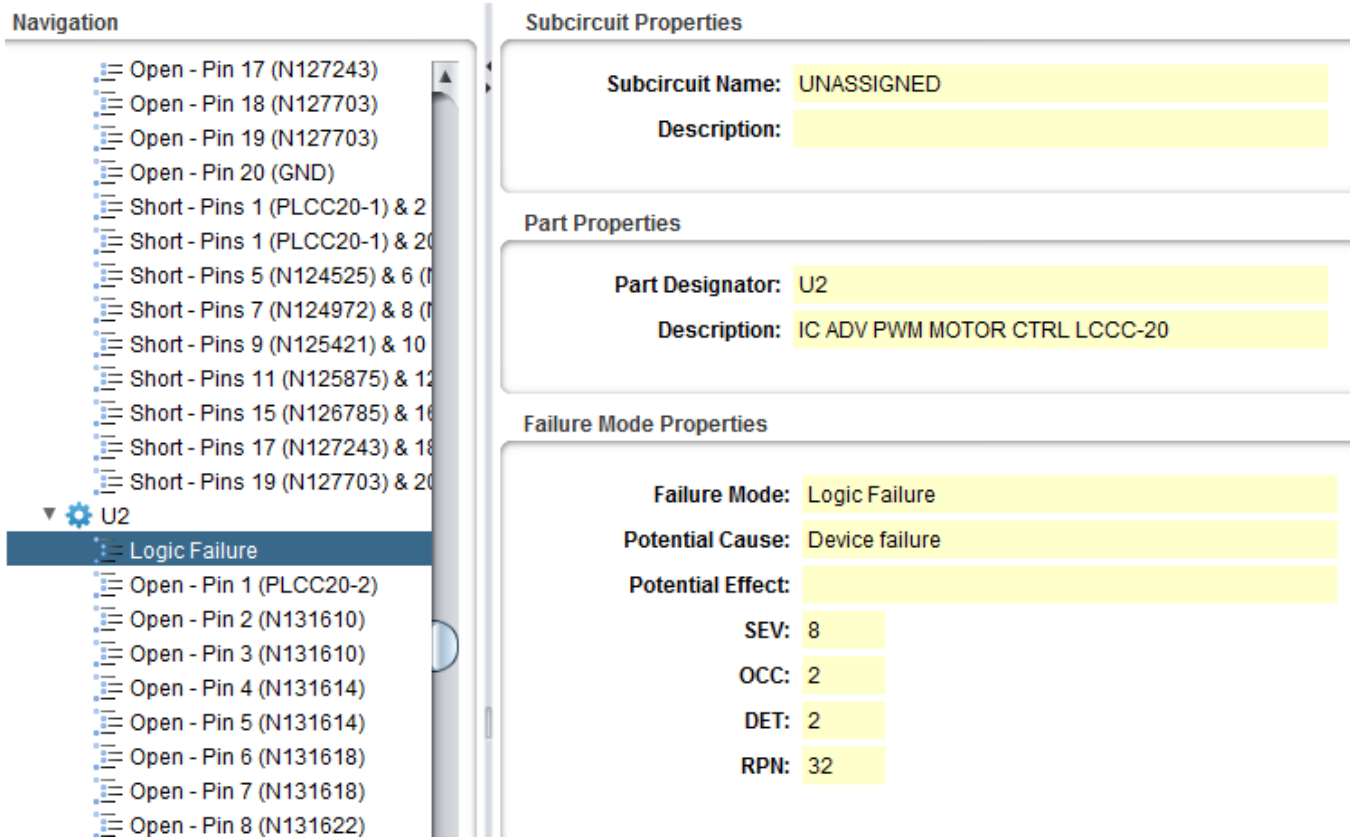
In-Circuit Test Evaluation



- Uses embedded FEA engine to compute board deflection and strain cause by ICT fixture

DFMEA



- Uses ODB++ data including net list to create board level DFMEA
- Includes customizable spreadsheets for export

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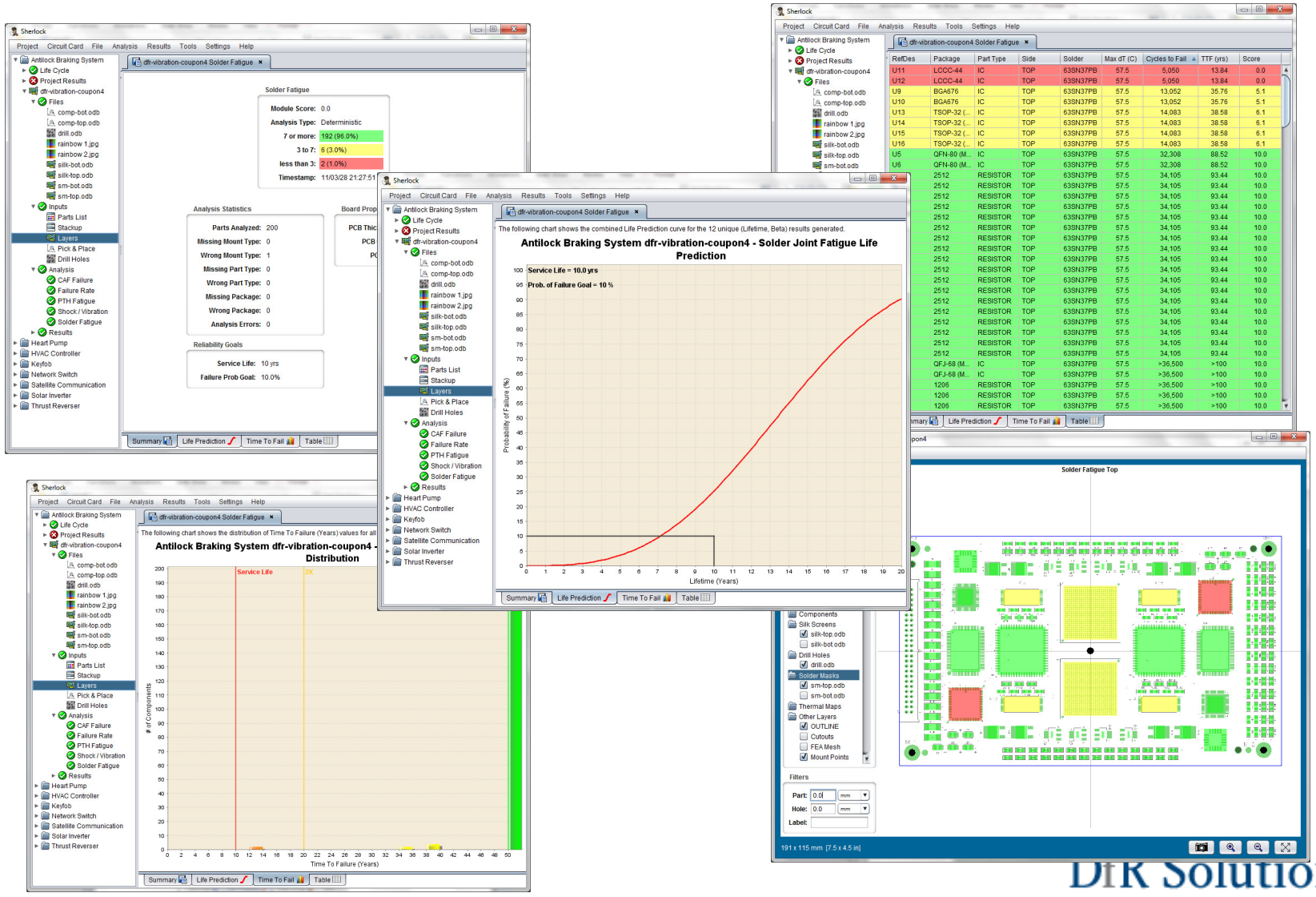
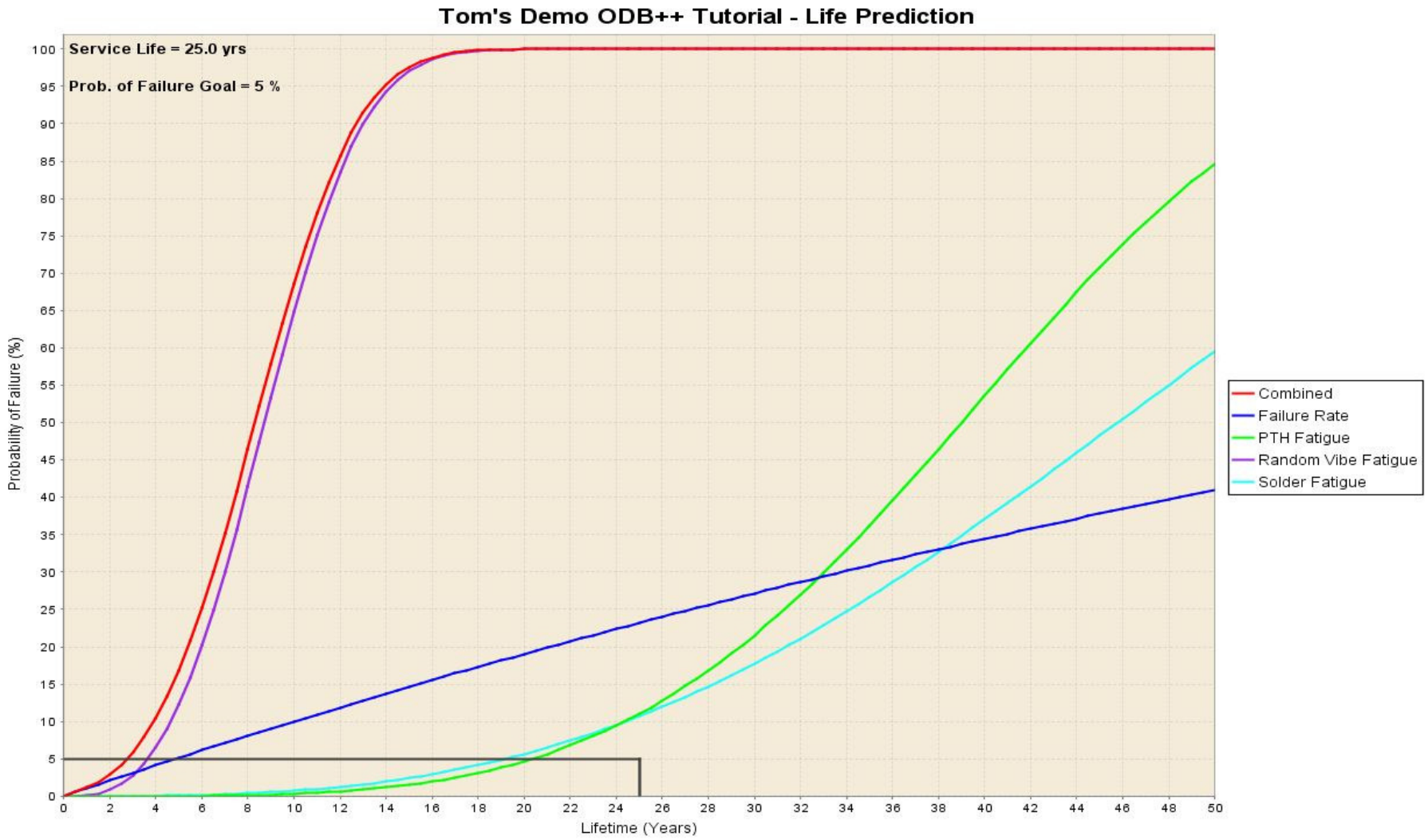
Results: Five Different Outputs



Unreliability Curves



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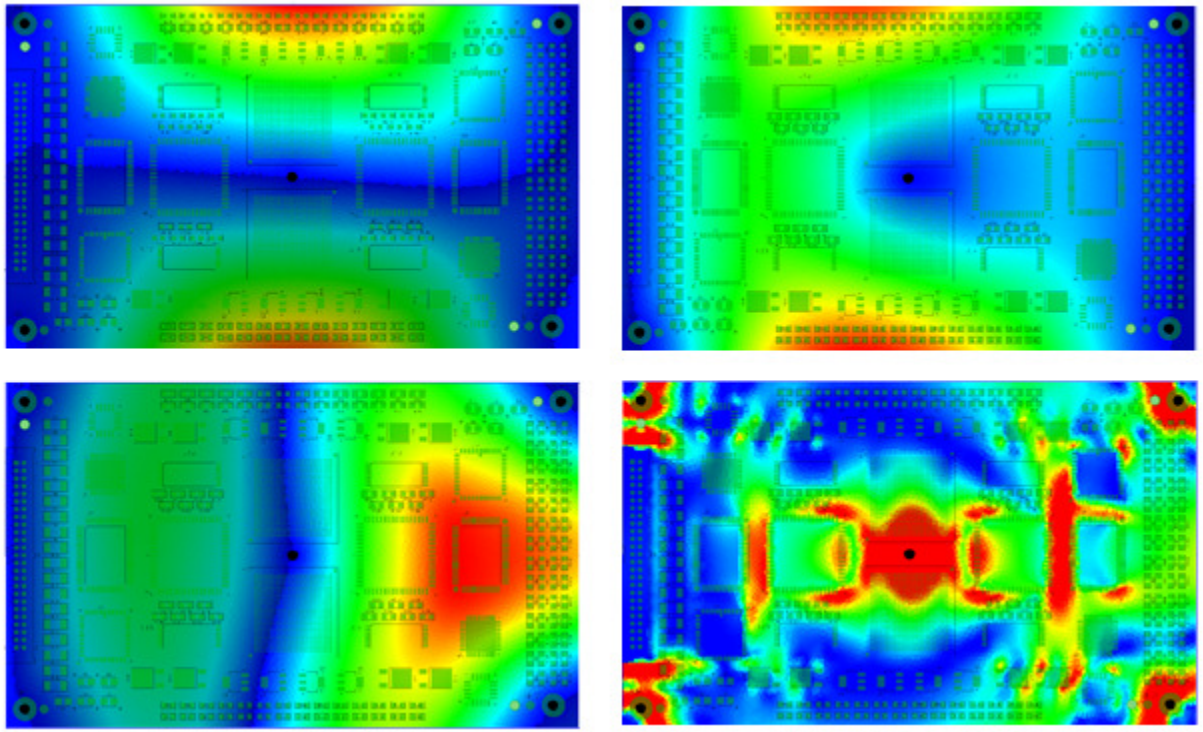
Natural Frequencies



Natural Frequencies Identified (1st-upper left), (2nd-upper right), (3rd -lower left) and 4th – lower right)

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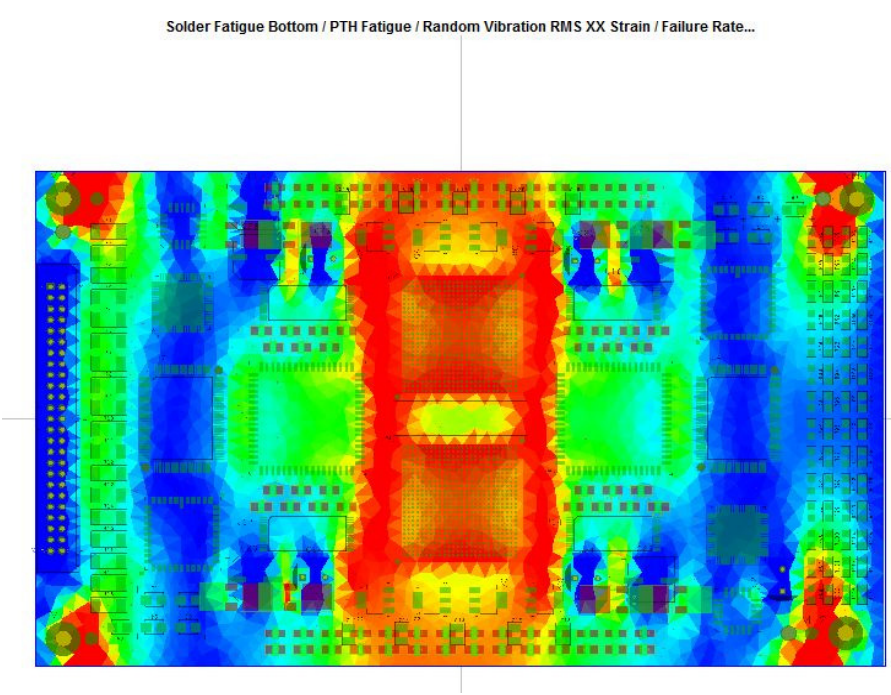
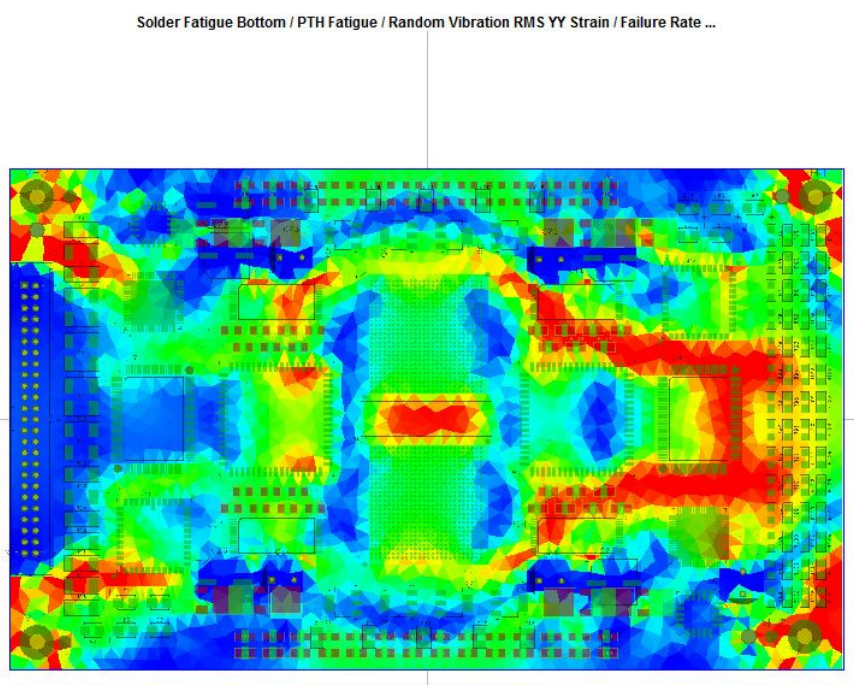
Vibration Strain Levels

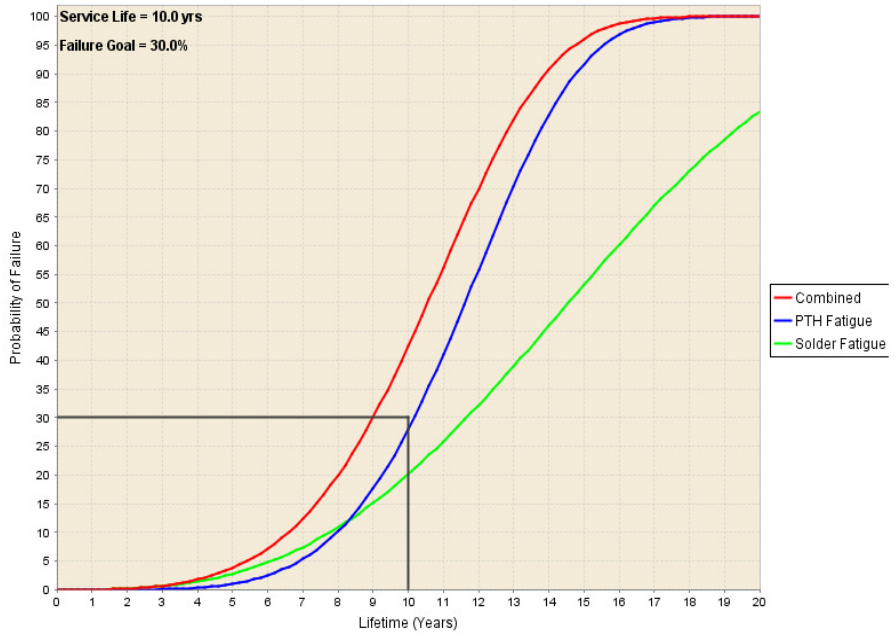


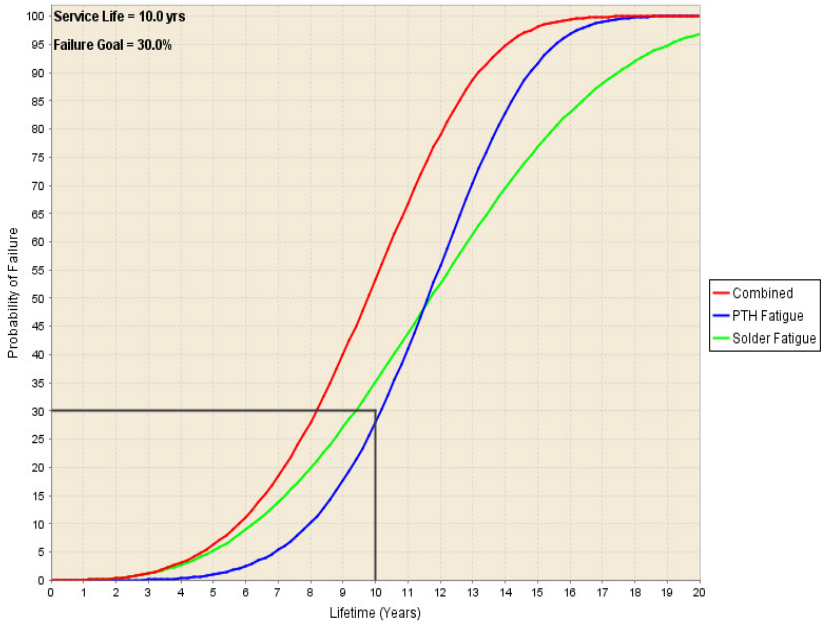


In addition, the analysis can provide data regarding the strains applied to the circuit board as a function of the vibration stress levels. The left illustrates this data in the XX direction and YY in the right image.

What If?

Comparison of Sn/Pb (left) and SAC305 (right) with respect to solder fatigue





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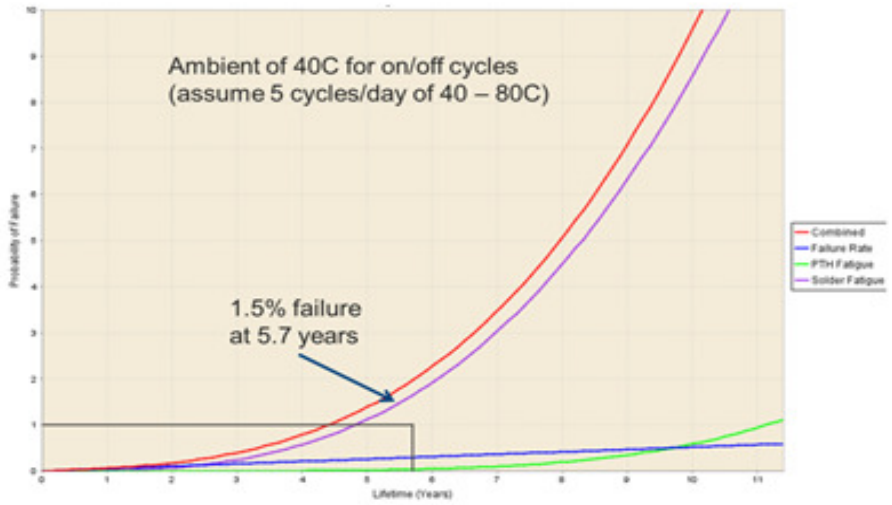
Product Test Plans

- Product test plans, also known as design verification, product qualification, and accelerated life testing (though, these are not the same thing), are critical to the successful launch of a new product or new technology into the marketplace.
- These test plans require sufficient stresses to bring out real design deficiencies or defects, but not excessive levels that induce non-representative product failure.
- Tests must be rapid enough to meet tight schedules, but not so accelerated as to produce excessive stresses.
- Every test must provide value and must demonstrate correlation to the eventual use environment (which includes screening, storage, transportation/shipping, installation, and operation).



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Thank You!

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