“High Reliability Products” What does it really take – A Test Perspective

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Abstract:

The Printed Wiring Board(PWB) industry, influenced by Semiconductor industry, strongly needs reassessment of its ability to satisfy the semiconductor needs and ultimately the customer needs and that is “High Reliability products at lower cost”

The production testing of a printed circuit board, while an integral part of PWB manufacturing, has risen to an indispensable level. Increasing board complexity, coupled with fine features has created a condition where the confirmation of board quality is needed as to avoid losses by assembly of a defective board.

This paper will explore how test can be an integral part of manufacturing to assure High Reliability Products. We will discuss how test parameters and test techniques are effective in finding time zero vs. time dependent defects. Understanding of manufacturing processes in terms defect levels as well as defect types is very critical in defining test parameters, new test techniques and test alternatives. This ultimately can improve the yield, quality, and reliability. We will discuss the types of defects, time zero vs. time dependent defects, test parameters and effectiveness and new test techniques to find time dependent defects.

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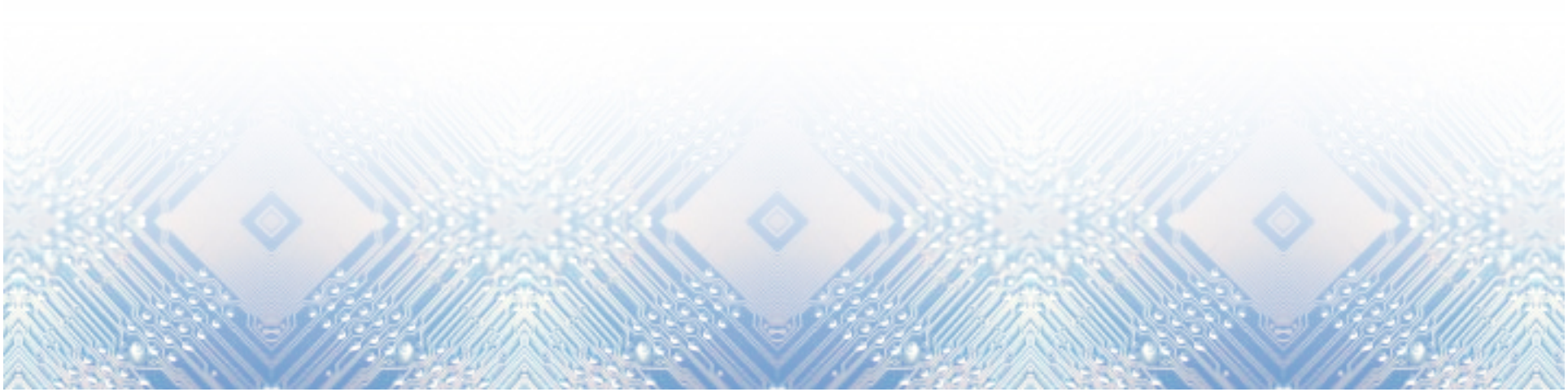


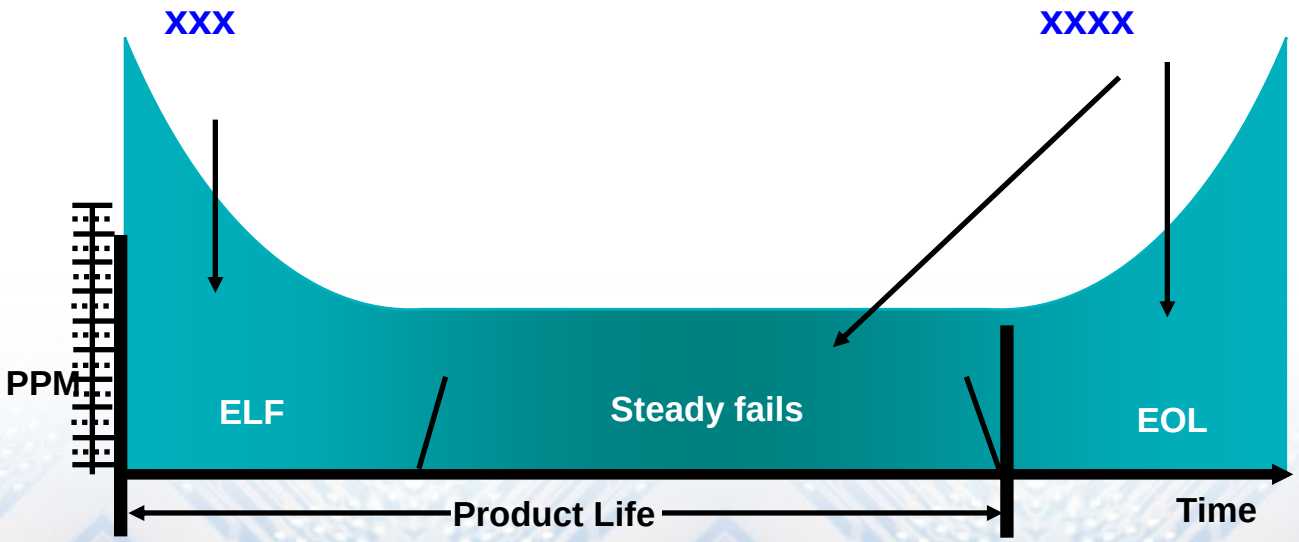
Agenda

- **Reliable Products – What does it mean?**
- **Test Strategy – How Test is an Integral part of Quality**
- **Types Of Defects**
- **Test Parameters And Data**
- **Test Techniques**
- **Q & A**

High Reliability Products

What does it mean?

- ✓ **Reduce or Eliminate fails after Assembly**
- ✓ **Reduce or Eliminate Early Life Fails(ELF)**
- ✓ **Reduce Steady Fails through product life cycle**



High Reliability Products

- How do you reduce or eliminate scrap after assembly of components?
- Reduce or Eliminate Early Life Fails or Field fails?

Must understand

PWB(Organic Chip Carrier) Structure/Complexity
Processes and Process Induced defects
Test Strategy and its Effectiveness

High Reliability Products

- **PWB or Laminate Chip Carrier Complexity**

  ➔ **must consider product design attributes**
  - ✓ **Line width/spacing**
  - ✓ **linear inches of circuitry**
  - ✓ **dielectric thickness**
  - ✓ **drill size vs clearances**

High Reliability Products

Test Strategy

- At which level of build, should test be done? Type of Testing at each level?

  ➔ Power core level, Signal core Level, or Finished raw board level?

  - ✓ Must understand type of defects and its impacts on board performance and yield objectives
  - ✓ Test efficiency by defect type

- Does the board require special Testing to improve Reliability?

  ➔Low voltage vs high voltage test?

  ➔Latest Test?, A new test technique to find near opens electrically.

  ➔Any other special Test to satisfy customer objectives?

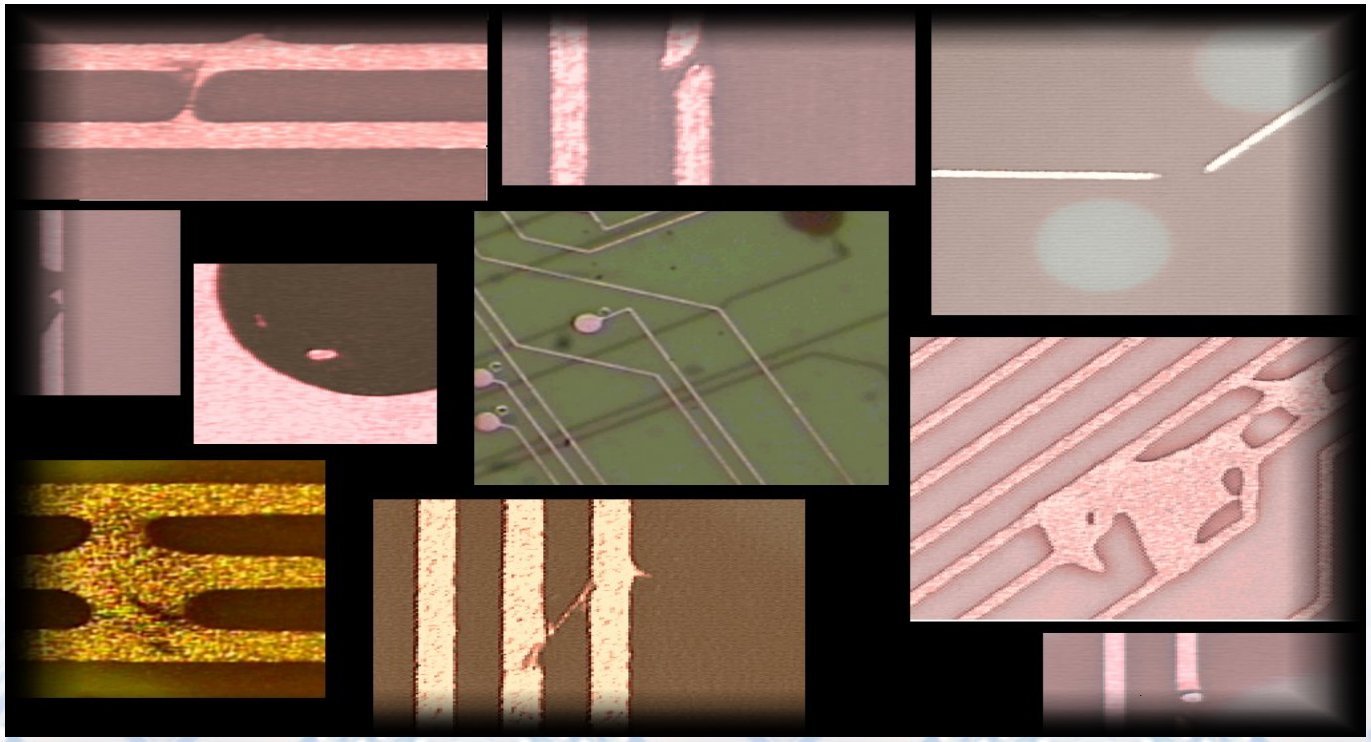
High Reliability Products

- **Types of Defects**
  - **Understanding Time 0 Vs. Time Dependent Defects**

- **Hi-Reliability Test**
  - **Electrical Test**
    - ✓ **Parameters**
  - **Test Techniques**
    - ✓**AOI(Automated Optical Inspection)**
    - ✓**Latest Test**
    - ✓**Hi-Pot Test**

Types of Time Zero Defects

- **Time Zero Defects**
  - ➔**Opens, Shorts**
  - ➔ **Any conventional test equipment can find these defects**



Time Dependent Defects

- **Near Opens(Neckdowns/dishdowns/crack circuit lines)**
  - ➔ **Impact**
    - ✓ **Intermittent resistive behaviour (Intermittent fails or No Defect Found)**
    - ✓ **Latent Open circuit line**

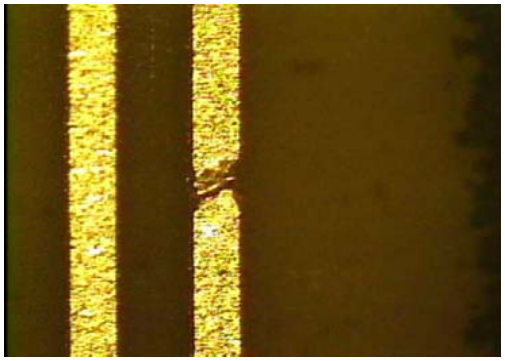
- **Metallic contamination/Laminate voids/near shorts**
  - ➔ **Impact**
    - ✓ **System Failure/shutdown**

Types of Time Dependent Defects

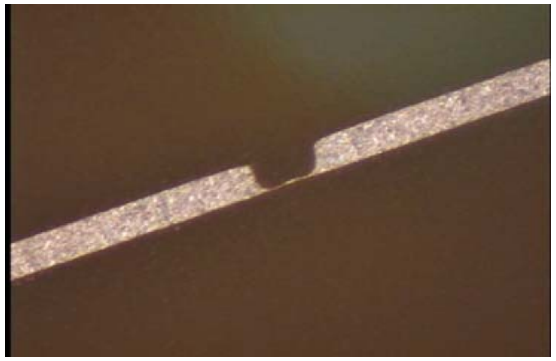
- Time dependent Defects
  - ➔Near Shorts,leakage
  - ➔Near Opens

Neckdown

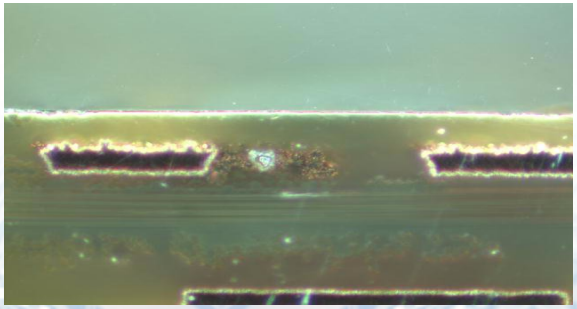
Dishdown



Neckdown



Leakage fail



Leakage fail

Assembly stresses induced defects. Raw board test at 250V may not find these type of defects.

Electrical Test Parameters for Time dependent shorts/leakages

- **Are electrical parameters critical?**
- **"Low voltage vs High Voltage Test" What does it mean to board reliability?**
  - ✓ **Selection of voltages to find certain type of defects is very essential:**

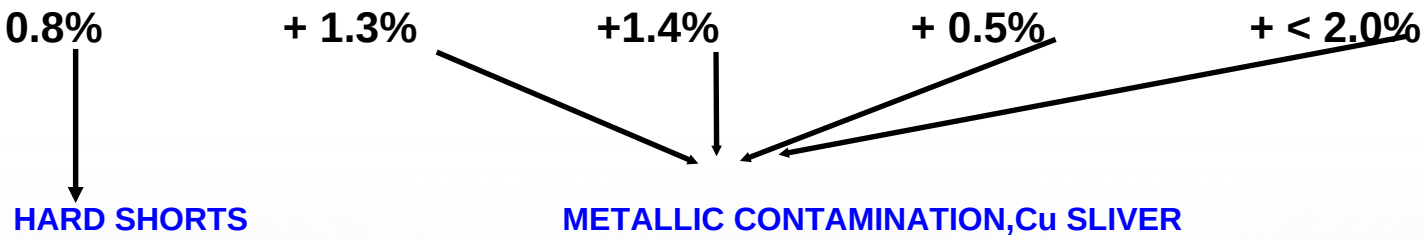
Electrical Test Parameters

- **How do you choose Electrical Test Parameters?**
  - ✓ **product design attributes**
  - ✓ **process induced defects**
- **Can 20V, 100V or 250V find all time dependent shorts/leakages?**
  - ✓ **must validate the data through IR(Insulation Resistance) testing**

Electrical Test Parameters-Voltage

ELECTRICAL TEST RELIABILITY
Shorts/Leakage Shorts

20V	100V	250V	500V	500V
100KOHMS	5MOHMS	10MOHMS	300MOHMS (pre-assembly)	300MOHMS (post assembly)



Note: 1. The %of fail is additive

Electrical Test Reliability

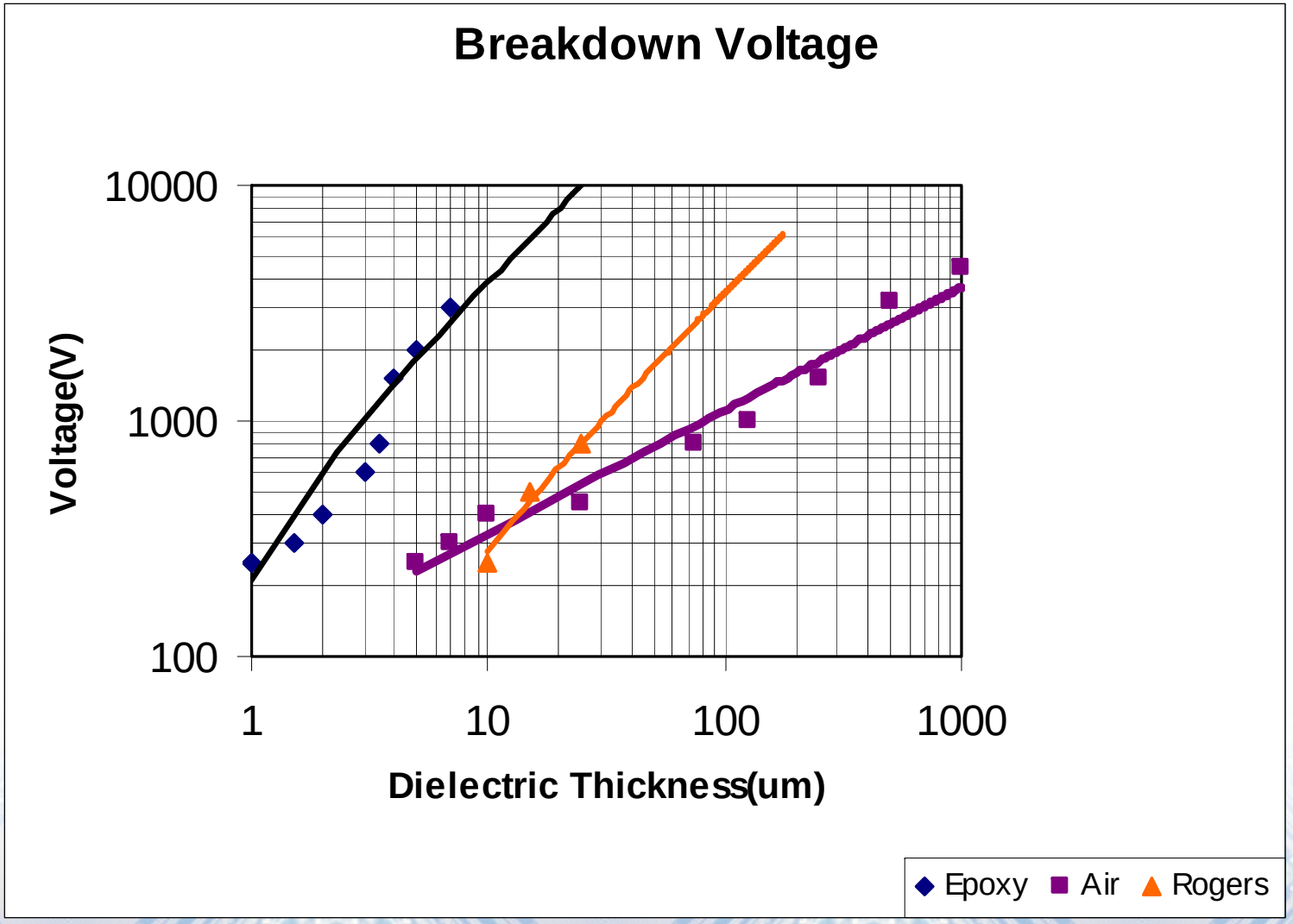
Total boards=67	TESTED GOOD	FAILED/defects	NEW FAILS
250V 10MEG	55	12/12	N/A
500V 300MEG	55	12/12	0
500V 300 MEG AFTER 2XIR	54	13/16	4

Hi-Pot Test

Why do you need Hi-Potential Test?

- ✓ **Must ensure that the dielectric can withstand its specified voltage**
- ✓ **Must ensure that the dielectric is free of contamination, voids that can result in time dependent defects**
- ✓ **Hi-Pot Test must be used when the inner layer dielectric thickness is low, specifically for voltage and ground layers**

Electrical Test Reliability



Sample data - Leakage Test vs IR Test

50c/80%RH,5V,1000 hours

Net	Coupon	Lkg Test-250V	Lkg Test-500V	IR Results
1	D	Pass	Pass	Pass
2	C	Pass	Pass	Pass
3	A	Pass	Pass	Pass
4	B	Pass	Pass	Pass
5	D	Pass	Pass	Pass
6	C	Pass	Pass	Pass
7	A	Pass	Pass	Pass
8	B	Pass	Pass	Pass
9	D	Pass	Pass	Pass
10	C	Pass	Pass	Pass
11	A	Pass	Pass	Pass
12	B	Fail	Fail	Fail
13	D	Pass	Pass	Pass
14	C	Pass	Pass	Pass
15	A	Pass	Pass	Pass
16	B	Pass	Fail	Fail
17	D	Pass	Pass	Pass
18	C	Pass	Pass	Pass
19	A	Pass	Pass	Pass
20	B	Pass	Fail	Pass

- **Example of correlation between time zero Leakage Test and IR Test**
- **Leakage Test and IR testing done after assembly simulation**

Reliability VS Test Voltage
PTFE

DATA:

ALL PARTS PASSED 250V/10MOHMS EOL TEST

1. 37 modules thru TH&B(85C/85%RH/3.7V/1000 hours)
NO FAILS

2. 43 modules thru HAST(110C/85%RH/3.7V/264 hours)
NO FAILS

Reliability VS Test Voltage
PTFE

- **6 parts of Group A tested at 250V, 10Mohms and passed.---> No fails at HAST - All Voltage and ground nets used due to high risk sites for shorts**
- **10 parts of Group B tested at 100V, 10 Mohms and passed, but all failed 250V,10Mohms**
  - **same nets were used because of no charring,still leakage fails at 250V,10Mohms**
- **12 parts of Group C tested at 10V,1 Mohms and passed, but all failed 100V,10Mohms Test**
  - **same nets were used because of no charring,still leakage fails at 250V,10Mohms**

Note : In HAST testing the nets wired were V1 or V2 to GND.

	Group A	Group B	Group C
No. Parts	6	10	12
EOL Test	250V,10Mohms	100V,10Mohms pass but failed 250V,10Mohms	10V,1Mohms pass but failed 100V,10Mohms
Retest post Precon	PASS	PASS-same as above	PASS-same as above
HAST	No fails	No fails	3 fails 1-passed after bake

Near Opens

How do you find Near Opens?

- **AOI is the industry choice**

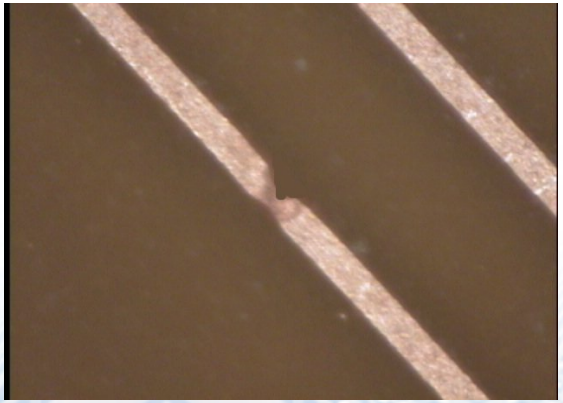
  AOI can find neckdowns and dishdowns - but surface defects only

  Cannot find inner layer defects at finished raw board level

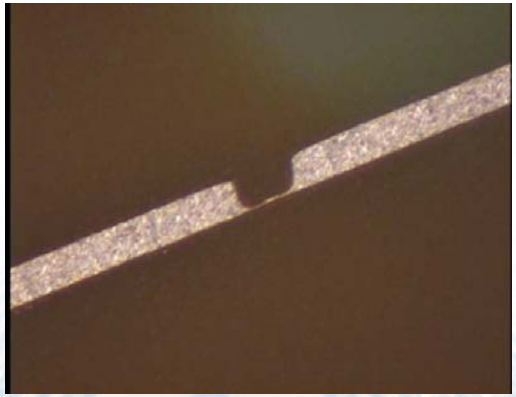
  A defined escape level exist from AOI Sector as well as defects induced through lamination/soldermask stresses

- Are there other methods to find these defects at finished raw board level?

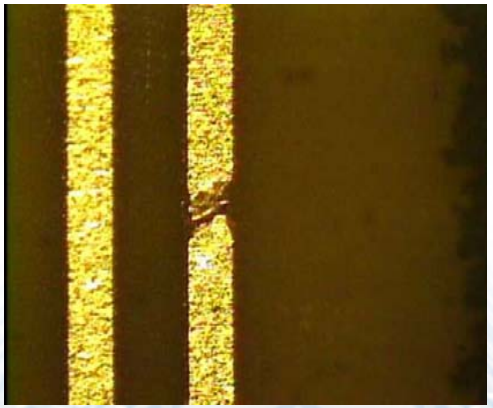
Neckdown



Neckdown



Dishdown



AOI Sector Efficiency is low due to human judgement at defect verification

Unique Test Technique
Latest Test

- The Latest Test is performed at finished bare board level
- Flying Probe is used for this test
- The Latest Test will find time dependent open defects electrically
- Defect Criteria
  - Nicks / Height Reductions in Circuit Traces
  - Will find % of the Cross Section Remaining in a Circuit Trace
  - For Example

    The parts with 5 mil line width and 1.0 mil thickness.

    The Latest will find 20% of the cross section remaining means

    Latest Defect Detection = 5X0.2 = 1.0 Sq. mil or less Cross Section left
- Performed on all High Reliability Products since 1980's
  - *No circuit line open Field Fails*

Latent Open Defect Data Analysis

Test Method	Defect criteria	False Defects	Comments
AOI	50% line width reductions	>10 per signal side	surface defects Human judgment
Latest	% of cross section left	non significant	performed at finished board level

Typical escape level from AOI

AOI	Latest Test	ELF or Field Fails
All layers through AOI	0.5%-1.0% (complexity dependent)	Non-Significant

- 384 line width reductions(less than 1sq.mil cross sectional area) that includes the Latest passes and fails were subjected to Assembly and Field Simulation.
- 324 Latest passes remain stable after assembly and field simulation
- Of the 60 Latest fails, 7 became defects

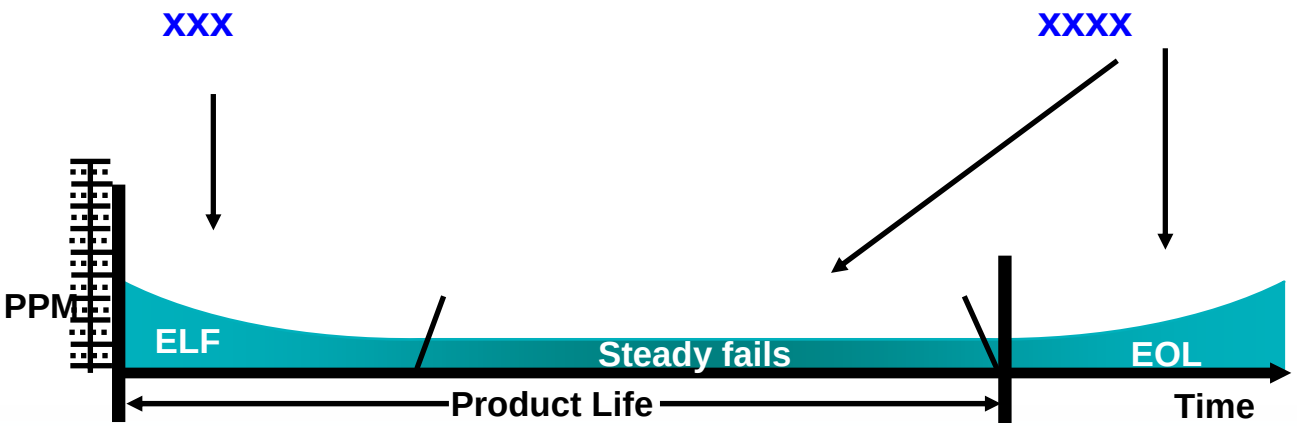
	New Fails	
	Opens	Reliability Fails
Assembly Simulation 3X-IR 220C/260C	3	0
Field Simulation 1200 cycles of 0C to 70C	1	3(+1)*

* 1 additional defect cross section indicates a severe defect but did not fail

LATEST TEST

- Cross Sectional area of the remaining Cu is the critical parameter
- AOI sector not 100% efficient in detecting dishdowns, and all Near Opens
- 60 Latest defects represents 2000 High Complexity 30+ layer boards
- Failure rate after assembly simulation = 1500ppm
- Failure rate at system test/ELF/Field fails = 2000-2500ppm
- More development required for other materials such as ceramic, teflon

High Reliability Products



Reliable Product

Summary:

- **Thoroughly understand defect mechanisms for new products/processes**
- **Continuously validate electrical test parameters to find latent defects**
- **Assessment on Test efficiency by defect type and overall test strategy**
- **Understanding customer objectives**