Electrical Performance of an Organic, Z-interconnect, Flip-Chip Substrate

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Abstract

We have designed test vehicle (TV) using the Z-interconnect building blocks, to make new RF structures. Specifically, large rectangular clearances were cut in multiple ground planes to make a very wide 50-ohm stripline. Also, typical 50-ohm stripline was designed with a ground-signal-ground structure. Each stack-up had 16 metal layers, including 3 0S2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. Two different material sets were used. One was a mixed set of materials, using different materials or the plane-dielectric-plane structure and for the dielectric layers associated with the signal layers. Dielectric 1 has Dk = 3 and tanδ = .003. Dielectric 2 has Dk = 3.2 and tanδ = .003. Resistance change for embedded resistors for different materials set is not significant. Conducting adhesives formulated using silver and Low melting point (LMP) fillers were used to fill small diameter holes for Z-interconnect applications. Laminated conducting joints show low resistance in the range of 10-12 milliohm per square inch. Detailed electrical performances of the TV are under investigations. Electrical performance tests include S-parameter measurements of stripline structures. Very low signal loss to 25GHz will be shown. Evaluation criteria for the test vehicle will include its ability to perform as a reliable, manufacturable, high-performance substrate.

Introduction

More and more substrate designs require signals paths that can handle multi-gigahertz frequencies [1-3]. The challenges for organic substrates, in meeting these electrical requirements, include using high-speed, low-loss materials, manufacturing precise structures and making a reliable finished product. A new substrate technology is presented that addresses these challenges. In order to achieve electrical performance goals in an organic substrate, several requirements must be met:

- via stubs must be eliminated
- lines must be wide enough to reduce signal loss, while still controlling impedance
- interconnects must be tuned to reduce signal loss
- vias must be tuned to reduce signal loss
- substrate must be manufacturable
- substrate must be reliable

Most existing organic substrate technologies have via stubs which can only be avoided with restrictive design rules, and do not have the flexibility to build arbitrary transmission-line structures. Using Z-interconnect substrate technology, all of the requirements can be satisfied [4-7]. Z-interconnect technology involves building mini-substrates of 2 or 3 layers each, then assembling several mini-substrates together to make the finished product. It is used to connect PCB metal layers vertically, using a conductive paste. Designing and manufacturing the mini-substrates separately makes it possible to reliably manufacture substrates with no via stubs, very low-loss materials, nearly arbitrary transmission line structures and a lot of flexibility in tuning features to reduce signal loss.

Many new designs require multi-GHz signals, dense wiring due to high I/O count, and both wide lines for RF signals and narrower lines for digital signals. With standard substrate stack-ups it is difficult to satisfy all those constraints at once [6]. A new Z-interconnect stack-up is developed to solidly satisfy all the constraints.

Currently there are a number of choices for a core plus build-up substrate that satisfy multi-gigabit data rates. [1, 5] The core plus build-up construction allows good performance and wireability in the build-up layers, but at a cost of less flexibility in the core layers. For instance, the core layers typically have a minimum via pitch, must be mostly a copper plane, and cannot have large clearances in them.

Another method of achieving multi-gigabit data links is using Z-interconnect. With the need for Z-interconnect, new materials are being developed to satisfy the electrical and mechanical requirements of the Z-interconnect layer. [4]

In the present investigation, we report new design that uses Z-interconnect building blocks, to make RF structures. The work was involved to optimize dielectric and conducting adhesive materials for the structures. The structure also contains embedded resistors. Overall, this effort is an integrated approach centering on three interrelated fronts: (1) materials optimization; (2) fabrication, and (3) electrical performances at the package level.

Z-interconnect construction

Electrically, in micro-chip packages, there is always a need for substrates that can handle a diverse range of signal types. Focusing resources, such as area on the substrate and expensive materials, where needed maximizes performance versus cost. The fastest RF signals get the widest lines and well-controlled impedance. The slower RF signals have narrower lines. Digital signals are just wide enough to carry their data and are squeezed as close as possible without violating crosstalk specifications. Low frequency interface signals (MHz) are very narrow and fit in around the critical signals. Power and DC nets are put in last. A Z-interconnect stack-up allows the engineer quite a bit of flexibility to place wide signals, narrow signals and grounds and clearances only where needed. The result is sketched below.
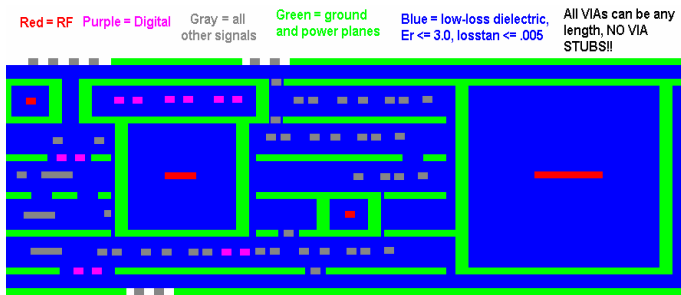
Figure 1 Versatile, Arbitrary stack-up

The way used to build a structure like this is with a series of building blocks called cores. The main building blocks are a plane-plane (0S2P) core and a signal-plane-plane-signal core (2S2P). The 0S2P is called a joining core because it has a conductive paste which allows it to attach to the 2S2P signal cores. The joining core starts with an off-the-shelf laminate with 2 layers of copper attached to a dielectric sheet. Then shapes and lines are etched into the copper on both sides.
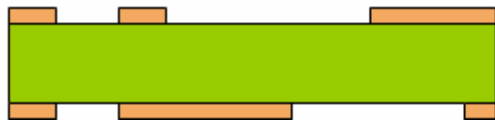
Figure 2 Etch 2P core

Next, a layer of dielectric and copper is stuck to both sides of the etched plane-plane core. Holes are then drilled all the way through the structure.
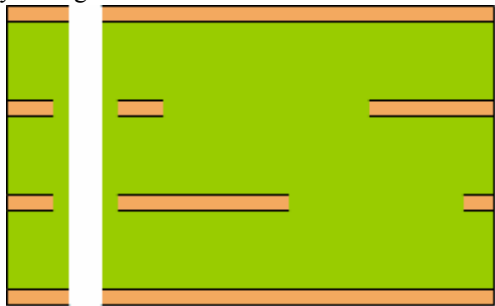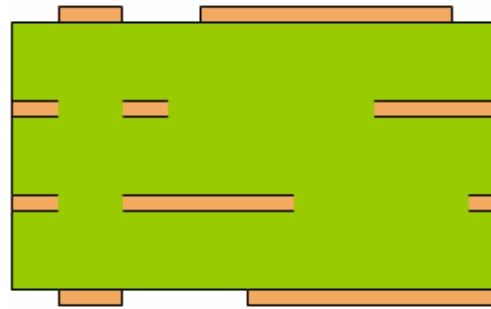

Figure 3 Drill laminated 2P core

Finally, the hole is filled with conductive paste and the outer copper is etched away, yielding a 0S2P joining core.
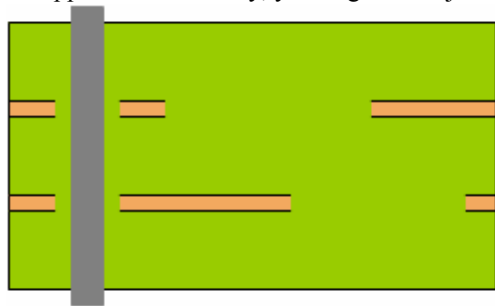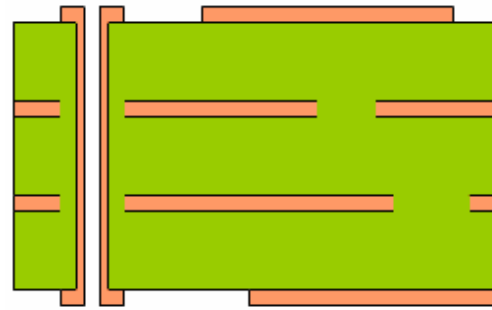

Figure 4 Paste fill drilled 2P core

The 2S2P signal core is processed the same way up to attaching the dielectric and metal layers to the 2P core. As the next step, instead of drilling, the outer copper is etched to create all the signal features.
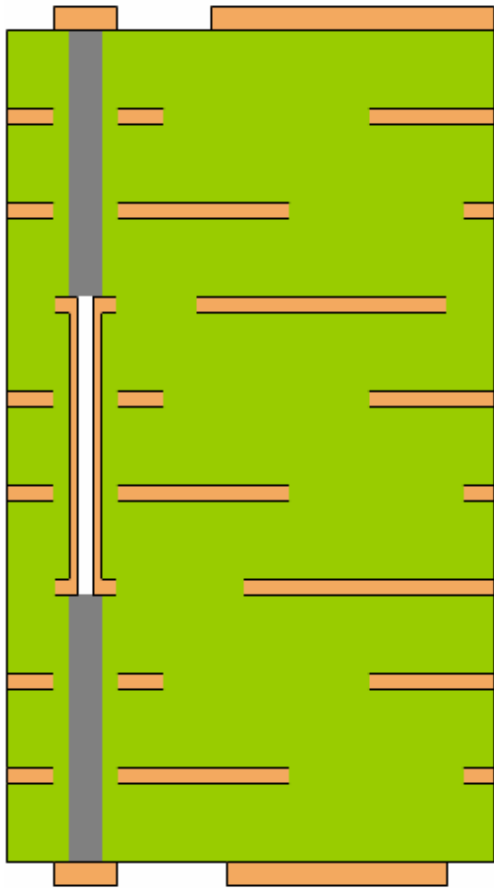

Figure 5 Etch laminated 2P core

Lastly, the holes are drilled and plated to make the 2S2P core.

Figure 6 Drill and plate laminated 2P core

The 0S2P and 2S2P cores are combined to make a Z-interconnect stack-up.

Figure 7 Z-interconnect composite stack-up

These building blocks in combination with blind and buried vias, allow arbitrary via connections starting at any layer and ending at any layer. In the 2P core, vias can be drilled and plated before the additional dielectric layers are added.
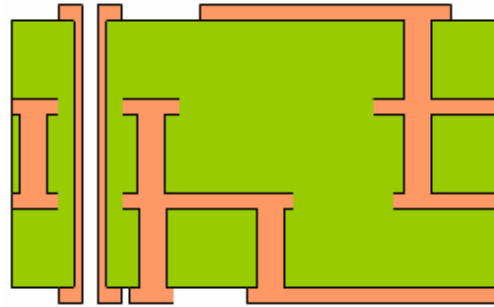

Figure 8 Micro-via 2P core

Blind vias can be drilled on the outer layers of the 2S2P also.
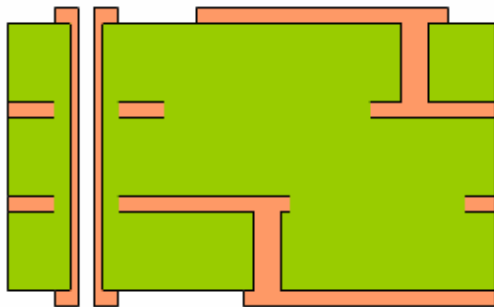
Figure 9 Micro-vias in 2S2P core

These one-layer micro-vias can be stacked to make arbitrary via connections.


Figure 10 Buried and blind vias in core

In addition, embedded capacitance layers can be inserted in any 2P core of the stack-up. Discrete embedded capacitors and resistors can be added to nearly any layer in the stack-up.
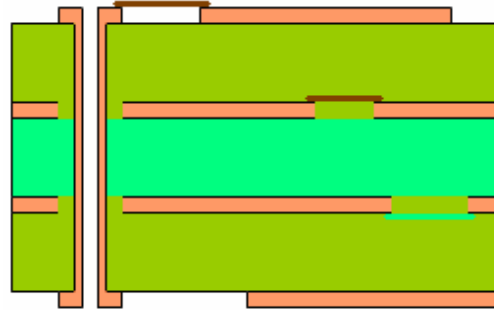

Figure 11 Embedded capacitance layer and embedded discrete caps and resistors in core

Test Vehicle Design

Test vehicles were designed, using the Z-interconnect building blocks, to make new RF structures. Specifically, large rectangular clearances were cut in multiple ground planes to make a very wide 50-ohm stripline. Also, typical 50-ohm stripline was built with a ground-signal-ground structure. Each stack-up had 16 metal layers, including 3 0S2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. Two different material sets were used. One was a mixed set of materials, using different materials or the plane-dielectric-plane structure and for the dielectric layers associated with the signal layers. (**Figure 12**) Dielectric 1 has Dk = 3 and tanδ = .003. Dielectric 2 has Dk = 3.2 and tanδ = .003. This made the manufacturing process a little simpler by customizing the dielectric material to the particular process where it will be used.

Figure 12 Mixed dielectric stack-up
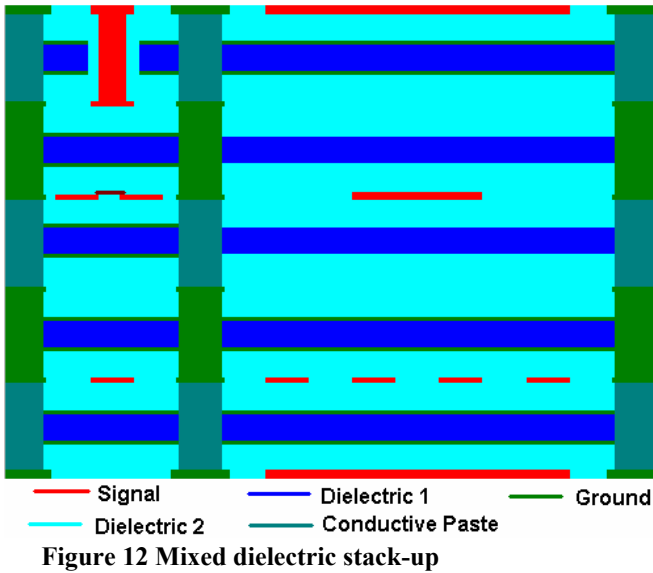
The other material was used throughout the stack-up. This made the electrical performance a little better, at a cost of more complexity in the manufacturing process. Dielectric 3 has Dk = 2.9 and $\tan\delta$ = .0025. **(Figure 13)**
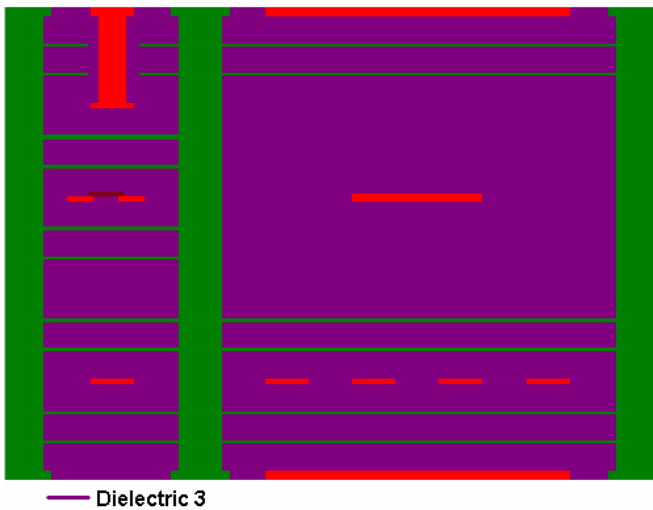

Figure 13 Homogenous Dielectric stack-up

Electrically, this type of stack-up allows a well-controlled, low-loss wide 50-ohm RF line. In the test vehicle the widest line width was roughly 300um, with the smallest about 50um. This new construction allows both transmission lines to fit in a stack-up less than 1mm thick. With the 50um line at 30mm long, the estimated 3dB bandwidth of a link with vias and pads is about 25GHz, and is nearly transparent (-0.5dB) to 2GHz[2]. Using a 300um line instead, the estimated 3dB point extends beyond 50GHz and is nearly transparent to 10GHz.

Composite Lamination

By alternating 2S/2P and 0S/2P cores in the lay-up prior to lamination, the conductive paste electrically connects copper pads on the 2S/2P cores that reside on either side of the 0S/2P core. Two signal layers are added to the composite structure each time one adds an additional 2S/2P core and an additional 0S/2P core. A structure with four signal layers composed of five sub-composites (two 2S/2P cores and three 0S/2P cores) is shown schematically in **Figure 14**. Although this particular construction comprises alternating 2S/2P and 0S/2P cores, it is possible to place multiple 0S/2P cores adjacent to each other in the stack.
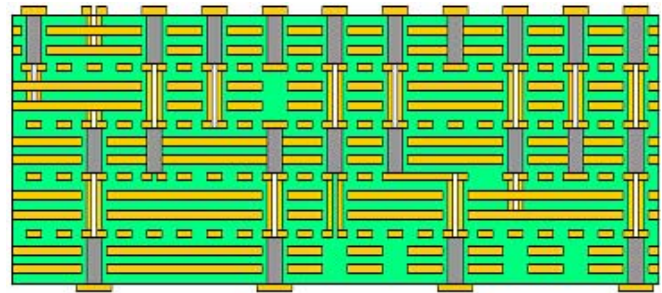

**Figure 14 Sixteen-layer Z-interconnect composite**

Proper preparation of the sub-composites is crucial to obtaining robust, reliable joining between dielectric layers and between the conductive paste and the opposing copper pad. Sufficient flow of the dielectric materials must be achieved during lamination to allow for complete encapsulation of circuitized features and good dielectric-to-dielectric bonding. The photo of a cross section (**Figure 15**) taken from the 0S2P sub-composite prior to hole-fill reveals gaps between holes and registrations
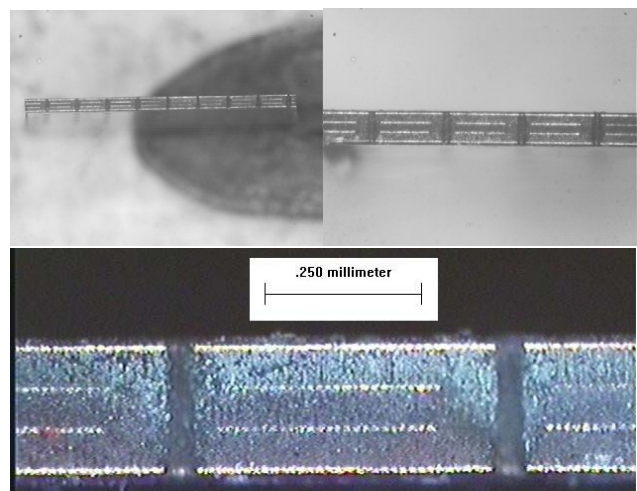
Figure 15 Photograph of cross sectional view of 0S2P joining core taken prior to hole-fill process
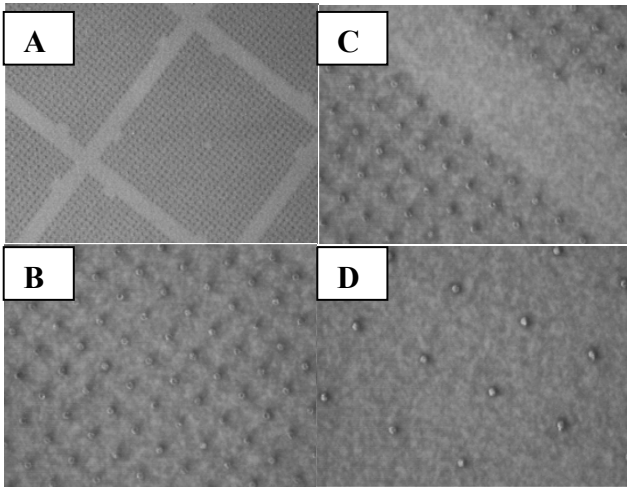
Figure 16 Photographs of adhesive filled joining cores; (A) Large area optical photograph, (B)-(D) higher magnification optical photograph
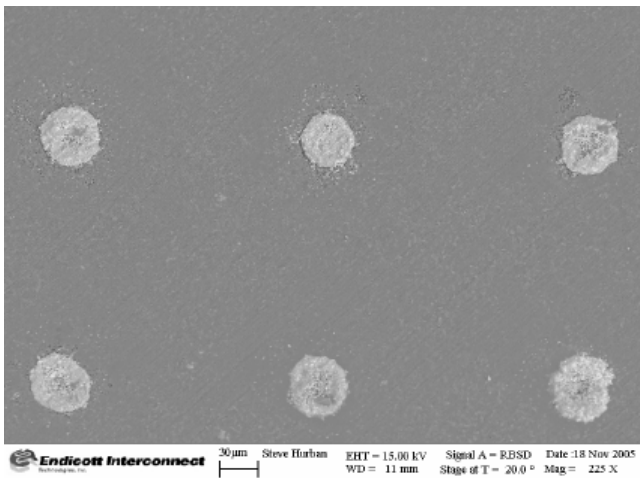
Figure 17 SEM micrographs of laminated adhesive filled joining cores

The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. **Figure 1-4** shows a process flow chart for fabrication of adhesive filled 0S/2P cores. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized sub-composites. **Figure 16** shows optical photographs taken prior to composite lamination, of a joining core having paste-filled holes with a diameter of 55-75 μm. It can be seen that the conductive adhesive height is higher than that of the surrounding dielectric. This excess height helps to produce robust conductive joint between two 2S/2P cores during lamination process. **Figure 17** shows SEM photographs (top view) of adhesive filled joining core taken after composite lamination. These conductive adhesives were typically used to connect C4 of substrate. A variety of silver, and low melting point (LMP) filler based conducting adhesives were used in the joining core to achieve uniform, highly conducting joint. In a typical procedure, epoxy-based conductive adhesives were prepared by mixing appropriate amounts of the

conducting filler powders and epoxy resin in an organic solvent. Conducting adhesives when laminated at ~200°C showed very low resistance. **Figure 18** shows photographs of laminated conducting joint taken from bulk of the materials. **Figure 18A** represents silver-based and **Figure 18B** represent LMP-based conducting adhesives. Both conducting adhesives show very low resistance in the range of 10-12 milliohm per square inch area. Preliminary photographs of a composite laminate structure are shown in cross section in **Figure 19**. It can be seen that both mixed or single dielectric materials can fill large cut outs. It is also possible to make substrate with embedded resistors. **Table 1** shows various embedded resistors value with mixed dielectrics and single. Each row represents similar size embedded resistors.
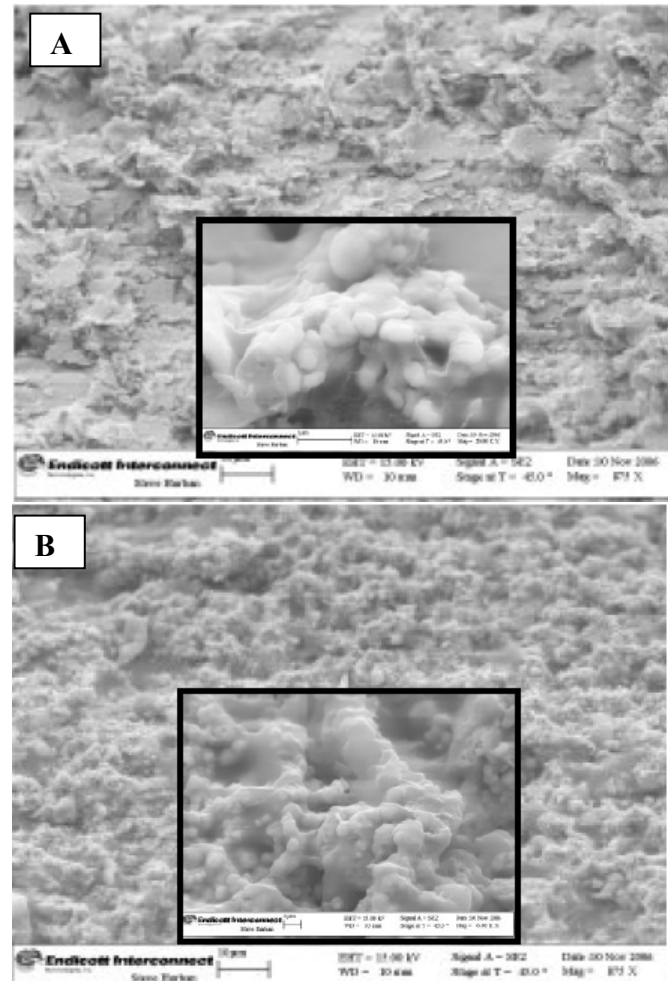
Figure 18 SEM photographs of conducting adhesives (A) silver based, and (B) LMP based system

Mixed Dielectric Resistance (Ω)	Single Dielectric Resistance (Ω)
11.08	11.11
10.52	10.42
9.41	9.43
11.21	10.71
13.04	12.48
12.27	12.53
12.14	12.31
12.93	12.26

Table 1: Embedded resistors with different dielectrics
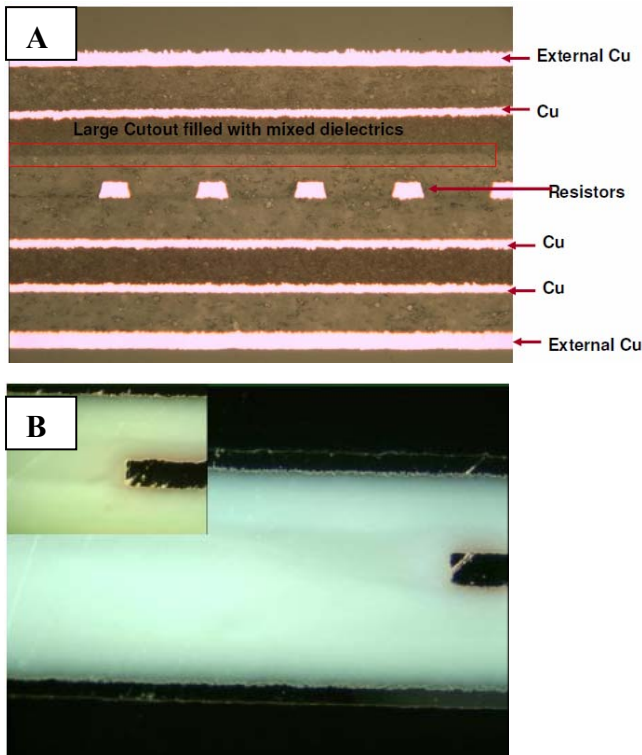
Figure 19 (A) Photograph of 0S2P and 2S2P composites with mixed dielectrics (Dk = 3 and tanδ = .003; Dk = 3.2 and tanδ = .003) and embedded resistors, and (B) Photographs of single dielectric (Dk = 2.9 and tanδ = .0025)

Conclusions

A Z-interconnect substrate, with large clearances in planes and embedded resistors, can be built with sufficient flatness on subsequent metal layers. Using 0S2P and 2S2P building blocks, a nearly arbitrary stack-up of signals and planes can be built. This allows very low-loss 50-ohm stripline to be built by making nearly 300um-wide lines and clearing out ground planes to make a 50-ohm structure. This also allows narrower 50-ohm lines and narrow digital lines and DC structures to be built on the same layers as the wide lines. A high-performance, mixed signal design can be built in a substrate less than 1mm thick. It is also mechanically robust and reliable. In addition, the electrical performance is outstanding, since the wide lines are nearly transparent to signals up to 10GHz. Measurements are continuing and more data will be available at the conference presentation.

References
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