Considerations for High Speed PCB Track Design in 10Gb/s Serial Data Transmission

White Paper

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Abstract

A fundamental evaluation of a variety of approaches for designing a high-speed (10 Gb/s) serial differential electrical channel is examined. The application of the electrical interface has been simulated using HSpice software. It demonstrated how the signal quality could be affected by the use of microstrip versus stripline traces and their associated advantages and disadvantages is discussed. Example XFI channels were assembled from the simulation results to demonstrate viability of the application.

Introduction

This white paper describes the main considerations in the design of a PCB for the transmission of 10 Gb/s serial data. It has been written to aid the PCB designer to devise the layout for a host board for use with the Avago 10 Gb/s HFCT-711XPD XFP LC differential serial transceiver and the electrical channel to the SerDes IC (XFI channel). Its focus is on the frequency-dependent attributes of the various components within the electrical channel. Additionally, the parametric issues of a pluggable connector are examined.

The XFI Electrical Channel

A block diagram of a typical electrical channel is shown in Figure 1. This is a simplified electrical channel within an XFP application. The electrical characteristics of the data are assumed to be XFI compliant, see the XFP MSA (www.xfpmsa.org) for further details on an XFI interface. The numbers in Table 1 relate to the position within the channel:

Table 1. XFI data channel details

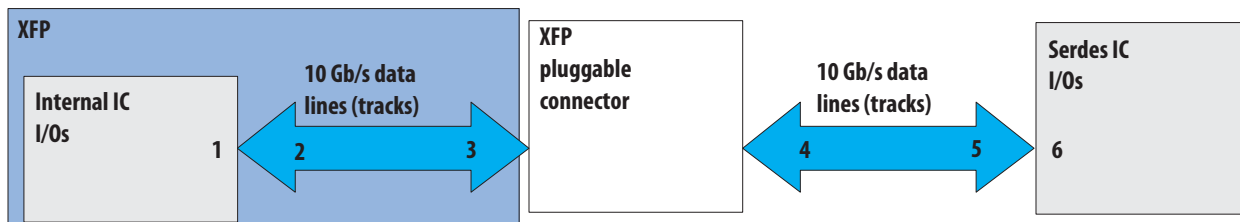| Number	Location
1 - 2	Channel from the IC pads to the IC I/O pins
2 - 3	10Gb/s data channel including vias
3 - 4	Channel through the pluggable connector
4 - 5	10Gb/s data channel including vias
5 - 6	Channel from the IC I/O pins to the IC pads

Figure 1. Block diagram of an electrical XFI channel

Within the XFP MSA is an option to utilize eye opener ICs. This enables a reduction in the amount of jitter on the signal in both directions of the XFI channel. However, the interest here is in the degradation of signal quality due to the channel, ie. practical tests are necessary for an absolute evaluation of the channel. Where measured data is not yet available, the parametric values for components and parasitics within the XFI channel have been estimated.

There are many factors affecting the signal integrity of high-speed data links: -

1. Track dimensions

2. Dielectric material properties of the PCB

3. The physical design of the pluggable connector (effects of implementation)

4. Discontinuities between the track and component pads (reflections)

5. Type and length of track used, microstrip / strip line

6. Physical configuration of vias

7. Data pattern-dependency of the signal quality – jitter

8. Temperature dependency

Here, we will examine each one in turn and analyze the associated effects on the transmitted digital data stream.

Track Length/Width and PCB Materials

Track dimensions together with PCB material properties become more prohibitive with increasing frequency. The dielectric constant, er, of the PCB material dictates the effective capacitance around the transmission lines and is frequency dependent. Additionally, the velocity of an electromagnetic wave that travels through a dielectric is reduced proportionally to the square root of the dielectric constant er, ie. for a given EM wave, as er increases, the velocity decreases. Furthermore, as the frequency of the EM wave increases, the effective er of many dielectrics used for the manufacture of PCBs decreases. *The group velocity of an electrical signal therefore depends on its frequency, an effect known as dispersion.* However, this effect is usually small and will be ignored for the purposes of this study. The dielectric material of a PCB is generally composed of glass fiber and resin. The er is affected by the ratio of glass to resin used to make the laminate. The most common dielectric material used in high-speed data transmission is FR4. This material has a low er with a typical resin/glass ratio of around 55%. At 5 GHz, er is about 4.2 [Ritchey 1999].

The losses of transmission lines are determined by the skin effect of the conductor and the absorption of electric energy by the dielectric. The skin effect confines the current flow to the surface of the conducting material, typically copper. Increasing the surface area, ie. by increasing the width of the transmission line, can mitigate the skin effect. The loss of electric energy in the dielectric is described by its loss tangent tan(d). In most digital applications up to about 1 GHz the dielectric loss is a small fraction of the loss due to the skin effect. However, since dielectric losses increase faster with frequency than skin-effect losses, they can become the dominating loss mechanism for very high data rate systems.

When transmitting at frequencies of around 5 GHz or higher, the combination of trace dimension and PCB material is paramount in finding the right trade-off between low channel-loss, ie. low attenuation to maintain signal levels well above digital decision thresholds, and minimizing jitter or standing wave effects through the right amount of attenuation of unwanted reflections. For a shorter trace length at 5 GHz, the use of a lossy combination in order to introduce a small amount of additional attenuation may actually help to improve the overall XFI channel return loss.

Pluggable Connectors

When using a pluggable connector, it is essential that the physical properties of the connector do not limit its use in the intended data channel. The electrical parasitics of the connector, eg. inductance, have to be included during the evaluation. The parasitic values are usually available from the manufacturer of the connector and enable the use of electrical simulation for Signal Integrity evaluation of the data channel.

PCB Layout Design and Microstrip versus Stripline Geometry

A Time Domain Reflectometer can be used to evaluate discontinuities in the data track. It is critical to avoid reflections when transmitting data to ensure that only a clean signal with well defined edges and voltage levels is received. In the case of a short track length in an XFI channel transmitting at around 5 GHz, it maybe an advantage to use a PCB material that has a higher loss tangent tan (d) to help absorb reflections and hence improve signal quality[1]. Furthermore, the type of track used, stripline or microstrip, has both advantages and disadvantages for high-speed data transmission. See Table 2.

Table 2. Microstrip versus Stripline

	Advantages	Disadvantages
Stripline	Buried track avoids surface EMI emission and improves EMI immunity.	Vias have to be used: 1) Can lead to reduced signal quality by causing reflections. 2) Can limit the track length due to narrow track width and increased dielectric losses.
Microstrip	Longer track lengths permitted; does not require vias so fewer impedance discontinuities that can impact Signal Integrity - more predictable.	Can lead to an EMI emission and immunity penalty for the channel both for the transmitting device and surrounding components - open-air emissions.

Note:
1. Reference: XFP Multisource Agreement Rev 1.0

The Use of Vias in High-Speed Data Transmission

The introduction of vias in to a high-speed electrical design can lead to multiple electrical reflections caused by impedance discontinuities in the data line. Additionally, the manufacturing process can be troublesome at frequencies >1 GHz to achieve the required signal quality. Other considerations are: simplifying electrical designs and optimizing signal integrity.

Data Pattern-Dependency of the Signal Quality – Jitter

The frequency content of the test pattern and the 'typical' live traffic will determine how the signal is affected by the format of the data. The Synchronous Optical Network, SONET, data format typically has more content at lower frequencies than an Ethernet pattern, normalized to remove the bit rate difference. This is due to long strings of Ones and Zeroes that are allowed in the SONET format. Thus the range of frequencies that the PCB has to handle is relatively different for each of the network protocols. This can have a significant affect on the signal quality due to resonance effects and the overall frequency dependence of the data channel. It can therefore be important to check that a data channel not only works at the highest frequencies, but also does not cut off any low frequency content that could be present in SONET protocols for example.

Note: The simulations within this document have utilized the PRBS 2^7-1 data stream.

N.B. It is probable that a pattern with a lower frequency content, e.g. PRBS 2^{23}-1 would display worse results, however using this pattern would result in a much longer simulation time due to the required resolution of the waveforms, thus longer patterns were not used in the simulations.

Temperature dependency

It is clear that materials used in the manufacture of PCBs can have differing coefficients of thermal expansion. However, the temperature range of a typical data application does not usually exceed the –40 to +85 °C limits. Over this temperature range the relative dimensional change of the PCB materials is less than 1%, and in the case of differential tracks, both tracks should be affected by the same amount. Such a small change in length of the traces should be insignificant in terms of the Signal Integrity of the XFI data channel. Similarly, for track width, the proportional change is of the same amount as the length change with temperature. Again, this is very minor with regards to the practical limits that apply to track width control in a typical manufacturing environment.

Vias may experience stress caused by the expanding dielectric, due to differences in the thermal expansion coefficients of copper and FR4. This can threaten the mechanical integrity of the PCB and could lead to cracks in the vias for very thick PCBs, which may in turn manifest itself as intermittent failure [Ritchey 1999]. The most critical process step in that respect is soldering operations, which raise the temperature of the PCB to around +185°C. However, unless cracks occur during the manufacturing operations of the PCB temperature changes are not expected to affect the high-frequency properties of the XFI data channel. Hence temperature dependence will not be further discussed.

XFI Channel Simulation

The XFI channel has been simulated to show how the various properties, discussed above, can influence the signal shape and quality. In this section, the XFI channel is separated into component models. The simulation tools used were Agilent Advance Design System v.2002 and Synopsis (formerly Avanti) HSpice v.2002.2.1. The schematic in Figure 2 demonstrates how the receiver section of a XFP module was modeled to enable the simulation of an XFI compliant channel. The significance of the various elements of this XFP receiver model will be discussed in some detail before we look at simulation results for a whole XFI data channel. Additional detail of the output buffer model of the XFP receiver is shown in Figure 3. As can be seen from the schematic a Current-Mode Logic (CML) buffer model has been devised in order to meet the I/O buffer specifications of the XFP MSA. The following table explains the various elements of the output buffer model shown in Figure 3:

1. Differential digital signal generator

2. 6th order Bessel filter to generate realistic analog edges and eye shapes[1]

3. Fine-tuning network to slow the final settling of the buffer, if required. The RC time constant used here is 4 ps.

4. Fast open-collector transistors with 50 ohm internal pull-up resistors – intrinsic switching speed approximately 10-15 ps. The current source in the "tail" determines the signal amplitude.

5. Capacitance of the die bond-pads and other parasitic capacitances. The capacitance used in this model is 0.1 pF.

Note:
1. Reference: "The Art of Electronics" (Second Edition) by Paul Horowitz and Winfield Hill, Cambridge University Press, Chapter 5 "Active Filters and Oscillators".
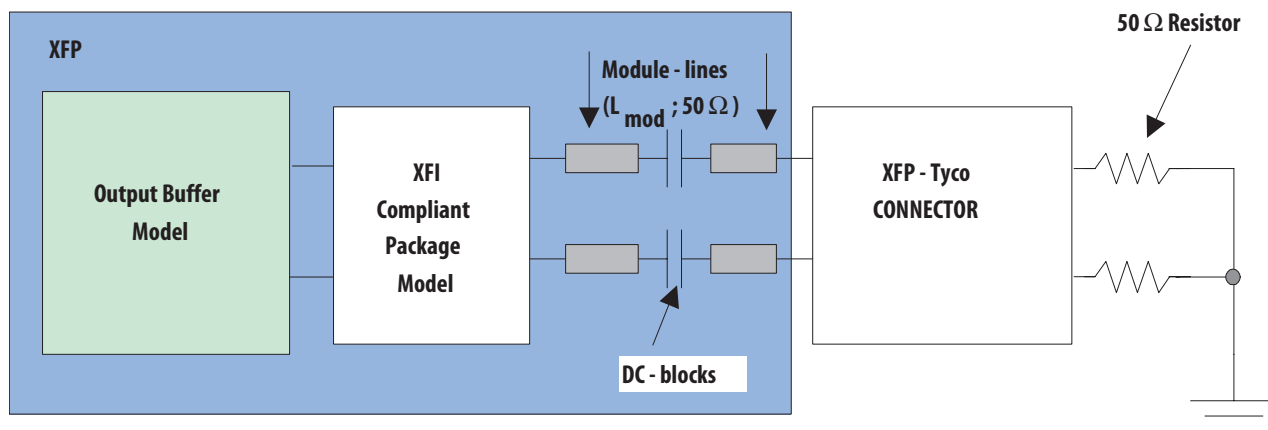

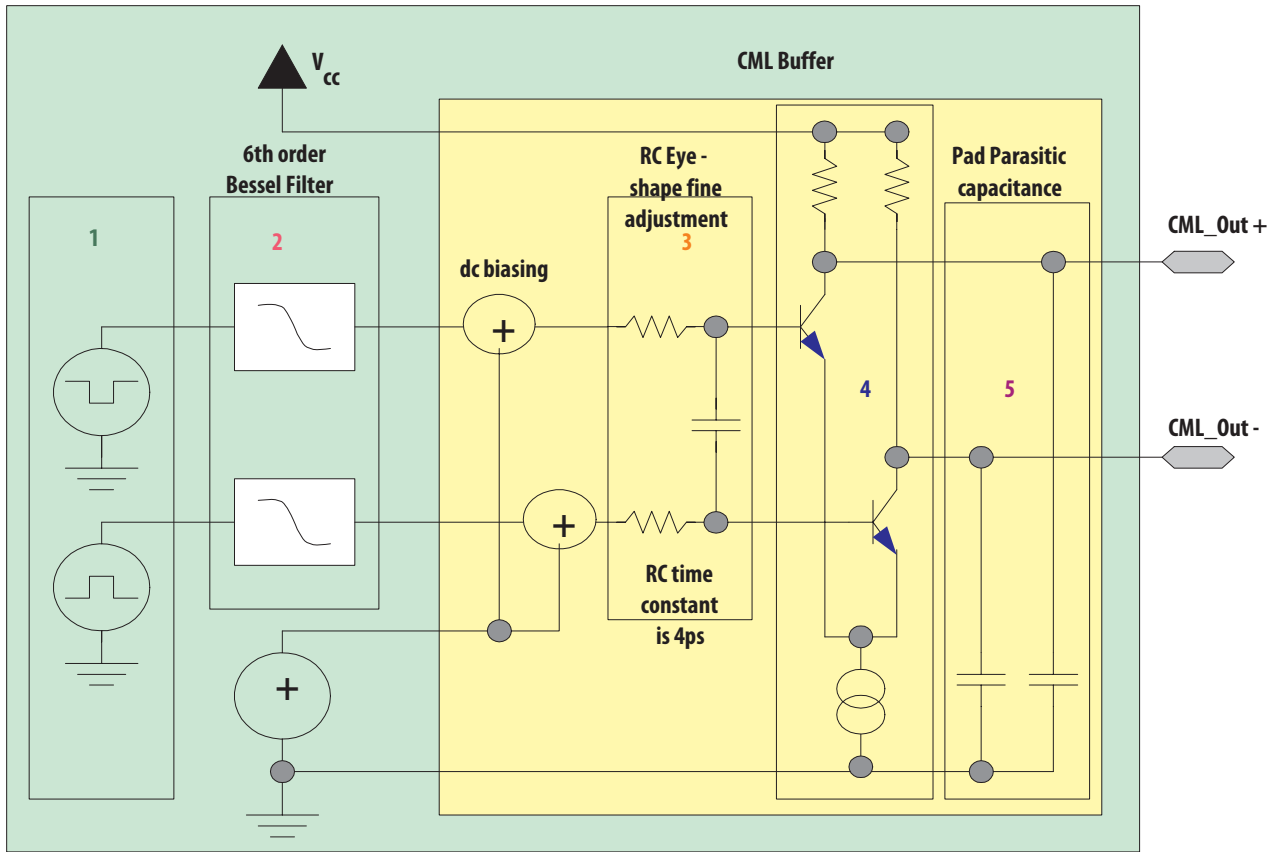**Figure 2. XFI channel model components**

Figure 3. Schematic of the quantizer CML output buffer created for XFI simulation

XFP Model Components

From the die pads the signal needs to pass through the IC package before it is launched onto the transmission lines inside the XFP module. Figure 4 shows the Scattering (S) parameters S11 and S12 of the preliminary quantizer IC package model that was used to account for package-induced parasitics between the Silicon die and the quantizer SMT pin[1]. At this point it shall suffice to say that the package model is compliant with performance requirements of an XFI data channel. The preliminary model used here is based on an RLC-"ladder" approach that is explained in more detail later in this white paper when we will look at the influence of the receiver IC package on the Signal Integrity of a XFI channel link.

A surface mounted dc-block allows the decoupling of the XFP module supply voltage from the voltages used by the Serializer/Deserializer (SerDes) IC on the host board. Figure 5 shows a schematic of the equivalent circuit for the parasitics of the 47 nF dc blocking capacitors that was used in the simulations.

Note:
1.   SMT: Surface Mount Technology

A Spice model of the pluggable connector, supplied by *Tyco Electronics*, was also inserted into the XFI channel model. The pins corresponding to the RD+/- signals were terminated with two 50 Ω resistors as depicted in Figure 2.

All other connector pins were grounded. A simulation was run where the XFP receiver model was stimulated with a 10 Gb/s PRBS (2^7-1) bit pattern. The differential waveforms were probed between pins RD+ and RD- of the XFP module connector (host side), the resultant eye-plot is displayed in Figure 6.

Due to the complexity of the XFP connector model, simulation times tend to be long. A compact version of the model was therefore constructed in order to save processing time. The compact model is an equivalent single-line model that ignores the coupling between the pins and consequently cannot be used for connector-induced crosstalk analysis, however, it accurately describes the impedance discontinuity caused by the connector. The simulated Time-Domain Reflectometry (TDR) responses of the two connector models are shown in Figure 7. The agreement between the 2 models is satisfactory. This is also confirmed by XFI channel simulations where the resultant eye-plot together with the XFI compliant eye mask[1] is shown in Figure 8. It can be seen that the eye-plot with the compact model is very comparable with the plot using the full connector model. All subsequent simulations used the compact connector model unless otherwise stated. Furthermore, the eye diagram in Figure 8 will serve as a reference for quantitative evaluations of eye closure as a function of XFI link design parameters.

The frequency content of the simulation pattern is shown in Figure 9. This is the Fourier transform of the PRBS (2^7-1) pattern emitted by the XFP receiver. It can be seen from this plot that frequencies above 20 GHz contribute little to the output signal produced by the receiver model. As mentioned earlier, for some data formats it can be as important to check the low frequency end of the spectrum, as it is to verify performance at the high frequency end. For the SONET data format, strings of consecutive ones and zeroes as long as 72 bits are allowed. The lowest frequency which then needs to pass the channel can be estimated according to f_low = BitRate/(2*N), where N is the maximum number of identical bits. Thus, for an OC-192 SONET data pattern, this equates to approximately 69 MHz. The low frequency cutoff of the XFI channel needs to be well below the 69 MHz in order for the link to be usable for SONET data formats. However, even for small values of the cutoff frequency, there is still an influence on Data-Dependent Jitter (DDJ) and eye-closure. The effect is most pronounced for long sequences of ones and zeroes. The R&D department of Avago has estimated the DDJ and the reduction of the inner eye height for the maximum allowed sequence of 72 identical bits. The results of these worst case calculations are depicted in Figure 10 as a function of cutoff frequency for a 10 Gb/s SONET data pattern.

Note:
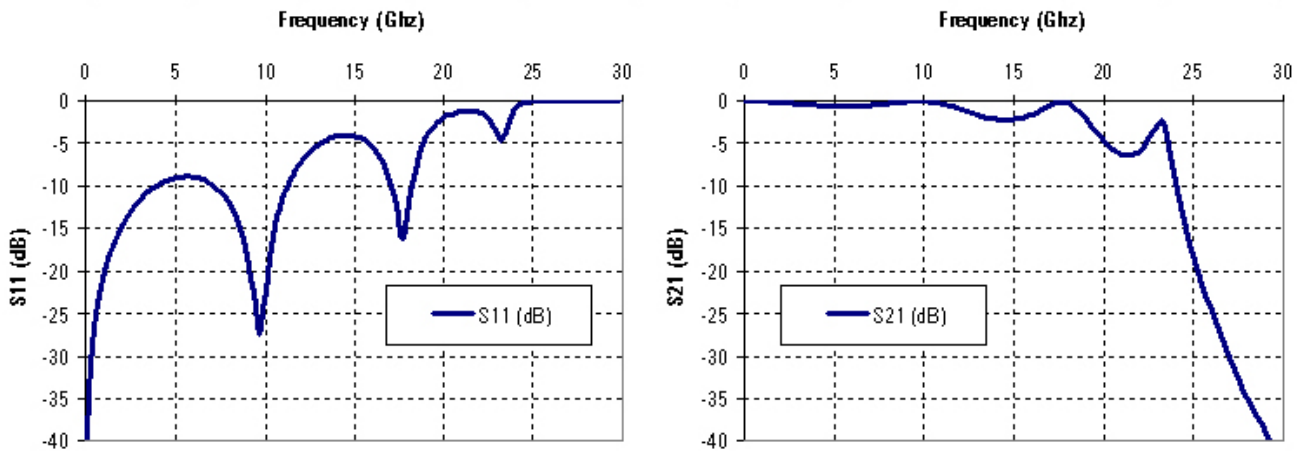1. Reference: XFP Multisource Agreement, www.XFPMSA.org.

Figure 4. S11 and S21 plot of the quantizer IC package model. The model is based on an RLC "ladder" approach, which is explained in a later chapter of this white paper.
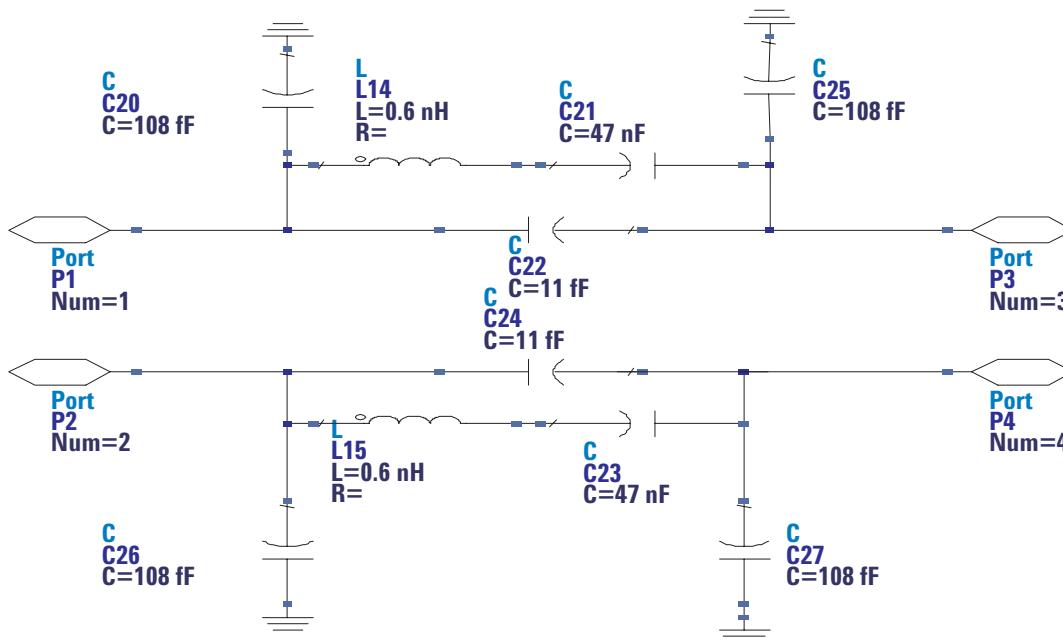

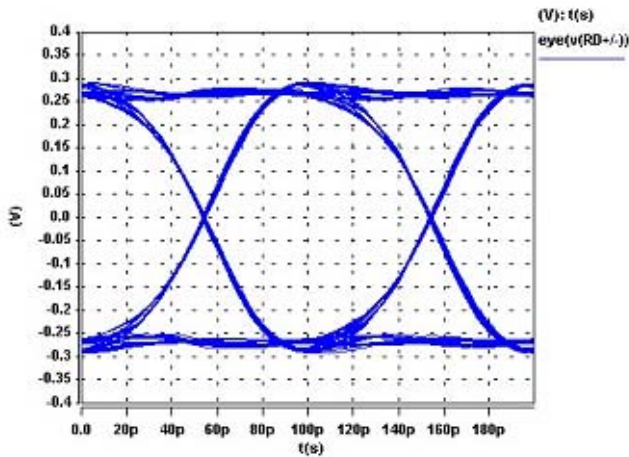Figure 5. Schematic of the parasitics for the dc blocking capacitors

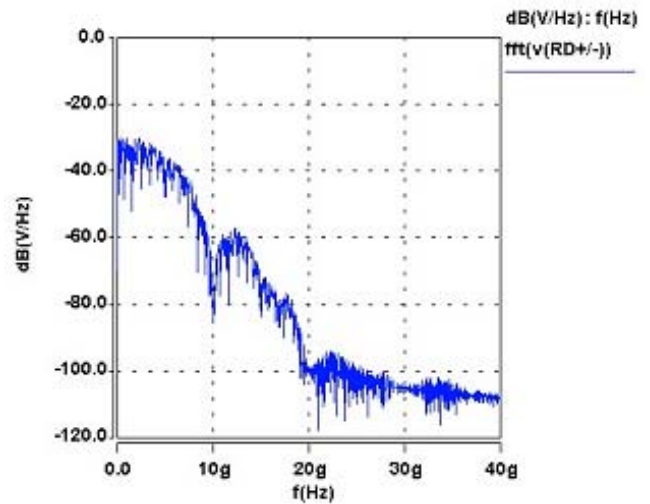**Figure 6. XFI channel simulation using the full connector model**

Figure 7. TDR simulations of the full Spice connector model and the compact model.

Figure 8. Simulation plot using compact connector model incorporating the XFI compliance eye mask

Figure 9. Frequency content of the 2^7-1 PRBS bit stream emitted by the XFP receiver

Figure 10. Effect of the low-frequency cut-off on DDJ and inner eye height.

Eye Measurements

In the following we will focus on the highfrequency aspects of XFI channel design. After having developed a suitable base model, simulations were carried out to map out the design space. In order to quantify the impact on the electrical eye from varying several of the parameters described earlier, measurements were taken from eye-plots of transient simulation runs. These are compared to the reference eye-plot in Figure 8. The eye-diagram in Figure 11 shows how the measurements were taken.
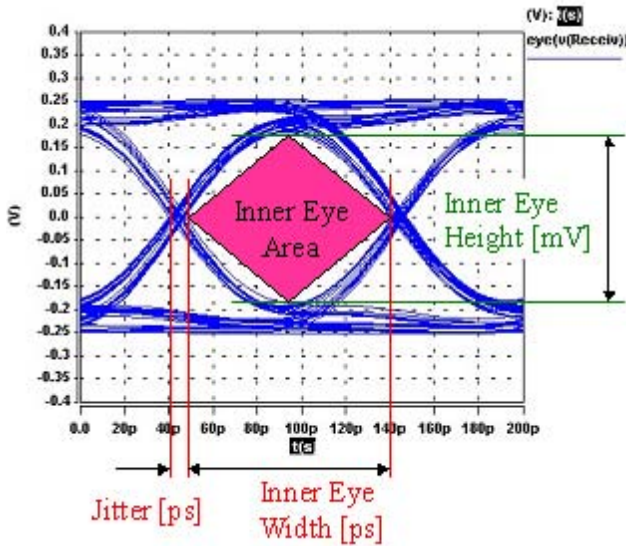

Figure 11. Simulated electrical eye plot showing measurement parameters

Simulations with Microstrip Tracks

In a first analysis we will look at the effect of track dimensions and dielectric loss on the propagation of a 10 Gbit/s signal on microstrip transmission lines. The configuration adopted for the simulations is shown in Figure 12. The electrical signal is emitted by the XFP *optical* receiver (which acts as an *electrical* transmitter), and travels through the XFP connector and along the interconnect structure on the host PCB to the resistor that provides 100 Ω differential termination. The signal is probed across the termination resistor as indicated by the red arrows in Figure 12.
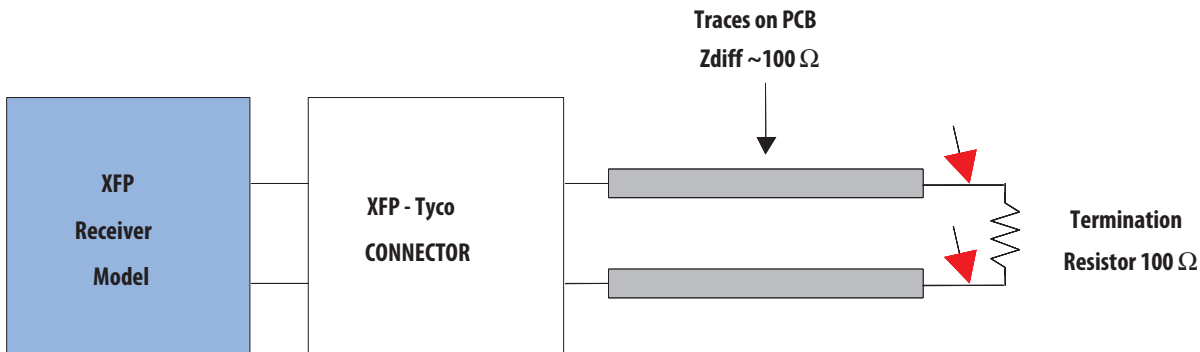
This simulation setup is a somewhat "idealized" arrangement which neglects the frequency dependant characteristics of the IC package of a real-world SerDes or Eye Opener IC, and the finite, albeit small, input buffer capacitance of the die. However, this approach will allow us to analyze the influence of the trace parameters on the XFI data channel in an unambigiuous manner. In a later chapter we will replace the termination resistor with a more realistic electrical receiver model.

For the board-level interconnect, loosely coupled microstrip traces were used with a differential impedance of 100 Ω. Three combinations of trackwidth and dielectric were simulated for 4, 8, and 12 inches track length each. The details of the configurations together with the results of the eye diagram analysis are listed in Table 3. Please note that for both epoxy laminates the same dielectric constant was employed to enable the use of identical trace geometries. The dielectric constant reduces with frequency and differs somewhat for the two laminates, the figure used here is at the higher end of the range of reported values.

It can be seen from the plots below in Figure 13 that the expected eye closure and increased data dependent, i.e. deterministic jitter is evident due to the increase in track length. Both '0' and '1' transitions split into multiple traces and the central area is severely reduced. The central eye mask shown in Figure 13 is based on the "XFI ASIC/SerDes Receiver Input compliance mask"[1] and is for relative comparison only. Please note that 12 inches track length is the maximum recommended in the XFP multi source agreement.

The results listed in Table 3 are plotted in Figure 14 to illustrate the increased deterministic jitter and the reduced eye opening as a function of the chosen microstrip geometry and dielectric material. It is evident that simulation 1 produces the largest losses, which are attributed to the skin- resistance of the relatively narrow, only 5 mil wide track. Widening the tracks to 12 mil considerably reduces the skin effect induced losses as can be seen in the data for Simulation 2. For both of these simulations, a lossier (and therefore cheaper) laminate with a loss tangent of 0.025 was used. To increase eye margin further one can

Figure 12. Building blocks for XFI data link simulation. The red arrows indicate where the signal is probed.

use lower loss laminates as per Simulation 3. However, the improvement is small except for very long interconnect lengths exceeding about 6 inches length. For traces shorter than 6 inches standard, i.e. higher loss laminates should be sufficient to meet the XFI channel requirements.
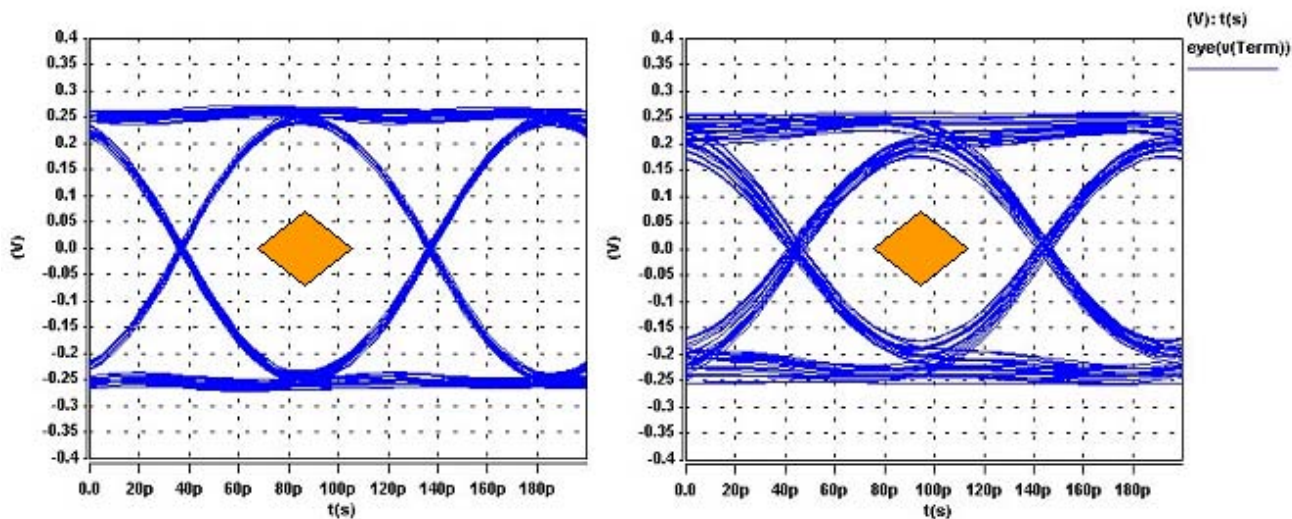

Figure 13. Comparison of eye plots from 4in (left) to 12in (right) track length for simulation 2.

Table 3. Simulation parameters and results for microstrip interconnects.

| Simulation Configuration	Inner Eye Height [mV]	Deterministic Jitter [ps]	Inner Eye Width [ps]	Inner Area [ps*mV]
XFP Reference Eye	508.0	1.9	98.1	24917.4
Simulation 1 : N4000-6 (er=4.1, loss tangent 0.025, 2.8 mil thick), 5 mil wide microstrip, 100 mil track spacing, 0.5 oz copper				
4 in track length	428.1	4.1	95.9	20527.4
8 in track length	337.3	7.8	92.3	15558.0
12 in track length	262.1	12.8	87.2	11427.6
Simulation 2 : N4000-6 (er=4.1, loss tangent 0.025, 6.6 mil thick), 12 mil wide microstrip, 100 mil track spacing, 1 oz copper				
4 in track length	464.0	3.2	96.8	22457.6
8 in track length	401.6	5.1	94.9	19055.9
12 in track length	347.3	7.4	92.7	16088.7
Simulation 3 : N4000-13 (er=4.1, loss tangent 0.016, 6.6 mil thick), 12 mil wide microstrip, 100 mil track spacing, 1 oz copper				
4 in track length	483.4	2.9	97.1	23469.1
8 in track length	426.6	4.3	95.7	20412.8
12 in track length	379.7	6.0	94.0	17845.9
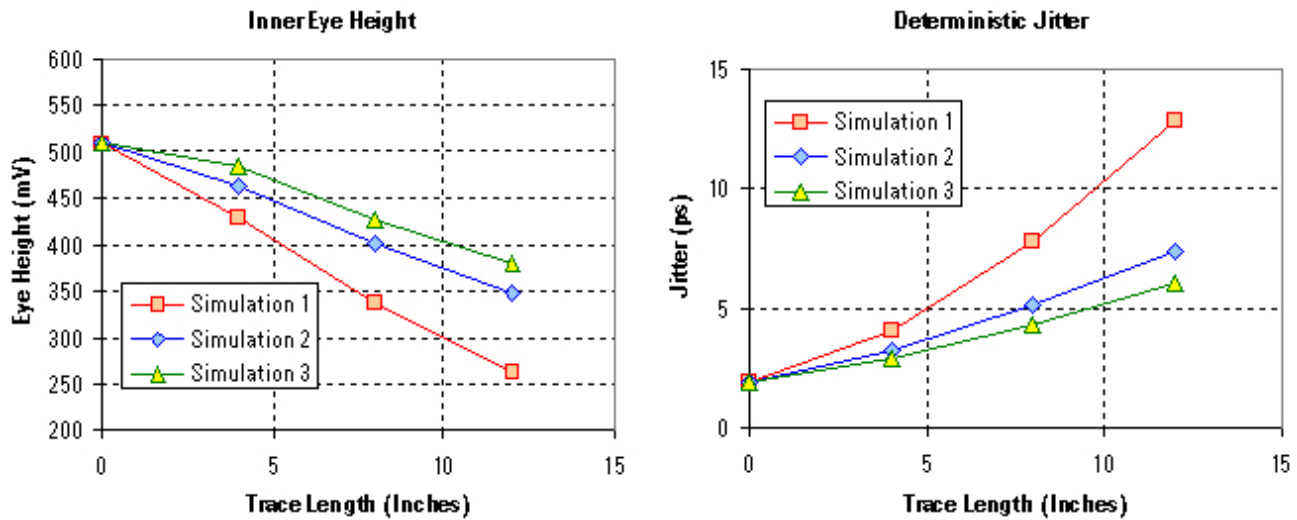
Figure 14. Selected eye diagram parameters for microstrip interconnect XFI link configurations

Simulations with Stripline Tracks

Stripline trace geometries are sandwiched between two reference planes, which can simultaneously act as Power and Ground planes. The various conductive layers are typically separated by about 6 mil thick dielectric layers. This implies that the stripline width needs to be fairly narrow, of the order of 5 mils, in order to meet 100 Ω differential impedance design targets. It is therefore assumed that skin-effect losses will play a significant role, even though the whole surface of the striplines conducts current, in contrast to microstrip traces where most of the current flows on the surface opposite to the reference plane [Hall 2000]. Wider tracks to reduce the skin-effect induced resistance at high frequencies would require thicker layers of dielectric material, however, this may not be feasible as the overall thickness of the stack up may exceed practical limits. Thicker boards may also require thicker vias, which can have adverse effects on routing density and lead to pronounced impedance discontinuities.

Another disadvantage of striplines is the need to contact them with vias. The choice of via design can have a significant impact on signal integrity and the performance of the whole XFI channel. The XFI MSA offers some guidelines for the design of vias, differentiating between single-ended and differential vias, as well as analyzing the effect of open-circuit stub length on the via return loss (S11).

The high-frequency properties of vias (e.g. described by S11, S21 parameters) depend on the geometric parameters of the via (drilled hole diameter, length of via, clearance diameter, etc.), as well as the stack-up configuration and the precise location of Ground and Power planes. In addition, back drilling can be used to reduce the stub-length of the via for improved high-frequency performance. However, a full investigation of the influence of these parameters on the XFI data channel is neither possible nor within the scope of this white paper. Thus, an equivalent circuit was developed for single-ended vias that produced a similar response to the S11 plot shown in the XFP MSA (Figure 60 in XFP MSA revision 1.0), allowing the appropriate simulation of the impedance discontinuity introduced by the via. The equivalent circuit of the employed via model is shown in Figure 15. Some manufacturing variability has been incorporated into the model by using slightly varying capacitance and inductance values. The resultant graph of the via's return loss is depicted in Figure 16. Similar to the via simulation shown in Figure 60 of the XFP MSA (revision 1.0), the model produces a dominant resonance peak at around 17 GHz.

The via model was subsequently inserted into the XFI data channel at either end of host board stripline interconnect. This allows the signal to flow from the XFP connector to the stripline and back from the stripline to the SMT termination resistor.
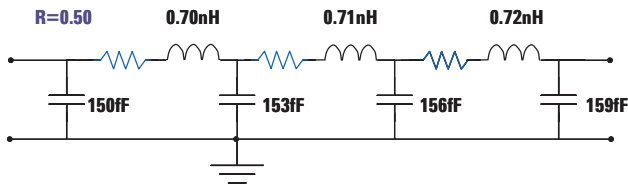
R=0.50 0.70nH 0.71nH 0.72nH

150fF 153fF 156fF 159fF

Figure 15. Via equivalent circuit.

Figure 16. S11 return loss of via equivalent circuit

Two sets of simulations were performed, one using a standard laminate and another for a lower loss dielectric having loss tangents of 0.025 and 0.016, respectively. For both simulations, the striplines were 5 mil wide and sandwiched between reference planes that were 12.2 mil apart. The tracks were weakly edge-coupled with 50 mil spacing.

The simulation parameters and results are summarized in Table 4, two selected parameters are plotted in Figure 17. As expected, due to the relatively narrow linewidth the skin effect induced losses lead to a pronounced reduction in eye opening caused, predominantly by a greatly reduced inner eye height. In fact, the XFP MSA only recommends stripline lengths up to a maximum of 6 inches for standard FR-4. The use of a lower loss dielectric, however, can lead to a noticeable improvement in eye opening. This is attributed to the fact that dielectric losses are proportionately larger for stripline than for microstrip geometries, since the electric field is fully contained in the dielectric in a stripline configuration. Lower loss dielectrics can therefore be used to exceed recommended stripline lengths to greater than 6 inches. A related discussion of the relative importance of skin-effect and dielectric losses can also be found in [Johnson 2002].

It is also worth noting that the inner eye opening (inner eye height, Figure 17) is reduced even for "zero" inches of trace length due to the presence of the two vias. In the particular case considered here the two vias lead to a reduction of the eye opening by approximately 10%. Careful via design or the use of differential vias can be employed to minimize this loss.

Another effect of using vias is an increased level of data-dependent jitter, DDJ. For short trace lengths the deterministic jitter oscillates with trace length, as is shown
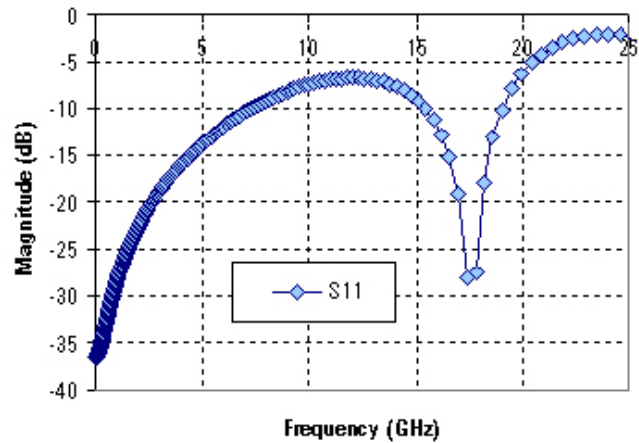
for the lower loss dielectric in Figure 18. This oscillatory behavior is attributed to resonance effects set up by the reflections from the impedance discontinuities caused by the two vias at each end of the stripline. The effect is surprisingly large despite the use of a pseudorandom bit sequence.

To further investigate this phenomenon, the propagation delay of the stripline for simulation configuration 5 was determined (174.17 ps/in). This allows us to plot Figure 18 as a function of the signal round-trip time (twice the trace length) in units of the bit period (100 ps). The resulting graph is shown in Figure 19. It is clear from Figure 19 that the maxima and minima are periodic with the bit period which confirms the original interpretation of the jitter magnitude oscillations as a resonance effect.

This effect can lead to variability in system performance for short interconnect lengths. Small variations of the dielectric constant of the epoxy laminate between manufacturing runs will result in variations of the stripline's propagation delay. This in turn will cause differences in the signal round-trip time for interconnects with the same nominal length. The overall effect on system performance will be a variability of the total jitter that needs to be tolerated by the receiver. In the interest of consistent system performance it will be best to user a lower grade laminate that introduces dielectric losses large enough to sufficiently attenuate reflections.

Table 4. Simulation parameters and results for stripline interconnects.

| Simulation Configuration	Inner Eye Height [mV]	Deterministic Jitter [ps]	Inner Eye Width [ps]	Inner Area [ps*mV]
XFP Reference Eye				
Simulation 4 : N4000-6 (er=4.1, loss 0.025, 12.2 mil separation between reference planes), 5 mil wide stripline, 50 mil track spacing, 0.5 oz copper				
2 in track length	375.7			
4 in track length	321.4	7.9	92.1	14800.5
6 in track length	264.0	10.4	89.6	11827.2
8 in track length	225.6	13.4	86.6	9768.5
10 in track length	190.4	17.5	82.5	7854.0
12 in track length	161.3	21.7	78.3	6314.9
Simulation 5 : N4000-13 (er=4.1, loss 0.016, 12.2 mil separation between reference planes), 5 mil wide stripline, 50 mil track spacing, 0.5 oz copper				
2 in track length	391.1			
4 in track length	345.0	7.1	92.9	16025.3
6 in track length	294.0	8.9	91.1	13391.7
8 in track length	259.6	10.6	89.4	11604.1
10 in track length	227.9	13.6	86.4	9845.3
12 in track length	200.3	16.4	83.6	8372.5
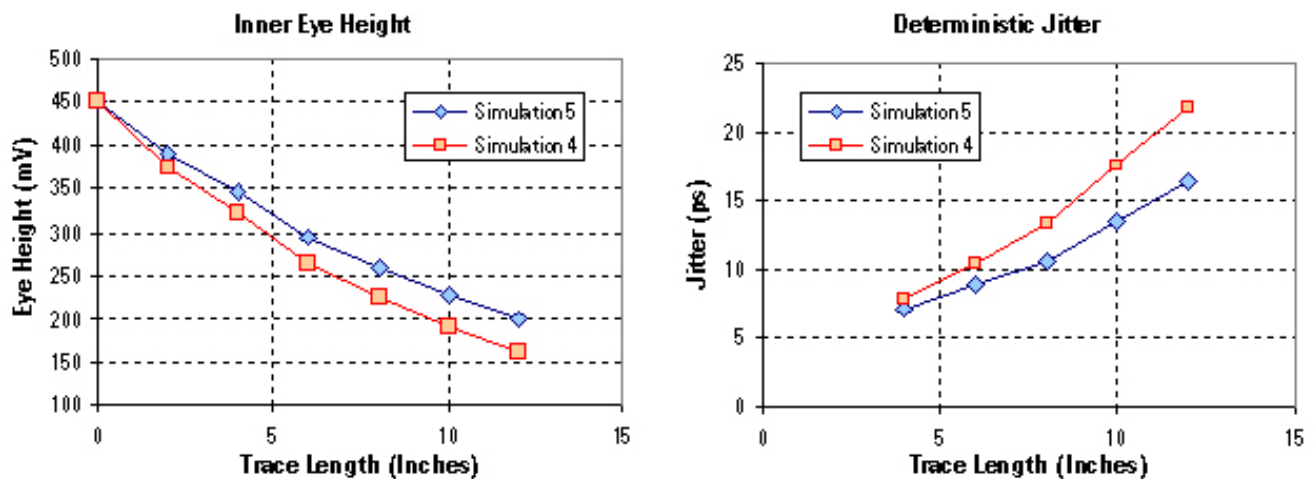
Figure 17. Selected eye diagram parameters for stripline interconnect XFI link configurations
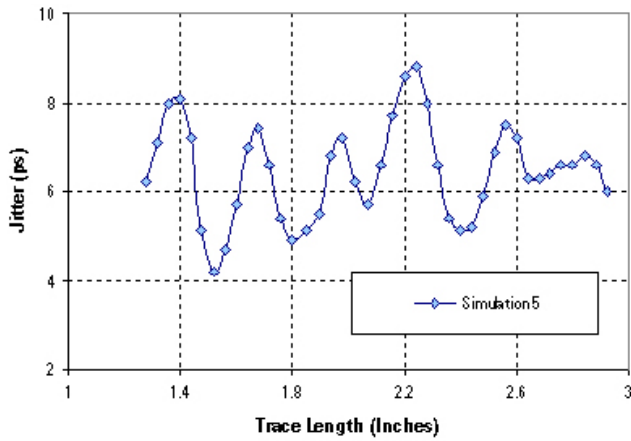
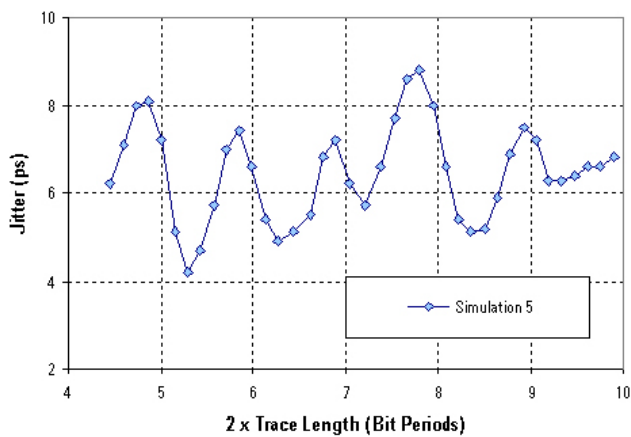**Figure 18. Data dependent jitter as a function of stripline trace length**

Figure 19. Data dependent jitter plotted as a function of the signal round-trip in units of the bit period.

XFI Channel Simulations with a SerDes Receiver

So far the "receiver" circuit was an ideal 100 Ω termination resistor. In a real-world XFI channel this will in most cases be replaced by an Eye Opener or SerDes IC with the termination resistor implemented on the Silicon die as part of the differential input buffer. This greatly simplifies system designs, as no additional surface mounted components are required for a XFI channel. However, this also means that the frequency dependent characteristics of the IC package are between the end of the host-board transmission lines and the termination circuitry. This in turn can have an influence on the quality of the received signal.

To evaluate this effect a model for the IC package was created. An ideal package for a XFI channel component would be a 50 Ω impedance (z0, zdiff =100 Ω) transmission line that would just introduce a delay to the signal but no reflections. Modern Ball Grid Array (BGA) IC packages may get fairly close to this transmission line limit, however, the internal structure of the IC package (eg. package vias and bond wires) will introduce impedance discontinuities. To model this progressively, we will take as

an example a 50 Ω transmission line with a delay td of 90 ps. This corresponds to an IC package interconnect length of approximately 10 mm (~0.4 in), depending on the refractive index of the package material. Instead of describing the interconnect as a transmission line, however, we will break the package interconnect down into a discrete number of identical RLC circuits. In a circuit diagram this would resemble a "ladder" of series resistors and inductors linking capacitors that are connected to ground. Each RLC element constitutes a step of the "ladder" as is shown schematically in Figure 20. The more steps this "ladder" has, the more it will resemble a transmission line. Fewer steps on the other hand will lead to increased losses and pronounced resonances in the S11 and S21 parameters of this IC package interconnect model.

The resonances and the cutoff frequency of this package model move to lower frequencies as the number of RLC circuits is reduced. This is illustrated in Figure 21. For the chosen example of 50 Ω asymptotic impedance and a delay of 90 ps, the total inductance equates to 4.50 nH, and the total capacitance to 1.80 pF. These are distributed equally between the different "steps" of the "ladder" [Hall 2000].

The thick grey line in Figure 20 is the maximum allowed channel loss in an XFI link as per the XFP MSA. The package model consisting of only 2 RLC circuits is clearly not consistent with the performance requirements of an XFI link.

The effect that a realistic package model has on the XFI link budget was investigated for a microstrip transmission line link model. As an example simulation configuration 2 was chosen with a microstrip length of 8 inches.

The signal was probed at the IC pins (point 5 in Figure 1, point D in the XFP MSA revision 1.0). Two eye diagrams that resulted from these simulations are shown in Figure 22. The eye on the left serves as a reference and shows the signal without an IC package model probed at the end of the microstrip lines. The eye diagram on the right shows the same signal after the insertion of an IC package model consisting of 3 RLC circuits. It is evident that the level of jitter has increased, and the maximum inner eye opening is reduced.
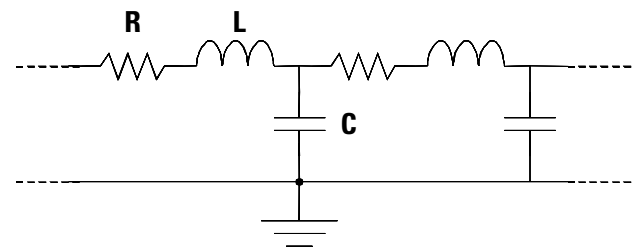
$$L = td * z0 / N \qquad\qquad C = td / z0 / N$$

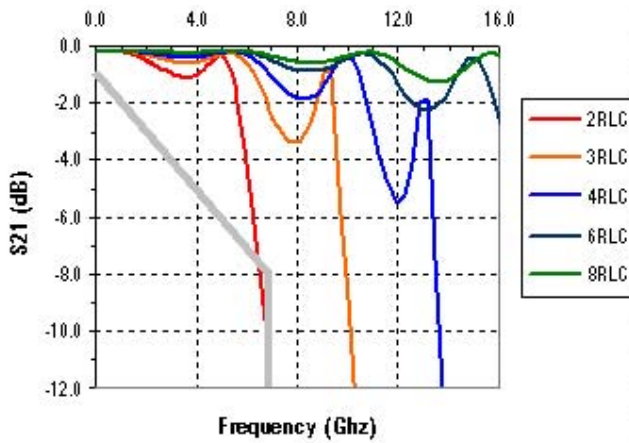**Figure 20. Constituting elements of an RLC-"ladder" package model.**

Figure 21. Transmission characteristics (S21) of the SerDes/Eye Opener IC package model. The package is broken down into multiple identical RLC sections.
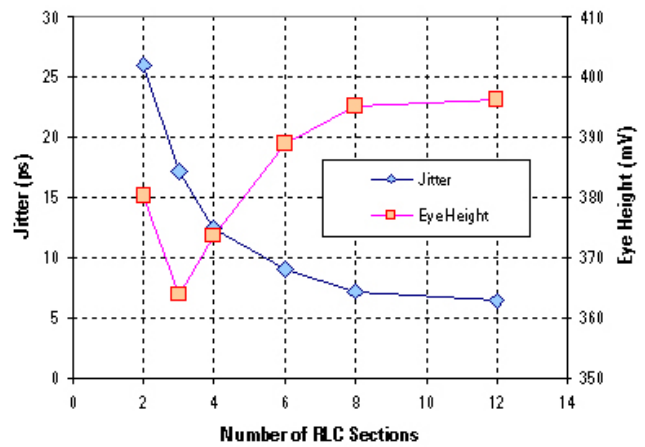

Figure 23. Jitter and inner eye height as function of the IC package characteristics.
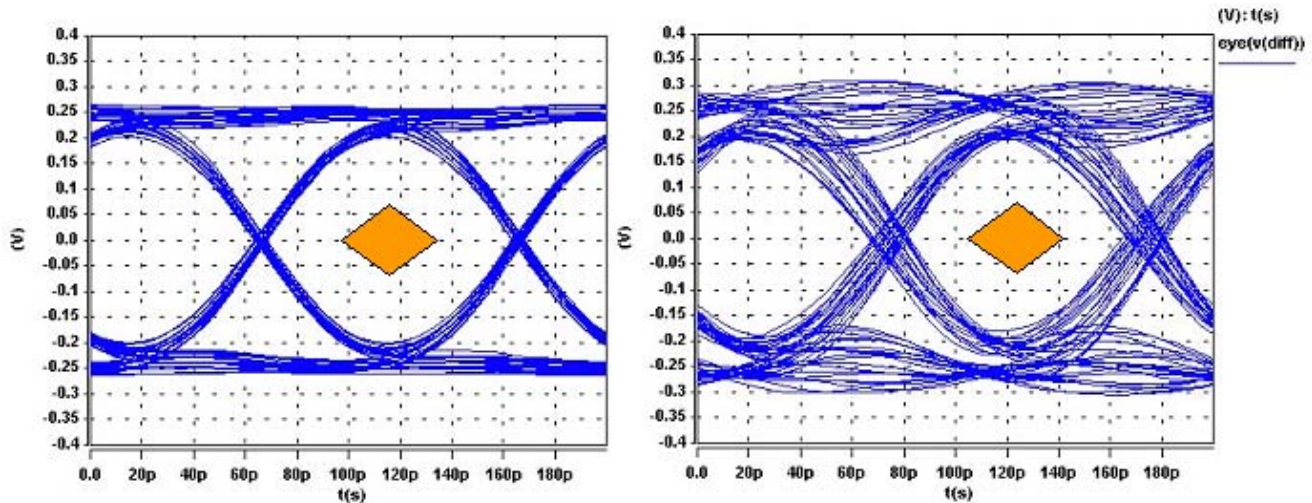

Figure 22. Simulation without IC package (left eye diagram) and with an IC package model consisting of 3 RLC circuits. The signal is probed at point 5 (figure 1, point D in XFP MSA) of the XFI channel reference model.

The jitter and the inner eye height have been derived as a figure of merit from simulations where the total inductance and capacitance of the chosen package model was broken down into 2, 3, 4, 6, 8, and 12 identical RLC circuits. The results are shown graphically in Figure 23.

In order to interpret Figure 23 one needs to remember that fewer RLC sections in the package model means a poorer package with a lower cutoff frequency. A high number of sections means that the package model asymptotically approaches a 50 Ω transmission line. It is therefore evident from Figure 23 that a package with a lower bandwidth (fewer RLC sections) leads to increased jitter and a reduced eye opening. For the evaluation of the overall XFI channel link budget it is therefore important to pay attention to the frequency characteristics of the IC package of the eye opener or SerDes IC. The same argument applies of course the other way round, when the SerDes acts as the transmitter of the electrical signal and the XFP

transceiver module as the receiver. In order to keep jitter to a minimum the bandwidth of the XFP transceiver needs to be optimized in a similar fashion in order to keep any parasitics as small as possible.

One counter-intuitive observation in Figure 23 is the fact that the eye opening seems to increase again if the number of RLC sections is reduced to two. However, one needs to remember that this package model does not meet the loss specification of the XFP MSA. It appears that the inner height of the eye is increased due to the reflection of the high frequency portion of the 10 Gbit/s data stream by the package parasitics. Thus, from the point of view of the Silicon die the IC package acts as a low-pass filter. The reflected high frequency components of the signal will therefore be missing at the die pads, consequently reducing the edge-rate and inner eye-opening at the input buffer where it is most relevant.

Conclusions and Recommendations

The simulation examples and results within this paper have shown how the design of the XFI channel can adversely affect the Signal Integrity of the link. Special attention was paid to the influence on signal quality of the interconnect structure between the quantizer/ eye opener circuits on the XFP module and the eye opener/ SerDes IC on the host board. It became clear that the design decisions will depend on a number of trade-offs:

- For XFI channels where the transceiver and SerDes IC are placed very close to each other, EMI from the traces will contribute little to the overall EMI of the system. This allows the use of microstrip traces with standard, relatively high loss FR-4. Attention needs to be paid to resonance effects due to reflections from impedance discontinuities. The skin-effect resistance of relatively narrow traces and the dielectric losses of standard FR-4 should provide the necessary attenuation for immunity to these reflections.

- For XFI channels where the design requires a large separation between the XFP transceiver and the SerDes or Eye Opener IC, stripline interconnects are the most likely configuration to provide the targeted EMI margin. For good signal integrity, however, the use of low loss FR- 4 will be necessary. Furthermore, it is recommended to employ high-speed design rules for vias like increased clearance diameters and back drilling to reduce via stub lengths.

- If the XFI channel design falls between these limits, it is recommended to determine the optimum configuration through simulation. Avago will support the activities of system designers and signal integrity engineers by providing state-of-the art component models. In addition, Avago's Application Engineering teams will provide design references and simulation support to facilitate the adoption of the XFP standard for next generation systems.

The overriding theme in the successful design of a XFI data channel is perhaps the requirement for a careful analysis of each constituting link element. "Due diligence" of a XFI link design is to establish compliance of each element with the frequency dependent loss specifications outlined in the XFP MSA. Furthermore, the sum of all losses needs to be smaller than the overall link budget. Interactions between the various link elements can still cause the XFI channel to show unexpected behavior and fail the compliance tests, this will have to be verified by signal integrity simulations. However, following this methodology the system design should rapidly convergence towards a solution that will meet the requirements.

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