WHITE PAPER

3D ICs WITH TSVs—DESIGN CHALLENGES AND REQUIREMENTS

CONTENTS

INTRODUCTION

As demands accelerate for increasing density, higher bandwidths, and lower power, many IC design teams are looking up – to 3D ICs with through-silicon vias (TSVs). 3D ICs promise "more than Moore" integration by packing a great deal of functionality into small form factors, while improving performance and reducing costs. 3D IC packages may accommodate multiple heterogeneous die—such as logic, memory, analog, RF, and micro-electrical mechanical systems (MEMS)—at different process nodes, such as 28nm for high-speed logic and 130nm for analog. This provides an alternative to system-on-chip (SoC) integration, potentially postponing an expensive move to a new process node for all of the functionality developers want to place in a single package.

3D ICs with TSVs are expected to have a broad impact in areas such as networking, graphics, mobile communications, and computing, especially for applications that require ultra-light, small, low-power devices. Specific application areas include multi-core CPUs, GPUs, packet buffers/ routers, smart phones, tablets, netbooks, cameras, DVD players, and set-top boxes.

While there is great interest in this emerging technology, it is still in its early phases. Standard definitions are lacking, the supply chain ecosystem is still in flux, and design, verification and test challenges need to be resolved. This paper presents a brief overview of 3D IC technology, and then discusses design challenges, ecosystem requirements, and needed solutions. While various kinds of multi-die packages have been available for many years, this paper focuses on Silicon Realization of stacked die with TSVs, particularly those where different types of die are stacked (such as logic, memory, analog, digital, or RF).

From a design standpoint, the good news is that extensive retooling is not needed for 3D ICs. There is no need to acquire a new "3D" design system. There are also no apparent showstoppers in process technology. However, new capabilities are needed in such areas as architectural analysis, floorplanning, place and route, thermal analysis, timing, signal integrity, IC/package co-design, and test. Some of these capabilities are available today, and others are under development.

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What is ultimately needed is a Silicon Realization approach to 3D ICs. As described in the EDA360 vision paper[1], Silicon Realization[2] can take many forms, including analog and digital IP blocks, complete ICs and systems-on-chip, or 3D ICs. But whatever the end product, three characteristics mark Silicon Realization flows: unified design and verification intent, the appropriate use of higher levels of abstraction, and convergence with physical, electrical and manufacturing data into a successful "signoff" flow. A successful 3D IC design environment will capture design intent up front, support abstraction with early estimation and floorplanning, and achieve convergence through test, implementation, extraction, analysis and packaging tools.

A CLOSER LOOK AT 3D ICS WITH TSVS

Systems-on-chip (SoCs) today pack an incredible amount of functionality onto a single silicon die. SoCs typically include a processor, digital logic, memory, and analog components, along with embedded software. Some SoCs have hundreds of millions of gates and are pushing gigahertz speeds.

However, traditional single-die SoCs have some disadvantages. One is that all components are placed on the same die at the same process node, even though analog and RF design at advanced process nodes is extremely challenging. If a design team tries to implement analog circuitry at an advanced process node, it may take a great deal of time to develop and test the necessary IP blocks, as well as cope with process-related issues such as variability and leakage.

Another challenge for single-die SoCs is mixed-signal integration and verification. Placing analog and digital circuitry in close proximity can cause many problems. Alternatively, sensitive analog or noisy digital components could be placed in a separate IC, but that makes it necessary to drive signals between individual packages, which consumes power and reduces performance.

Perhaps the biggest concern with SoC design today is the rising development costs. According to industry estimates, SoC hardware and software development may top $100 million at the 32nm process node. Additionally, long development cycles result in an additional cost. If costs cannot be reduced, advanced-node SoCs will be feasible only for a small number of high-volume applications.

One alternative to single-die SoCs is to place multiple silicon die into a single package. Then it will be possible, for example, to use a 90nm process for analog/RF circuitry, and a 28nm process for digital logic (Figure 1). The terms system-in-package (SiP), silicon-in-package, and multi-chip module (MCM) have all been used to refer to multi-die packaging technologies in which multiple die are mounted on a common substrate that is used to connect them together. These technologies started to gain acceptance in the early 1990s.

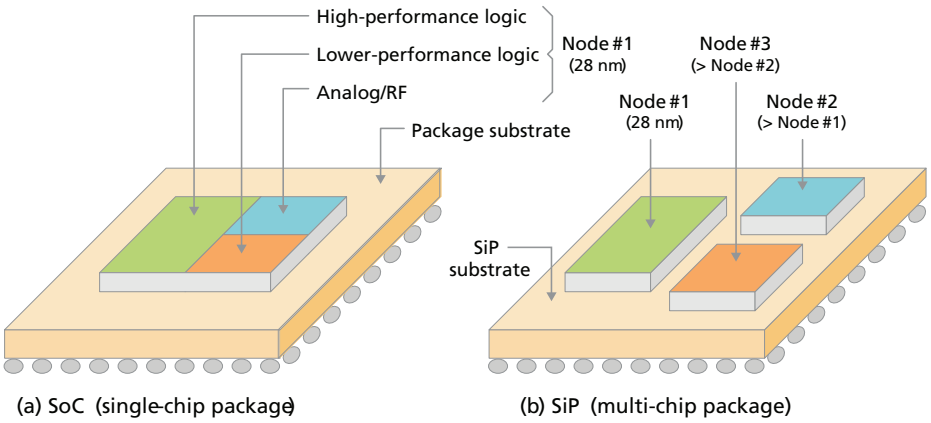

Figure 1: System-on-Chip (SoC) compared to System-in Package (SiP)

The SiP approach offers several advantages compared to SoC implementations, including the fact that the various analog, digital, and memory die can each be implemented using the most appropriate technology process for that domain. In addition to logic, memory, analog, and RF functionality, modern SiPs may also include micro-electromechanical systems (MEMS) components such as antennas or mirrors.

Other packaging options that have evolved over the years include package-in-package (PiP), where a number of smaller SiPs may be mounted in a larger SiP, and package-on-package (PoP), where one SiP may be mounted on top of another SiP. Both PiP and PoP assemblies may be categorized as 3D ICs, but neither offers the performance, power, density, and form factor of true 3D ICs using TSVs.

Until recently, silicon die have been attached to the SiP substrate using conventional wire bond and/or flip-chip technologies. Today, a silicon interposer substrate (either passive or active) may be added to provide much finer die-to-die interconnections, thereby increasing performance and reducing power consumption. A silicon interposer also includes TSVs, which provide connections from the upper metal layers to additional backside metal layers, as illustrated in Figure 2. Sometimes this technique is referred to as 2.5D stacking.

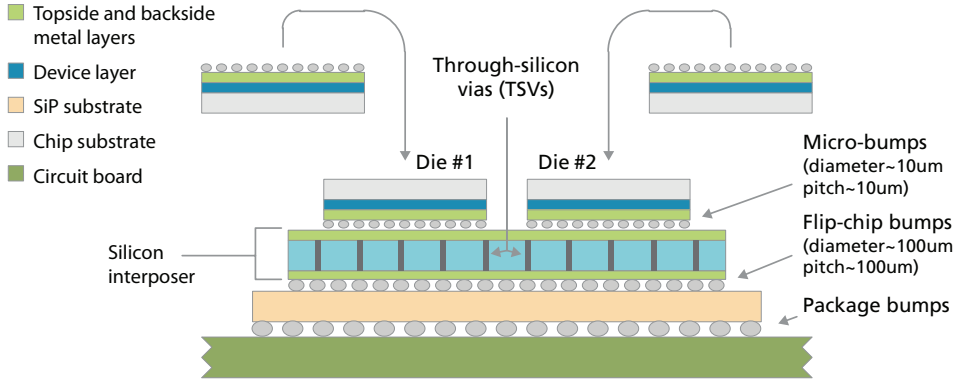

Figure 2: Adding a silicon interposer with TSVs (only two die are shown for simplicity)

A TSV is a vertical electrical connection passing through a silicon die. TSVs are copper vias with diameters that may range from 1 to 30 microns. A "true" 3D IC using TSVs involves two or more die connected together using TSVs. For example, consider a scenario in which one die containing TSVs is attached to the SiP substrate using conventional flip-chip technology. Meanwhile, a second die is attached to the first as illustrated in Figure 3.

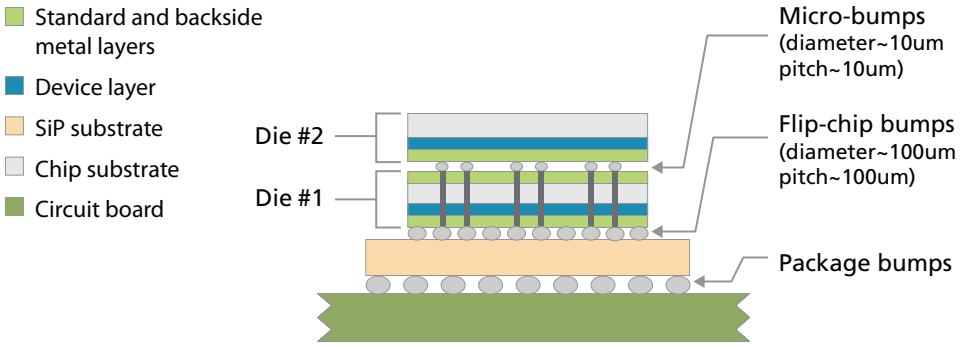

Figure 3: A simple 3D IC using TSVs

The 3D IC shown above would be referred to as a back-to-face (B2F) configuration, because the back of the first die is attached to the face of the second die. It would also be possible to have back-to-back (B2B) and face-to-face (F2F) configurations, especially when more than two die are stacked in this manner.

As of this writing, it is unusual to see more than two layers of die stacked on top of each other. Even so, it is not uncommon to see a larger die on the bottom attached to two or more smaller die. In the future, we may expect to see more complex scenarios as illustrated in Figure 4.

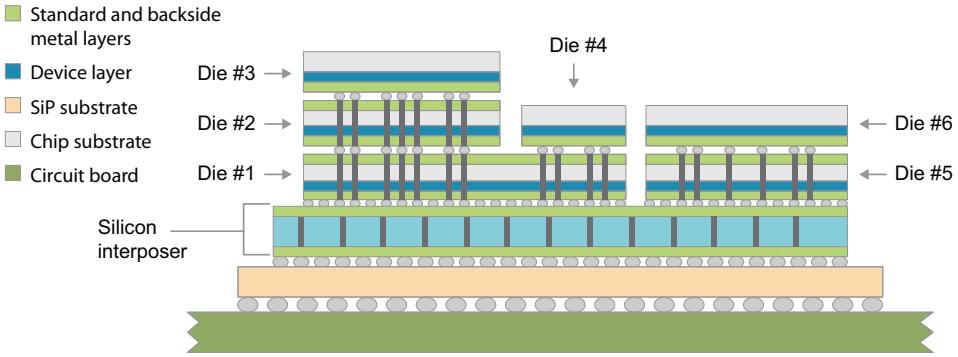

Figure 4: A more complex 3D IC using TSVs and 6 die

The advantages of 3D ICs with TSVs, compared to traditional SoCs, can be summarized as follows:

- Lower costs are possible, because all functionality including analog and memory does not need to move to advanced process nodes.
- It's easier to meet high interconnect speeds and bandwidth requirements, which will reach 100 Gbits/second for advanced memory technologies.
- 3D ICs allow miniaturization, saving space on the board and in the end product. They're ideal for extremely compact mobile devices.
- 3D ICs can reduce power because big drivers are no longer needed. A 3D stack can use small I/O drivers with lower power. Further, reduced resistance-inductance-capacitance (RLC) helps reduce power.
- Interconnect between packages is reduced, allowing for faster performance and a better power profile.
- Time to market can be faster, thanks to modularity, the potential for "die reuse," and the ability to leave analog/RF at higher process nodes.
- Emerging technologies such as photonics or MEMS can potentially be integrated into 3D stacks.

Compared to a wire-bonded SiP, TSVs offer reduced RLC parasitics, better performance, more power savings, and a denser implementation. Compared to a silicon interposer approach, a vertical 3D die stack offers a higher level of integration, smaller form factor, and faster design cycle. But a 3D stack raises some additional challenges, including thermal, timing, and power management concerns. These challenges are discussed in the next section.

3D IC DESIGN CHALLENGES AND REQUIREMENTS

While 3D ICs with TSVs do not require a revolutionary new 3D design system, they do require some new capabilities that need to be added to existing toolsets for digital design, analog/custom design, and IC/package co-design. These capabilities should support the three key Silicon Realization goals – unified design intent, abstraction, and convergence. The end goal is to optimize system cost with the shortest possible turnaround time. If 3D ICs cannot be both cost and time effective, they will not enjoy widespread adoption.

Above all, a comprehensive solution is needed. Many 3D stacks will combine digital and analog/RF circuitry, requiring a strong analog/mixed-signal capability. Because of the unique packaging requirements of stacked die, an IC/package co-design capability is a must. Additionally, fitting 3D ICs

on a board is challenging, requiring a capable PCB layout system with appropriate analysis tools. Thus, anyone who presents a complete "solution" must provide expertise in digital, analog, IC, package, and PCB design.

3D IC design is a shared effort. The package designer knows where to put pins, but knows little about the design of the IC. The IC designer can put TSVs inside the die, but has limited knowledge of the package. The PCB designer will have to integrate the 3D IC package with other components on the board. 3D ICs will require close collaboration and co-design among groups that have historically worked separately.

TSVs have some special tooling requirements. TSVs in active layers must be designed by IC design tools. However, TSVs in active layers may be planned with packaging or SiP tools. TSVs in passive layers may be both planned and designed with packaging or SiP tools. Silicon interposers are best designed with digital IC design tools.

In order to meet the design challenges of 3D ICs, new capabilities are needed in the following areas:

- System-level exploration
- 3D floorplanning
- Implementation (placement, optimization, and routing)
- Extraction and analysis
- Design for Test (DFT)
- IC/package co-design

Challenges and capabilities are described in the following sections.

SYSTEM LEVEL EXPLORATION

Sometimes called "Pathfinding," 3D IC system-level exploration will both raise the abstraction level and provide a way to describe design intent to downstream tools. It will help users partition designs into separate chips, select the appropriate silicon technology for each chip, determine where functionality goes, choose the best die order in the stack, and optimize connectivity between chips. This intent must then be carried through the design process.

Existing system-level exploration tools can provide early power, area, and cost estimates, and allow what-if explorations across architectures, silicon IP choices, and foundry processes. However, these tools need to be extended to serve stacked die implementations and package considerations.

3D FLOORPLANNING

TSVs are very large compared to logic gates and other circuit features. Thus, the number and location of TSVs is crucial. With too many TSVs, the wire length goes up. TSVs cause coupling, which can be reduced by adding space to their keep-out zones – but this adds to the area. TSVs also cause mechanical stress, which can impact the performance of nearby devices.

Given these considerations, a TSV-aware 3D floorplanning capability is quite challenging. It must provide an abstraction level to capture all the die, and provide a unified representation of intent for placement and routing tools.

A 3D floorplanner should work in the X, Y, and Z directions, and should have visibility into the top and bottom of each die. This helps optimize the placement of blocks, TSVs, and micro-bumps, and shortens interconnect distances, thus improving performance and power. For continuous design convergence, micro-bump and TSV assignments should take into account the floorplans on adjacent die.

Ideally, a 3D floorplan will be thermal-aware and will help avoid thermal hot spots. It will also help users determine the optimal placement of die into stacks. The order of the stack is important—die in the middle are most susceptible to thermal problems. The bottom chip in the stack is closest to the air flow, so it's best to put the "hottest" chip there.

IMPLEMENTATION

Synthesis, placement, and routing for 3D ICs brings forth a number of new considerations. For example, there are new layout rules that may be driven by features on adjacent die. The back-side redistribution layer (RDL) is a new layout layer. And given their size, TSVs themselves are a significant new layout feature.

A digital implementation system that supports 3D ICs must be "double sided aware," taking into account both the top and bottom of each die. This may call for a new modeling and database infrastructure, TSV-specific tools, and support for a variety of stacking styles.

Power planning for a single-die IC is hard enough. With a 3D stack, it gets more complex. Designers need to provide enough power to drive all of the die, including the top-most die. Designers must manage vertical voltage drop and reliably simulate system power consumption. Tools need to support power distribution for TSVs and micro-bumps. A unified representation of power intent should be carried across the entire 3D IC design.

Place and route tools should include thermal constraints to avoid hot spots. Routing tools need to handle TSVs and micro-bumps properly, route signals across multiple die, and verify the bump alignment between adjacent die.

Managing clocks across multiple die while avoiding skew is another challenge. If there are different clocks for different die, the designer must figure out how to synchronize them.

Analog implementation environments also need to add support for 3D ICs. Examples of useful capabilities include multi-chip visualization with background views; support for bump, TSV, and reverse-side routing; and connectivity extraction maintained through TSV connections.

Throughout the design convergence process, design intent must be maintained and checked, and the necessary abstraction techniques must be applied for proper implementation and analysis.

EXTRACTION AND ANALYSIS

Extraction and analysis tools are crucial for design convergence. However, existing extraction and analysis tools need to be extended for 3D ICs. For example, the tools must consider RLC parasitics for TSVs, micro-bumps, and interposer routing. Further, analysis tools must be 3D-aware. Timing, signal integrity, power, and thermal gradients must be analyzed across multiple die. Multi-die static timing must be validated, with an understanding of interactions between multiple die and with the package.

Because the metal stack creates heat gradients, thermal analysis and signoff is critical, especially for die located in the middle of the stack. Further, the substrate thinning required for 3D stacks results in relatively poor heat dissipation. After placement and routing, thermal signoff is needed to ensure hot spots are below specified limits, and that thermal effects do not have a negative impact on performance or leakage.

Signoff raises new questions with 3D IC stacks. For example, can design rule checking (DRC) and layout-versus-schematics (LVS) run on the entire stack? Can timing be verified for the entire stack? Is there any crosstalk between die?

Electromagnetic interference (EMI) is a possible concern for 3D ICs, raising a potential need for analysis tools. A multi-die package offers less shielding than a single-die package, and thus offers more likelihood that emissions could escape.

Finally, to facilitate TSV connections, the wafer is thinned to implement a 3D IC. This causes stress and adds susceptibility to thermal changes. Testing is needed across a range of thermal variations to ensure the wafer won't warp, bend, crack, or break.

DESIGN FOR TEST

Test raises many challenges for 3D ICs, including access to die inside a stack and proper handling of thinned wafers. Both new standards and tool support are required to help validate that design intent is maintained once 3D IC silicon is realized, and to diagnose issues properly if the system doesn't behave as intended.

Like conventional single-die IC test, 3D IC test must be considered at two levels – wafer test (for the silicon die), and package test (after die assembly into the package). The difference is that in the 3D IC fabrication, there are many more intermediate steps, such as die stacking and TSV bonding. This provides many more opportunities for wafer test before final assembly and packaging.

Wafer test is needed for cost optimization. If a die is bad, it can be thrown away before it is placed in a package. If a package-level test fails, the entire package would have to be thrown away. Thus, wafer test is highly desirable, especially early in the product lifecycle while defects may still be relatively high.

But wafer test for 3D ICs is challenging for three reasons. First, today's probe technology is unable to handle the finer pitch and dimensions of TSV tips, and is generally limited to handling several hundred probes, whereas the TSVs may have several thousand probes. Second, probe technology leaves scrub marks that can potentially cause problems with the downstream bonding step. Finally, wafer test requires the creation of a known-good die (KGD) stack. To stack known-good die, the wafer must be thinned by about 75 percent so the tips of the TSVs can be exposed. However, as the thinned wafer is contacted by a wafer probe, there's a danger of damaging the wafer.

3D ICs also introduce new intra-die defects. These may be introduced by new manufacturing steps such as wafer thinning, or by bonding the top of a TSV to another wafer. Thermal effects are another potential sources of defects, because excessive heat may be generated from the densely packed stack of dies. Thermo-mechanical stress is caused by different thermal coefficients of the various materials in the stack. Despite the differences in the manufacturing steps, the resulting faults (shorts, opens, delay defects) appear to be similar to what we see in conventional ICs. It is possible that new fault models may be required as we get more empirical data.

Modeling defects through TSV-based interconnects is a new area. These defects may be introduced in the fabrication or the bonding of TSVs. Fortunately, defects introduced through TSVs can be mapped to existing fault models, such as opens, shorts, static, delay, and bridging faults. However, a methodology is needed to map TSV defects to known fault types.

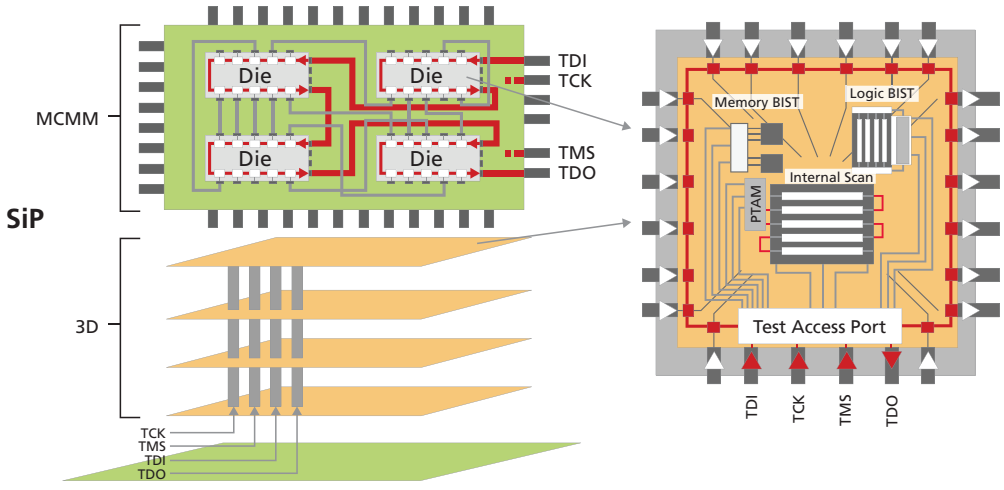

Figure 5: Test access to individual die within a stack can be challenging. DFT techniques like memory BIST, logic BIST, and internal scan can help.

A sound methodology for 3D IC test includes a DFT architecture that provides efficient ways to control and observe individual die from the chip I/Os, while providing different test access modes (such as a mode for a known good die test or a known good stack test). Conventional DFT

architectural approaches and techniques such as on-chip compression, boundary scan, memory built-in self-test (MBIST), reduced pin count testing, and on-chip clocking for at-speed test are broadly applicable, and need to be configured and optimized to meet 3D controllability and observability goals. The trick is one of making an intelligent allocation of DFT resources across the multiple die to minimize the area overhead, while meeting constraints for test cost and shipped product quality.

IC/PACKAGE CO-DESIGN

Developers of 3D ICs need to remember that any electronic product includes three different fabrics – chips, packages, and boards. Designing the chip first and throwing it "over the wall" to package and board designers will not result in design convergence on an optimal, cost-effective solution.

If the chip, package and board are not designed co-operatively, the interconnect will not be optimized, and extra vias will be needed to handle signals that cross from one point to another. As a result, performance will be reduced, additional board layers may be needed, and board and package costs may rise. Further, without co-design, timing, power, and signal integrity will not be optimized.

IC/package co-design is important for 3D ICs because there are a large number of I/Os, and because the cost of packaging goes higher with multiple die in one package. Without co-optimization, the package could end up costing more than the silicon die. Important capabilities include I/O feasibility planning, connectivity management, 3D visualization, SiP layout, and support for multi-fabric analog and RF circuitry. To ensure complete design convergence, the packaging tool must understand the IC and package design intent, and should effectively abstract the IC design database to provide constraint-driven layout of the package substrate.

The board must be considered as well. 3D die stacks result in additional interconnect that will have to find its way down to the board. As more connectivity is handled inside the package, there's less complexity on the board. The board designer needs to know what's going to be positioned near the 3D package. By positioning and rotating components properly, the designer can reduce the number of layers required for the board.

Some companies drive co-design from the board up. They know where components will go on the board, and those locations are fixed. They then design the package that contains the stacked die in order to optimize connectivity, and to allow the minimum number of layers on the PCB. But it's not so important where co-design starts – what's important is that it is done to assure convergence for the 3D IC Silicon Realization process.

FORGING A 3D IC ECOSYSTEM

3D IC/TSV Silicon Realization will never become "mainstream" and step outside the IDM world unless 3D ICs can be designed and produced in a cost-effective way, with sufficient turnaround time to meet market windows. This will be possible only with a robust and well-defined supply chain ecosystem, including semiconductor design companies, EDA vendors, IP suppliers, foundries, and outsourced semiconductor assembly and test (OSAT) providers.

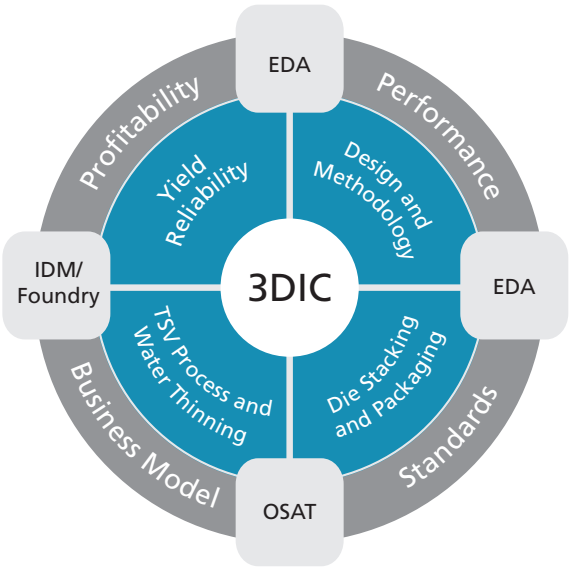

Figure 8: Profitable 3D IC design requires a well-defined ecosystem

Boundaries between the different players may start to blur. For example, when are TSVs created and who is responsible? Possible implementation steps include:

- Via first – wafer processing starts with TSVs and is done by the foundry.
- Via middle – TSVs are created after transistors, but before back end of line (BEOL), by the foundry.
- Via last – TSVs are created after BEOL, probably by the OSAT.

Since one size does not fit all with 3D ICs, the supply chain needs to be adaptable to customer needs.

Many customers will want to line up a second-source 3D packaging service provider before production is started. Additionally, key strategic alliances between memory suppliers, logic IDMs, foundries, and packaging subcontractors will need to be forged.

Foundries need to establish design rules, create models and libraries, and provide process design kits (PDKs) and reference flows. One example of a design rule is to avoid placing TSVs too close to active devices, because they cause mechanical stress that may change the performance of the device. Tools must be aware of recommended TSV diameters and pitches. They need to understand distances between TSVs as well as the width of metal routing to TSVs.

In 2009, TSMC announced Reference Flow 10.0, which offered SiP capabilities. Reference Flow 11.0, announced in June 2010, addresses 3D ICs with new TSV design and analysis capabilities, including placement and routing, physical verification, and thermal analysis for a two-die stack. GLOBALFOUNDRIES is also actively working on support for 3D ICs with TSVs.

OSATs will play a role in assembling early 3D stacks and interposer configurations, combining die from different foundries, and developing tests for 3D stacks – but in the long term they will have to compete with foundries who are pulling OSAT tasks in-house.

3D IC STANDARDS

Standards will become an important part of the 3D IC ecosystem. An initial standards effort may focus on defining a taxonomy of terms. Down the road, I/O standardization between interfaces such as memory, logic, and interposer layers will be helpful.

Meanwhile, the 3D-IC Alliance[3] is focusing on the manufacturing side, and has released the Intimate Memory Interconnect Standard (IMIS) to standardize vertical interconnect requirements. Another area calling out for standardization is 3D IC test. Two emerging standards - IEEE 1149.7 compact JTAG and IEEE P1687 internal JTAG (iJTAG)—can be deployed together to embed test structures in 3D ICs.

The IEEE 1500 standard for embedded core test makes the pins of an IP core controllable and observable. The same principle could potentially be used to access individual die in a 3D stack. The IEEE 1500 "core test wrapper" concept places a DFT wrapper around a core. In a 3D IC, this concept could place an entire die in a wrapper and make it accessible through a product-level I/O interface. The same test patterns could be reused at the package test level.

CONCLUSION

3D ICs with TSVs represent a major new trend in the semiconductor industry. They offer compelling power, performance, and form factor advantages in many application spaces, and they may curb the escalating costs of SoC development. Because designers can stack die from different process nodes, it is no longer necessary to move all system components, including analog and RF, to a single process node.

While there are no major showstoppers from a design or process point of view, much remains to be done to bring 3D ICs into volume production by mainstream users. New capabilities are needed in such areas as system-level exploration, 3D floorplanning, implementation, extraction/analysis, test, and IC/package co-design. For optimal, timely, cost-effective design, a 3D IC Silicon Realization flow will support unified design intent, abstraction, and convergence with physical and manufacturing data. A well-defined ecosystem including foundries, IP providers, EDA vendors, and OSATs needs to emerge, with design kits and reference flows.

Cost-effective 3D IC design requires the co-design of three fabrics – chip, package, and board. With comprehensive offerings in analog and digital implementation, packaging, and PCB design tools, Cadence is uniquely positioned to support the 3D IC revolution and to provide the capabilities that are needed for cost-effective design of 3D ICs with TSVs.

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