

# A Two-Layer Board Intellectual Property to Reduce Electromagnetic Radiation

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**Abstract**—A non-ideal return path in the printed circuit board (PCB) with a split reference plane will increase electromagnetic interference (EMI) that is encountered in the digital LCD-TV system using a 2-layer PCB. An innovative layout skill using the surface mounted jumpers or zero ohm resistors to connect the power nets in the PCB and DDR SDRAM can avoid the split reference plane in the bottom layer. From the S-parameters simulation, the proposed PCB design induces less signal insertion loss, which is expected to have less radiation. The radiated emission measurement was also performed to verify the 2-layer PCB with the solid reference plane achieving less electromagnetic radiation from 0.36 dB to 8.65 dB ( $\mu\text{V}/\text{m}$ ) in the range of DDR operating and harmonic frequencies.

## I. INTRODUCTION

The trend of consumer electronics, such as digital LCD-TVs and DVD players, is cost reduction to satisfy the popular entertainment demands. Suppliers not only use the advanced chip process, but also the low cost packages and PCBs to reduce total system cost. The 4-layer PCBs with the dedicated ground and power layers are usually employed for high-speed signals routing in the conventional consumer electronics. If those two dedicated layers have to be removed to become the 2-layer PCB for board cost reduction, it always induces electromagnetic radiation problems, especially for the systems with high-speed memory interfaces. Many papers proposed the analyses for the effects of signal trace passing over the split ground in the packages or PCBs [1]–[3]. However, few papers presented how to reduce the excessive radiation caused by the non-ideal return path in 2-layer PCBs. In this paper, a PCB layout technique is proposed to maintain ideal return paths for high-speed traces routing. Our goal is to implement and verify the digital LCD-TV in 2-layer PCB including the high-speed memory interfaces with less electromagnetic radiation using S-parameters simulation and EMI measurement.

## II. MEMORY INTERFACE PRE-LAYOUT

The JEDEC defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionalities, AC and DC parametrics, packages and pin assignments [4]. Fig. 1 shows a 256-Mb (4-Mb  $\times$  4-Bank  $\times$  16-bit) DDR SDRAM packaged using a standard thin small outline package (TSOP). There are 66

leads in the TSOP package including the power pins, leads 1, 3, 9, 15, 18, 33, 55, and 61, on the two sides of package. The signal traces connect the digital LCD-TV controller to the memory on the top layer of 2-layer PCB directly. Because there is no dedicated layer assigned for the memory power supply ( $V_{DD}$ , 2.5V) in the 2-layer PCB, the power delivery network (DDRV) connects the power pins on one side of DDR SDRAM from the low dropout (LDO) regulator in the PCB, and then connects the other power pins on another side of DDR SDRAM package using the plated through hole and the bottom traces. Fig. 2(a) illustrates the conventional DDR SDRAM interface layout in the digital LCD-TV system. The color of salmon represents the bottom layer. The rest means the top layer except black and white giving the notations or gaps. The power traces (pink) in the bottom layer break the reference plane (ground layer) that produce the non-ideal return paths for DQ0 and DM0 signals. In order to maintain the bottom having “solid” reference plane (no splits), the surface mounted resistor ( $0\ \Omega$ ) or jumper is used to connect the DDRV net between the LDO regulator and the power pins in DDR SDRAM. One surface mounted resistor ( $0\ \Omega$ ) connects the DDRV net to the pin-1 of DDR SDRAM, and then DQ0 trace routes under the resistor and cross the solid ground plane as shown in Fig. 2(b). Another jumper on the bottom layer connects the DDRV net from the LDO regulator to the DDRV island below the memory package, so the ground plane beneath the DM0 trace has no splits, which means “solid” thereafter. Therefore, all signal traces DQ0-7, DM0, and DQS0 have more ideal return paths in the 2-layer PCB.

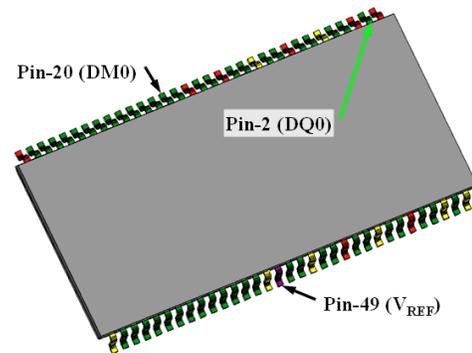
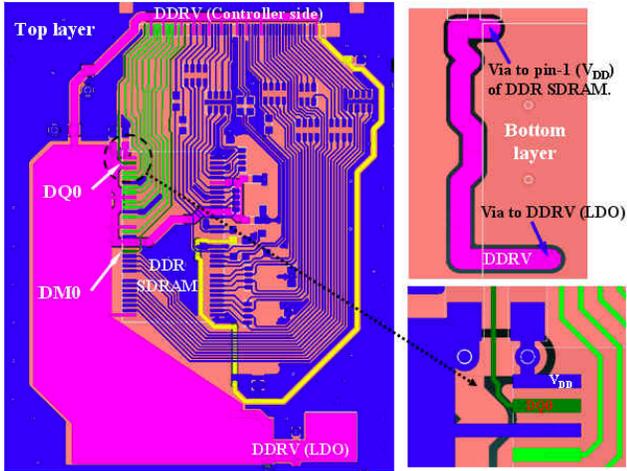
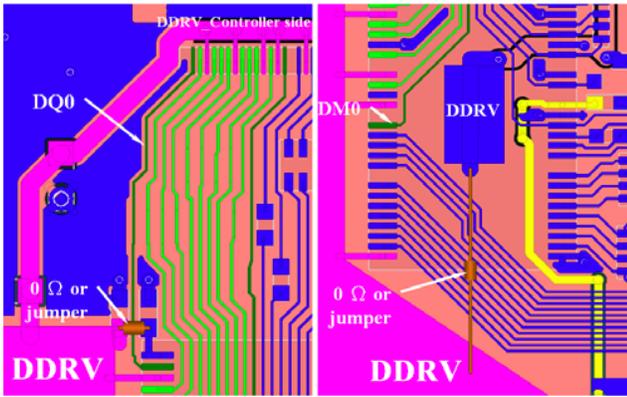


Figure 1. Pin assignment of DDR SDRAM. Red leads are the power pins, yellow leads are the ground pins, and green leads are the signal pins.



(a)

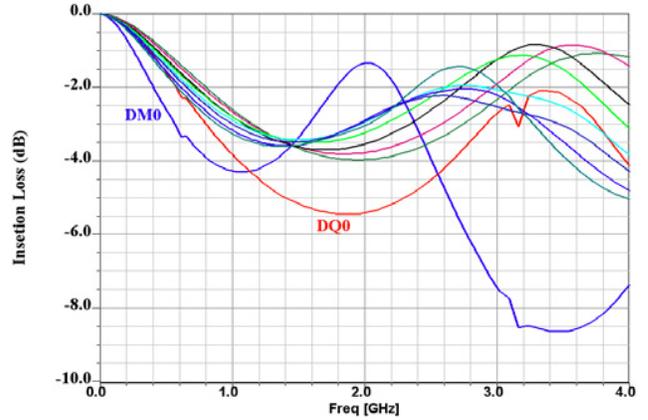


(b)

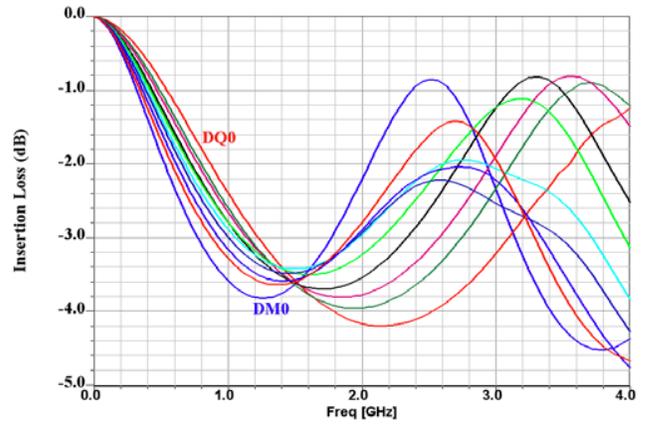
Figure 2. Conventional DDR SDRAM interface pre-layout in the digital LCD-TV system using a 2-layer PCB (a); and modified PCB design maintaining the solid ground layer for signals DQ0-7, DM0, and DQS0 (b).

### III. S-PARAMETERS SIMULATION

The standard 2-layer PCB has 1 oz. copper on the top and bottom layers separated by 0.058" FR-4 core. Trace width is 0.006". Ansoft SIwave<sup>TM</sup>, a full-wave electromagnetic simulator [5], was used to simulate S-parameters for signal traces DQ0-7, DM0, and DQS0 up to 4 GHz in the 2-layer PCBs with and without the slotted ground layers which are depicted in Fig. 2. Each signal trace was assigned with two ports at both ends (controller and DRAM sides) terminated to a 50- $\Omega$  load. The reference (ground) plane is in the bottom layer. Fig. 3 shows the simulation results. The return losses of all signal traces passing over a solid reference plane are within -5dB. Accordingly, Fig. 3(a) illustrates DM0 signal with the slotted ground layer experiencing insertion loss as low as -8dB. At frequency of 1 GHz, there are 1.4 and 0.7 dB improvements for DQ0 and DM0, respectively, with the solid ground layer. According to power conservation, less insertion loss results in less return loss. Therefore, less radiation is expected.



(a)



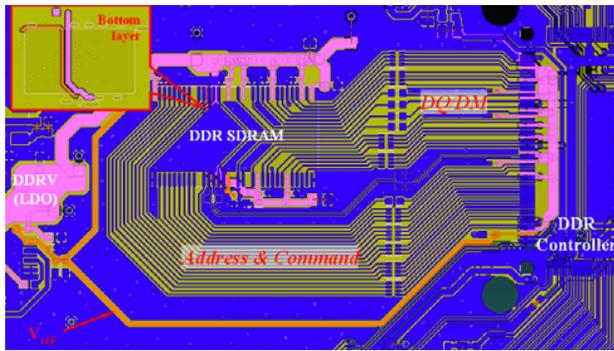
(b)

Figure 3. Simulated insertion losses of DDR signal traces in the 2-layer PCB: PCB with the slotted ground layer (a); and the solid ground layer (b).

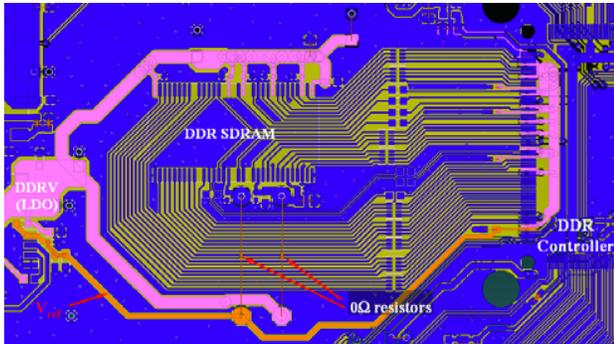
### IV. EMI MEASUREMENTS

High-speed return currents follow the path of the least inductance that lies directly under a signal conductor to minimize the total loop area between the outgoing and returning current paths [6]–[7]. The longer return path results in larger current loop, and then more radiation. Furthermore, since the slot effectively behaves as an antenna, it does not only radiate but receives energy as well [8]. Fig. 4 illustrates the experimental 2-layer PCB designs (Model-A and Model-B) of the LCD-TV system with memory interfaces. Model-A was laid out with the referenced power supply ( $V_{REF}$ , 1.25V) and the main power supply ( $V_{DD}$ , 2.5V) on the bottom layer forming the slotted ground. In order to maintain the solid ground, in Model-B, two 0  $\Omega$  dual inline package (DIP) resistors were used on the top layer to connect  $V_{REF}$  and  $V_{DD}$  nets to pins 49, 55, and 61 of the DDR SDRAM.

Fig. 5 shows Model-A and Model-B that were fabricated for EMI measurements. The DDR controller was packaged in an exposed pad low-profile quad flat pack (E-pad LQFP) package. Those designs are almost the same, including the routing of trace width, space, and length, damping resistors,



(a)



(b)

Figure 4. Model-A is the DDR SDRAM interface layout in the digital LCD-TV system with the slotted ground layer (a); and Model-B is the proposed PCB layout to maintain the solid ground layer for all memory signal traces (b).



(a)



(b)

Figure 5. Photographs of memory interface between DDR SDRAM and LCD-TV chipset in the 2-layer PCB: Model-A (a), and Model-B (b).

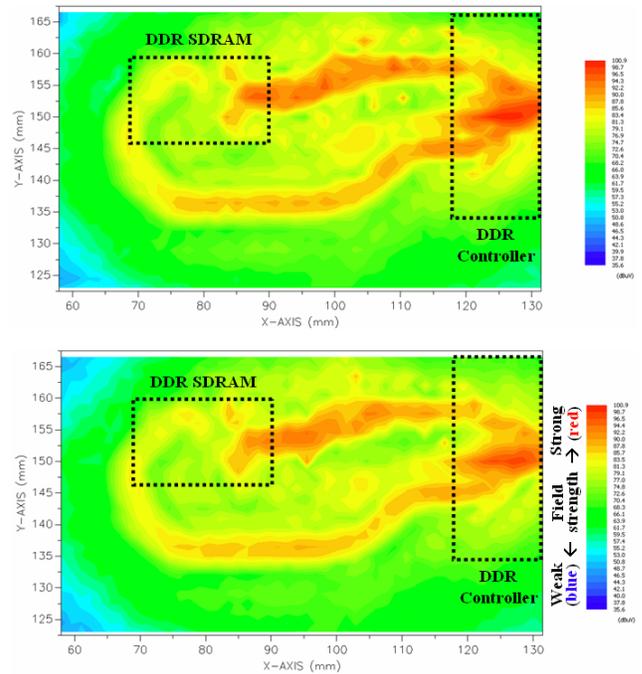


Figure 6. Measured near field strength distribution in the region of memory interfaces: Model-A (a), and Model-B (b).

and decoupling capacitors, except that two  $0\ \Omega$  resistors become the bridges supplying  $V_{REF}$  and  $V_{DD}$  to the DDR SDRAM. Because the resistor is not expensive, the system costs of those models are almost the same. Furthermore, due to the fixed component size and location, DDR trace width, space, and routing length, the Model-B design can be reused for the next LCD-TV development if it is verified for EMI reduction. Then, the reusable PCB design can be named as the board intellectual property (BIP).

#### A. Near Field Radiation

Before the measurement of far field radiation, the measurement of near field radiation was taken using Hitachi EMV-200 tester [9]. The testing configuration is as follows:

- Sweep frequency: 30 MHz to 1 GHz.
- Fix scanning probe location: 0.5 mm above the DDR controller.
- Scan the region of memory interfaces with step of 1.5 mm (x- and y-axis) and angles of 0 and 90 degrees.
- DRAM DQ operating at 499.5 Mb/s, DQS/CLOCK at 249.75 Mb/s, Addr/CMD at 124.9 Mb/s.
- Video sources: YPbPr (1080i) plus CVBS sources with picture in picture (PiP) display.

Fig. 6 presents the measured near field strength distribution in the region of memory interfaces. Generally,

TABLE I. COMPARISON OF NEAR FIELD STRENGTHS FOR THE LCD-TV BOARD AT THE OPERATING AND HARMONIC FREQUENCIES OF DDR SDRAM AT LOCATION  $(x, y, z) = (127 \text{ mm}, 150 \text{ mm}, 145.5 \text{ mm})$

PCB type \ Freq. (MHz)	125.1	250.2	374.4	499.5	624.6	749.7	873.9	999.0
Model-A in dB( $\mu\text{V}/\text{m}$ )	95.6	100.9	84.6	93.9	72.2	77.7	75.1	78.6
Model-B in dB( $\mu\text{V}/\text{m}$ )	94.1	98.3	83.4	91.1	70.0	73.8	75.4	76.5
Improvement in Model B	1.5	2.6	1.2	2.8	2.2	3.9	-0.3	2.1

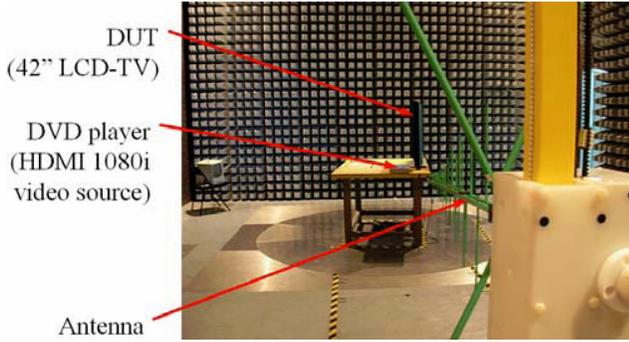


Figure 7. FCC Class-B (at 3 meters) radiation measurement of LCD-TV system in the  $9\text{m} \times 6\text{m} \times 6\text{m}$  semi-anechoic chamber.

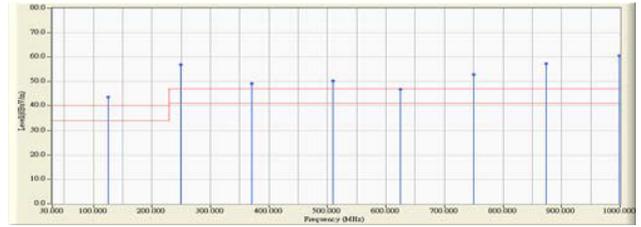
Model-A produces more deep red areas than Model-B in the distribution plots. By analyzing the results from TABLE I, we observe that Model-B has weaker field strength from 1.2 dB to 3.9 dB than Model-A does except the strength at 873.9 MHz when the probe is at location  $(x, y, z) = (127 \text{ mm}, 150 \text{ mm}, 145.5 \text{ mm})$ . As a result, Model-B with the solid ground plane is helpful to reduce the field strength.

### B. Far Field Radiation

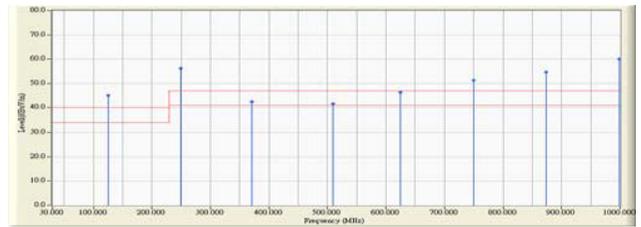
To further verify the proposed PCB design (Model-B) with less electromagnetic radiation, the measurement of far field radiation was done in the  $9\text{m} \times 6\text{m} \times 6\text{m}$  semi-anechoic chamber based on the IEEE standard ANSI C63.4-2003 [10]. Fig. 7 shows the equipment under test (EUT) connects to a 42" widescreen ultra extended graphics array (WUXGA,  $1920 \times 1200$  pixels) TFT LCD through a low-voltage differential signaling (LVDS) cable. The video source was high-definition multimedia interface (HDMI) 1080i from the DVD player. The sweep frequencies were from 30 MHz to 1 GHz. Fig. 8 demonstrates the measured far field radiation of horizontal and vertical polarization in the LCD-TV system at the operating and harmonic frequencies of DDR SDRAM. By comparing these results in TABLE II, we find that Model-B achieves less electromagnetic radiation from 0.36 dB to 8.65 dB than Model-A except the frequencies at 124.9 MHz in horizontal polarization and 370.3 MHz in vertical polarization. We can conclude that the high-speed traces with the solid reference plane induce less electromagnetic radiation.

TABLE II. COMPARISON OF FAR FIELD STRENGTHS OF HORIZONTAL AND VERTICAL POLARIZATIONS IN THE LCD-TV SYSTEM AT THE OPERATING AND HARMONIC FREQUENCIES OF DDR SDRAM

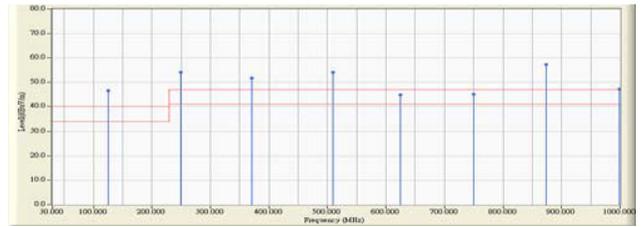
Freq. (MHz)	Limit dB( $\mu\text{V}/\text{m}$ )	Horizontal/Vertical Polarization Measurement, dB( $\mu\text{V}/\text{m}$ )		
		Model-A	Model-B	Improvement in Model-B
124.9	40	43.62/46.62	44.99/45.45	-1.37/1.17
249.7	47	56.91/54.03	56.11/51.37	0.80/2.66
370.3	47	49.19/51.67	42.55/52.82	6.64/-1.15
509.1	47	50.19/54.08	41.54/49.95	8.65/4.13
624.4	47	46.77/44.89	46.30/40.17	0.47/4.72
749.3	47	52.76/45.14	51.35/44.11	1.41/1.03
874.1	47	57.23/57.23	54.69/56.36	2.54/0.87
999.0	47	60.38/47.25	60.02/43.45	0.36/3.80



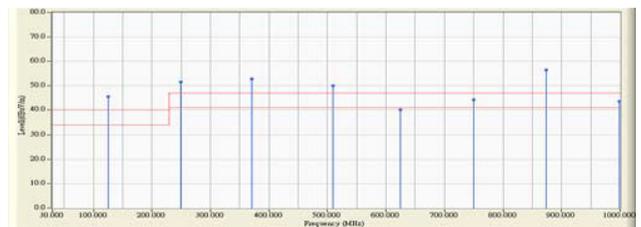
(a)



(b)



(c)



(d)

Figure 8. Measured far field radiation in the LCD-TV system at the operating and harmonic frequencies of DDR SDRAM: Model-A with horizontal polarization (a), Model-B with horizontal polarization (b), Model-A with vertical polarization (c), and Model-B with vertical polarization (d).

## V. CONCLUSIONS

By making use of the zero ohm resistors to connect the power nets between the LDO regulator and the power pins in the DDR SDRAM, our proposed PCB design can avoid the split reference planes for high-speed traces routing in the memory interfaces with negligible increment of system cost. We verified this design with low cost PCB, while maintain the good signal quality and less electromagnetic radiation from 0.36 dB to 8.65 dB. That can reduce the time for EMI troubleshooting for those systems including the DDR SDRAM in the 2-layer PCB. The similar approaches to reduce EMI radiation may be applied to the DDR2 and DDR3 traces routing in 2-layer PCB to avoid slotted ground layers. Those will be verified in the near future.

## ACKNOWLEDGMENT

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