SOLDERING TECHNOLOGY FOR AREA ARRAY PACKAGES

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ABSTRACT
Soldering is the primary interconnection technology for area array packages. Methods for solder bumping for area array packages can be categorized as follows: (1) build-up process, (2) liquid solder transfer, (3) solid solder transfer, and (4) solder paste bumping. The first group includes both evaporation and electroplating processes, while the second group includes meniscus bumping and solder jetting. The third group includes wire bumping, sphere welding, decal solder transfer, tacky dot solder transfer, integrated preform, and pick-and-place solder transfer processes, with the last one (pick & place solder transfer) being the current prevailing option. Solder paste bumping exhibits great potential to reduce bumping costs dramatically, and includes the print-detach-reflow, print-reflow-detach, and dispense approaches. For an area array package attachment process, depending on the type of packaging, either flux, fluxless soldering or solder paste printing may be used as the attachment medium. Although area array packaging generally offers a robust process, attention should be paid to reduce defects such as delamination, misalignment, elongated joint, voiding, bridging, opens, cracking, poor wetting and various attachment interactions.

Key words: solder, soldering, area array package, flip chip, BGA, CSP, sphere, bumping, paste, flux, fluxless.

INTRODUCTION
Packaging trends throughout the history of electronics manufacturing have moved progressively toward the characteristics of being smaller, faster, lighter, and cheaper. From surface mount technology (SMT), packages evolved further to the peripheral fine pitch lead approach. This development ran into limitations quickly at approximately 12-16 mil pitch applications. To address this challenge, area array packaging technology emerged, offering nearly a quantum leap over the peripheral packaging technology. From flip chips and chip scale packages to ball grid arrays, area array packaging now provides great benefits at both the IC and component levels. Figure 1 shows the increasingly wide variety of chip scale packages utilizing area array technologies.

Solder and soldering are by far the preferred approaches to interconnecting area array packages. This is especially true for the second level assembly stage; consequently, it is important to understand the nature, options, and limitation of both solders and soldering categories in order to successfully implement area array packaging technology.

SOLDER CRITERIA
The choice of solder alloys is determined by the requirements of both process and reliability. Initially, besides meeting the solder wetting requirement, the solder chosen should be able to maintain its physical and mechanical integrity during subsequent processing. In this manner, at the end of the packaging and assembly processes, the solder joints formed initially will not be altered or ruined. The second criterion for choosing a solder alloy is reliability. Since solder joints need to survive the challenges of service life, the alloy should have sufficient fatigue resistance as well as sufficient standoff to absorb the thermal expansion coefficient (CTE) differences between parts. The former dictates that the solder should have appropriate mechanical properties in terms of shear, tensile, creep, and fatigue. The latter requires that solder joint height should be maintained above a certain value.

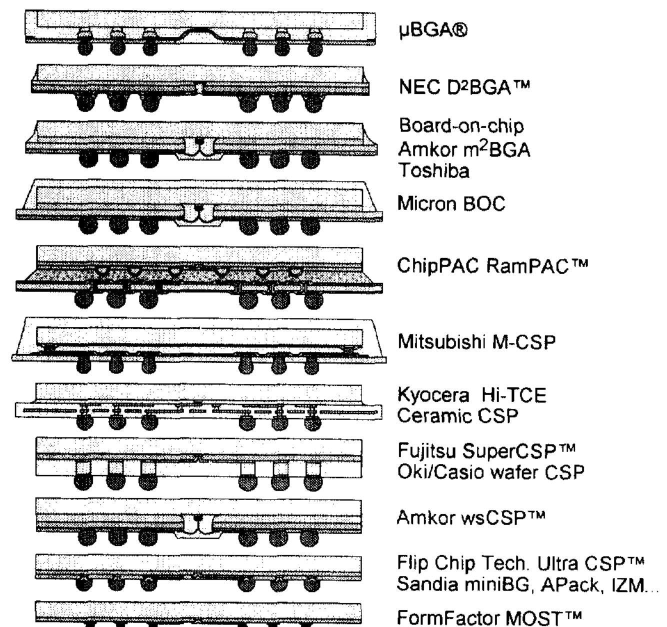


Figure 1 Various array packages [26].

This can be achieved through either solder surface tension (in the case of light components), or (in the case of heavy components) when High melting point solder functions as a spacer during the soldering process.

For area array packaging, interconnecting solder materials are usually introduced at two stages. The first is a predeposit of solder onto the packaging, usually accomplished through solder bumping. The solder bumped package is then mounted onto the next level of packaging through soldering. The soldering process here may or may not need the introduction of additional solder materials. The additional solder materials may or may not be the same solder alloy as the solder bump on the packaging. When additional solder materials are needed, they are often introduced through either solder coating onto the next level of packaging, or through solder paste deposition as a bonding medium.

SOLDER ALLOY ATTACH METHODS

1. Alloys Used in Flip Chip Solder Bumping and Soldering

For Flip Chip in Component (FCIP), the solders utilized for flip chip solder bumping and joining normally must have high melting points, such as 97Pb3Sn or 95Pb5Sn,. This ensures that the solder joints will not remelt during subsequent packaging and assembly processes using eutectic 63Sn37Pb solders. For direct chip attachment (DCA) or flip chip on board (FCOB) applications, the solders utilized for flip chip bumping as well as solder coating on the next level packaging often are eutectic or near-eutectic tin-lead solders. In some instances, In-Pb solders, such as 81Pb19In, are chosen for either better fatigue performance or better compatibility with Ni/Au substrate finish An Au-Sn alloy system is also used for some fluxless flip chip assembly applications, with a eutectic 80Au20Sn cap on top of an Au bump or Ni bump base. In the case of wire-bumping applications, the 97.5Sn2.5Ag alloy has been used as an option.

2. Alloys Used in BGA and CSP Solder Bumping and Soldering

For heavy components such as ceramic column grid array (CCGA) or ceramic ball grid array (CBGA) devices, the solder used for either column or ball is typically 90Pb10Sn. The column is mounted onto the area array package via either casting or 63Sn37Pb solder joining. For CBGA, the 90Pb10Sn solder ball is typically mounted via 63Sn37Pb solder paste soldering. The high melting point of 90Pb10Sn solder ensures the required standoff of CCGA or CBGA on PCBs during board level soldering assembly using eutectic 63Sn37Pb or 62Sn36Pb2Ag solders. For light components such as plastic ball grid array (PBGA) devices, the components are bumped with 63Sn37Pb or 62Sn36Pb2Ag, and soldered onto the PCB either with flux alone, or with solder pastes using similar alloy systems. In the instance of chip scale packages (CSPs), the alloys used are similar to that of PBGAs. However, the use of solder paste rather than flux alone, for board level assembly, is recommended.

3. Lead-Free Solders

Due to the toxicity of Pb, there has been an effort to eliminate Pb from solders. Through various concerted efforts worldwide, some good and favored Pb-free alternatives have been identified, although none can serve as a 100% drop-in replacement for existing solders. The favorable Pb-free solder systems comprise primarily alloys of Sn with Ag, Bi, Cu, Sb, In, or Zn, as shown in Table 1.

Table 1 Examples of lead-free solders

Melting Temperature Range (°C)	Alloy
227	99.3Sn0.7Cu
221	96.5Sn3.5Ag
221 - 226	98Sn2Ag
205 - 213	93.5Sn3.5Ag3Bi
207 - 212	90.5Sn7.5Bi2Ag
200 - 216	91.8Sn3.4Ag4.8Bi
226 - 228	97Sn2Cu0.8Sb0.2Ag
213 - 218	96.2Sn2.5Ag0.8Cu0.5Sb
232 – 240	95Sn5Sb
189 - 199	89Sn8Zn3Bi
175 - 186	77.2Sn20In2.8Ag
138	58Bi42Sn
217 - 219	95.5Sn4Ag0.5Cu
216 - 218	93.6Sn4.7Ag1.7Cu
217 - 219	95.5Sn3.8Ag0.7Cu
217 - 218	96.3Sn3.2Ag0.5Cu
217 - 219	95Sn4Ag1Cu

These alloys may serve as substitutes for eutectic Sn-Pb solders in area array packages. As to the substitutes for high melting temperature solders, nothing has been developed yet. However, it should be kept in mind that most of the data generated are either material properties or performance in typical SMT applications. Direct data for Pb-free solders used in area array packaging still needs to be generated.

SOLDER BUMPING AND CHALLENGES

Solder bumping techniques for area array packaging can be categorized in four major groups, as shown below:

1. Build-up Process

The solder bump is built up by depositing solder gradually through either a dry process, such as evaporation, or a wet process, such as electroplating.

Evaporation Bumping

This is a dry solder build-up process, typically used for wafer bumping. In the case of the IBM C4 (controlled collapse chip connection) process [1], the solder materials used are 97Pb3Sn or 95Pb5Sn. At first, a molybdenum metal mask is aligned to the bond pads on the wafer and

clamped . The underbump metal (UBM) is deposited through evaporation onto Al pads by (1) depositing 0.15μ Cr and 0.15μ phased 50/50 CrCu layer as adhesion/barrier layer, (2) depositing 1μ Cu as wetting layer, (3) depositing 0.15μ Au as oxidation barrier. The solder with a known composition and volume is then deposited through evaporation also onto the UBM surface. The molybdenum metal mask is then removed, and the solder bump formed is often reflowed in order to fuse the solder.

Motorola has developed an E-3 (Evaporated Extended Eutectic) wafer bumping process (see Figure 2). Here E-3 bumps are formed by evaporative methods, producing a bump with a pure Pb column and a pure Sn tip. It is not reflowed prior to die attachment. [2]

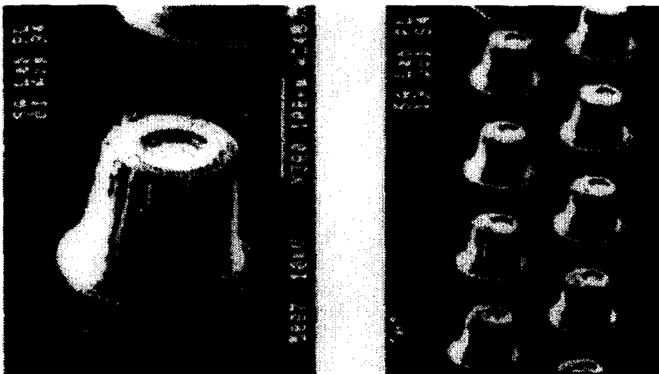


Figure 2 E-3 solder bumps [2].

In general, the evaporation process is adequate for coarse pitch and low I/O device, due to the constraints of metal mask technology, although 100μ diameter bumps on a 250μ pitch have been demonstrated. The quality of the solder composition and volume is very high. However, the high cost of the evaporation process is of concern.

Electroplating Bumping

Electroplating bumping can be regarded as a wet solder build-up process. At this stage, electroplating may be the most commonly used process for wafer bumping. Again, the solder alloys deposited are typically Sn-Pb systems. At first, the whole wafer is metallized with a seed metal [3]. It is than patterned with photoresist with the desired bumping location exposed. A static or pulsed current is then applied through the plating bath with the wafer as the cathode. After plating, the photoresist is stripped and the seed metal etched away. The solder deposited is then reflowed with the use of flux to form solder bumps.

It has been observed that some of the neighboring solder bumps formed may vary in size after reflow, even though the solder deposits are even in dimension prior to reflow. This phenomenon is more noticeable at higher reflow temperatures. Although the mechanism responsible for this phenomenon is not clear yet, it has been suggested that this variation in solder volume from bumps to bumps may be caused by solder robbing. On reflow, the outgassing of flux or impurities in the plated solder may have disrupted the molten solder domes, and consequently resulted in contact between neighboring solder deposits. This transit contact between deformed molten solder domes can easily result in solder robbing, hence forming uneven solder volumes in neighboring bumps.

2. Liquid Solder Transfer Process

In this process. the solder bump is formed by transferring liquid solder onto the wafer metal base either by solder dipping, such as meniscus bumping, or by liquid solder dispensing, such as solder jetting.

Meniscus Bumping

This is a solder dipping process [4] developed by Fraunhofer-Institute as a low cost alternative to conventional processes in cases where - as for flip chip on flex - only a relatively thin solder layer is needed. The wafer level bumping is based on the deposition of electroless Ni as a wettable UBM. Besides the possible cost advantage of this process, a very high uniformity of the layer and a near hermetic sealing of the Al-pad is claimed. Then, a solder layer - 80Au20Sn is chosen, in this case for its high reliability and its high melting point - and is applied by a well-controlled dipping technique. A mean bump height of 32 μ with a variation of ± 5 μ (Ni bump: 15 μ) is desired. This is reported to be sufficient for the bonding process (laser based Fiber Push Connection technology, FPC) on the flexible substrate applied here.

The solder bumps formed through this process can be soldered onto the flex through FPC technology. In this instance, an adhesive is dispensed onto the flip chip bump side, followed by placing a three-layer flexible substrate (a copper layer sandwiched between polyimide layers) on top of the flip chip bump. During the FPC process, the fiber maintains the bond force while the laser pulse guided through the fiber heats the contact zone. The temperature generated results in the emission of IR radiation, which is measured by a detector for in situ temperature control, thus avoiding overheating the flex. The FPC method allows bonding through the polymer film due to the low absorption of the flex at the wavelength provided by the Nd:YAG laser (1064 nm). The copper leads are thus selectively heated close to the interconnection area.

Since FPC technology utilizes sequential soldering process instead of mass soldering process, the inherent low rate of throughput can be of concern.

Solder Jet Bumping

Solder jetting is a process whereby a molten solder droplet is ejected from an orifice with the use of a driving force. At this stage, the most commonly used and also the most successful driving mechanism is piezoelectric force, as exemplified in Figure 3.

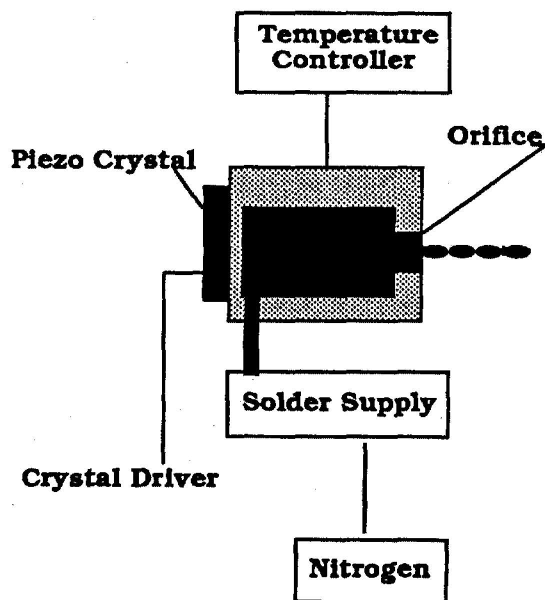


Figure 3 The piezoelectric crystal exerts a pulsing mechanical force to break up the solder jet stream to form solder droplets.

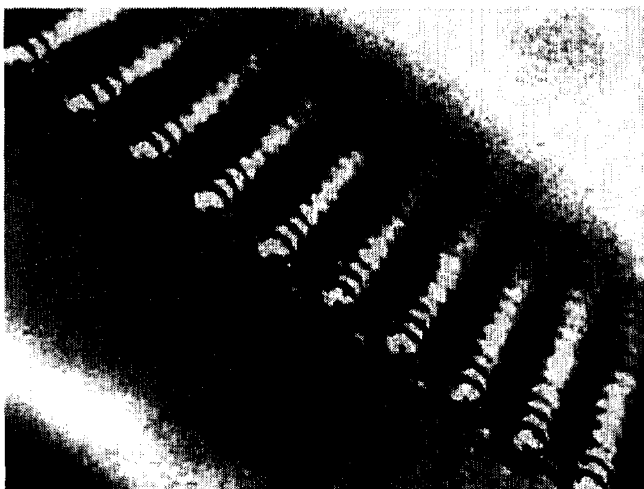


Figure 4 Solder bumps formed with Sandia solder jetting process [5].

Solder jetting used for BGA solder bumping has been demonstrated by Sandia National Laboratories [5], with results demonstrated by Figure 4. As mentioned earlier, the driving mechanism used is piezoelectric force. Using a graphite plate with 20x20 apertures matching that of a BGA pads, the bumping of 400 pads can be accomplished with one single shot. The BGA substrate is positioned at 0.100 inch under the orifice plate, aligned with the holes, and heated to 180°C to aid the wetting. The most consistent solder droplet with diameter 30 mil was produced at 205°C with 14 mil orifice. Higher temperature results in a larger solder droplet, due to a lower solder viscosity.

Other mechanisms have also been attempted, such as electromagnetic driving force reported by IBM [6], as shown in Figure 5. This IBM design, known as Micro Dynamic Solder Pump (MDSP), utilizes electric current pulse and magnetic field to induce a driving force exerted onto the molten solder and result in controlled solder droplets with dimension down to 0.004 inch. This driving mechanism involves no mechanical movement, hence eliminated any possible mechanical wearing issue.

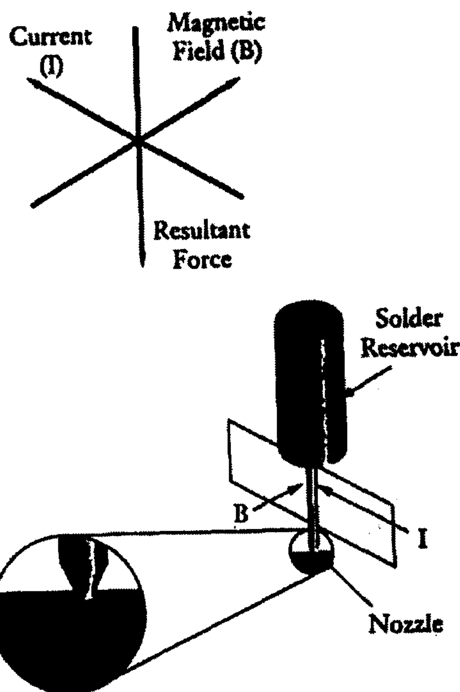


Figure 5 Schematic of Micro Dynamic Solder Pump [6].

For a drop-on-demand wafer bumping process developed by MPM and Microfab [7], the molten solder droplet is directly ejected onto a wafer pad with an Au surface finish. The machine can deposit Sn63 solder droplets (100-150 ± 10 μ size). During jetting, the wafer stage moves around, with the jetting area flooded with nitrogen. The solder solidifies immediately upon landing.

The limitation of this jetting technology on wafer bumping is at approximately 3 mil spacing. The solder bump formed has no metallurgical bonding formation with the pad, as evidenced by the lack of intermetallics, and apparently adheres to the pad mainly by physical force. However, a true solder wetting can be developed by reflowing the bumped wafer.

The solder jetting may have the greatest potential as a low cost wafer bumping process. It has been claimed that this process may cost $16/wafer for solder bumping, versus $50-100/wafer for some plating bumping processes. However, the throughput of this process is still fairly low, as reflected by the maximum jetting speed of 250

drops/sec. In addition, the consistency of bump size also appears to be an issue. Perhaps due to the challenging nature, recently some further developmental work on this approach has been discontinued.

3. Solid Solder Transfer Processes

The transferring of a solid solder mass to the pad area forms the defined solder bumps. This transferring process can be wire bumping, sphere welding, decal solder transfer, tacky dot solder transfer, pick-and-place solder transfer, and integrated preform, as exemplified below:

Wire Bumping

Wire bumping is similar to wire bonding in that a solder wire, such as 97.5Sn2.5Ag, can be bonded directly onto the aluminum bond pad using thermosonic energy. The solder stud formed then can be reflowed to form solder ball. The ball size and pitch limitations are determined by the diameter of solder wire and the thermosonic bonder's capability.

Sphere Welding

For TBGA, IBM Endicott has developed a solder bumping process using a fluxless welding approach, as shown in Figure 6. The 25 mil diameter 90Pb10Sn sphere is placed onto a thin nest with cup to hold the sphere in place. The TBGA tape with an Au-plated via is then placed on top of the spheres on the nest, followed by placing the setup under a welding machine. The welding tip is then lowered onto the tape via, and presses the via against the sphere underneath. If the welding tip traveling depth falls within the required spec, a current is then passed through the tip. This current will heat up the via Cu within few milliseconds to 600-700°C on the top side. The bottom side of the via is cooler, but is hot enough to melt down the top of the 90Pb10Sn sphere. The pressure on the via is maintained during the solder sphere melting stage to force the molten solder to not only wet to the bottom side of the pad (including the pad side edge, by forming $AuSn_4$ intermetallics), but also to wick up the via and emerge slightly from the top of it. Once the depth has advanced a pre-specified distance from the point before solder melting, the power is then cut off. The solder cools down rapidly, and resolidifies. During the welding process, the device holding stage moves around while the welding tip fixture remains stationary. The welding process throughput is approximately 7.5 bumps/sec.

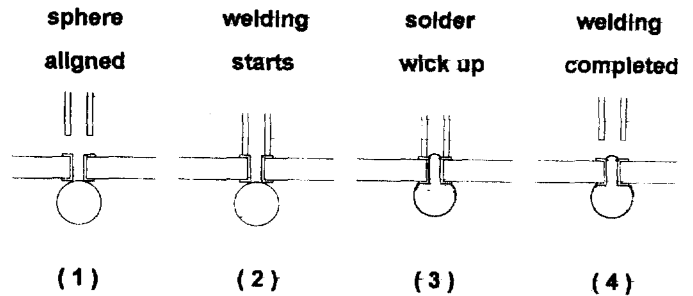


Figure 6 Sphere welding process for TBGA.

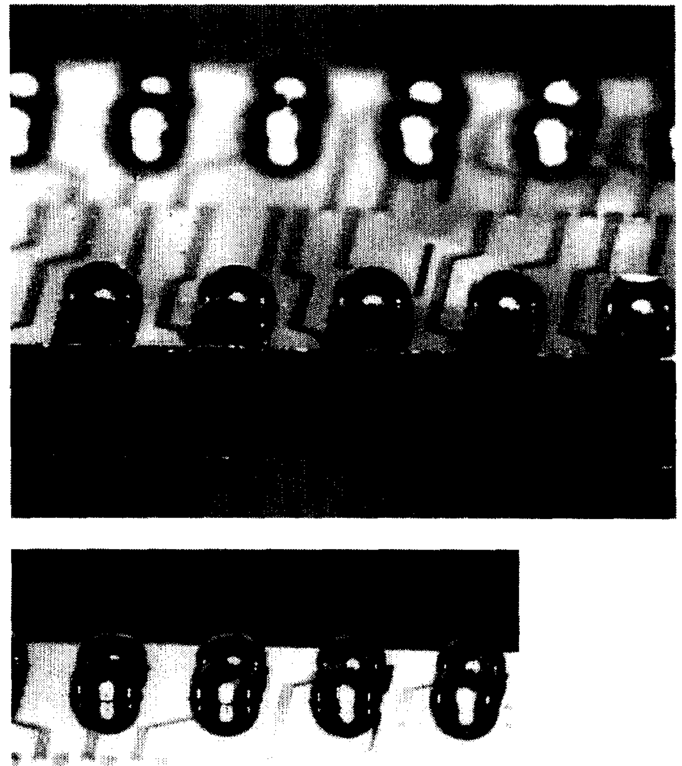


Figure 7 Spheres attached to distributed array utilizing Laser attach method.

This TBGA process can rework unwelded vias or underwelded vias. However, it can not rework an overwelded via. If there is an overwelded via, the whole TBGA tape has to be scrapped.

Laser Attachment

Laser solder reflow and attachment provides excellent results for CSP and extremely fine pitch devices, shown in Figure 7. The method utilizes a specialized placement / reflow head which drops a single preformed sphere on to the desired placement site. The patented placement head as seen in Figure 8 simultaneously holds the ball in exact position. A small ND: YAG laser simply heats each individual solder ball to reflow temperature in an inert

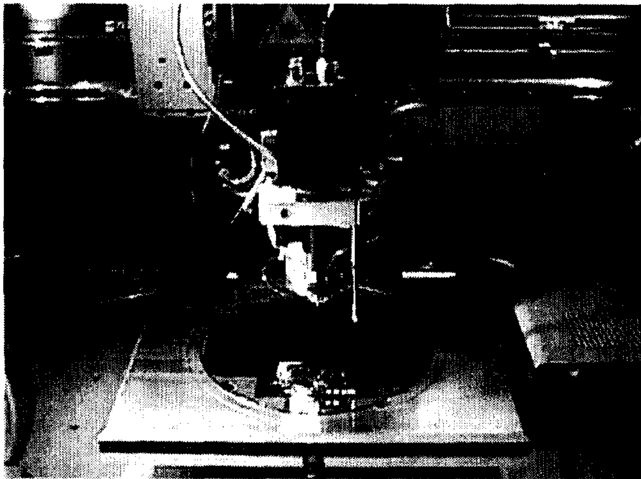


Figure 8 Laser attachment head courtesy Pac-Tech Industries.

environment typically of Nitrogen thereby eliminating the need for flux or flux processes. This process produces excellent results however, it can be a limiting factor if high throughput is desired [26].

Decal Solder Transfer

Decal Solder Transfer is a method reported to be simple, as well as effective for the addition of controlled amounts of eutectic solder to Flip Chip Attach (FCA) carrier pads or BGA pads (see Figure 9). In this process developed by IBM-Endicott [8,9], solder is plated onto a non-wettable decal substrate such as aluminum, and forms solder studs with a pattern matching that of a flip chip or BGA footprint pattern. This decal substrate, loaded with solder studs, is then placed on a fluxed wafer or BGA substrate, with each solder stud registered onto a metallized pad such as copper. This sandwiched assembly is then reflowed, followed by removal of the decal. The solder studs wet to the pad metallization and are detached from the decal substrate. The method, based on electroplated "non-wettable" substrates or decals, is a viable technique for chip attach and chip rework processes for card-on-board (COB) or BGA mounting applications.

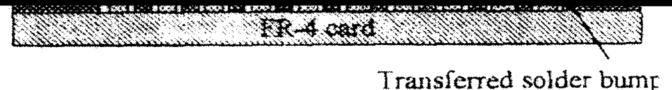


Figure 9 Schematic of decal solder transfer process [8,9]

Two important characteristics of the "nonwettable" substrate are the degree of wetting to the molten solder, and its planarity. If the substrate is wetted by the solder, the solder bumps often become ruptured upon removal of the decal. On the other hand, if the decal is warped, some of the solder studs may not contact the area array substrate pads, and hence may not be transferred to the pads.

Since this technique still requires the use of the solder plating process for decal solder deposition, its potential may be challenged by the direct electroplating solder bumping process for area array packaging.

Tacky Dot Solder Transfer

Du Pont developed an approach using tacky dots on polyimide film to transfer solder spheres for bumping CSP and flip chip [10,11]. The process involves the following steps: (1) preparing polyimide film with adhesive coating, and covering the adhesive coating with a Mylar cover sheet; (2) photoimaging the film to form the desired tacky dot pattern to match the CSP or flip chip pattern, with the tacky dot diameter being 20 to 30% of the sphere diameter; (3) peeling off the Mylar cover sheet; (4) pulling the polyimide film through a solder sphere bath to populate the tacky dots with spheres followed by full inspection; (5) placing the bumped film onto a flex stage typically used in the wafer dicing process; (6) cutting off the individual sheet; (7) mounting the bumped sheet onto a wafer printed with flux; and (8) either reflowing the solder so that the solder sphere wets to the wafer and detaches from the tape, followed by removal of the film, or UV curing the tacky dot to release the sphere, followed by inspecting the sphere on flux and then reflowing. The whole process may be about 1 wafer per minute, and has been demonstrated with wafers containing 29,000 bumps.

The target application is solder bumping the CSP or flip chip using small spheres. The spheres investigated range from 5 to 20 mil diameter, primarily of eutectic SnPb solder. However, peeling off the Mylar cover sheet from the adhesive layer tends to generate a static charge, and the static becomes a factor in handling those tiny spheres. In addition, an agitated solder sphere bath tends to oxidize the solder sphere surface, which further aggravates the sensitivity toward static. Therefore, the bottleneck is attaching the sphere to a tacky dot on polyimide film carrying some static charge, while at the same time achieving a high yield.

Pick-and-Place Solder Transfer

For BGA solder bumping, the most common process involves using a pick-and-place machine to transfer solder spheres to a BGA substrate predeposited with flux or solder paste, followed by reflow. The pick-and-place mechanisms utilized include (1) vacuum pick-and-place, and (2) gravity pick-and-place [12]. In the former, a sphere tray with a cavity pattern matching that of the BGA is connected to a sphere reservoir. The vacuum-regulated tray cavity is first loaded with spheres through a cycled-tilting process. Another vacuum fixture with a mirror cavity pattern is then placed near the top of the tray to pick up the spheres through gas-blow-ejection plus a vacuum-pick mechanism. The sphere is then ejected onto a BGA substrate pre-deposited with either tacky flux or solder paste. The BGA substrate loaded with spheres is then reflowed to complete the solder bumping process. In the gravity pick-and-place approach, no vacuum is involved. A revolving process is used to first load spheres onto a sphere tray, and subsequently transfer the spheres onto a BGA substrate pre-deposited with either tacky flux or solder paste, as shown in Figure 10. All sphere transferring processes rely on gravity alone. This is possible through the proper positioning of both tray and BGA substrate via the revolving process. The populated BGA substrate is then reflowed to complete the solder bumping process. As for wafer bumping, a prototype pick-and-place unit has been built, and it is reported that vacuum is not needed to pick up and transfer the tiny solder spheres.

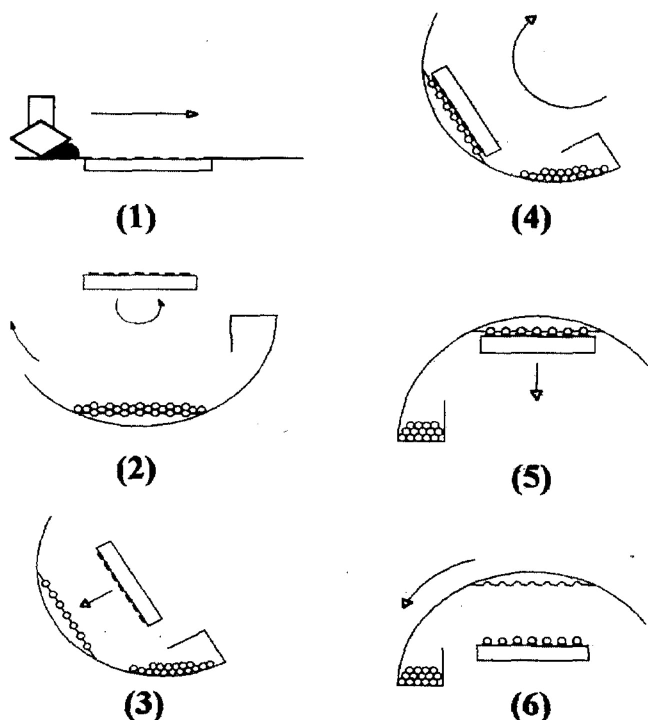


Figure 10 Gravity pick-and-place process, (1) print solder paste or flux onto BGA strip, (2) rotate BGA strip and sphere loader for proper alignment, excessive spheres being drained from sphere securing tray, (3) attach BGA strip to sphere on sphere securing tray, (4) rotate loader/BGA strip to allow BGA strip to face upward, (5) detach sphere-loaded BGA strip from loader, (6) rotate sphere loader to reload sphere securing tray with spheres.

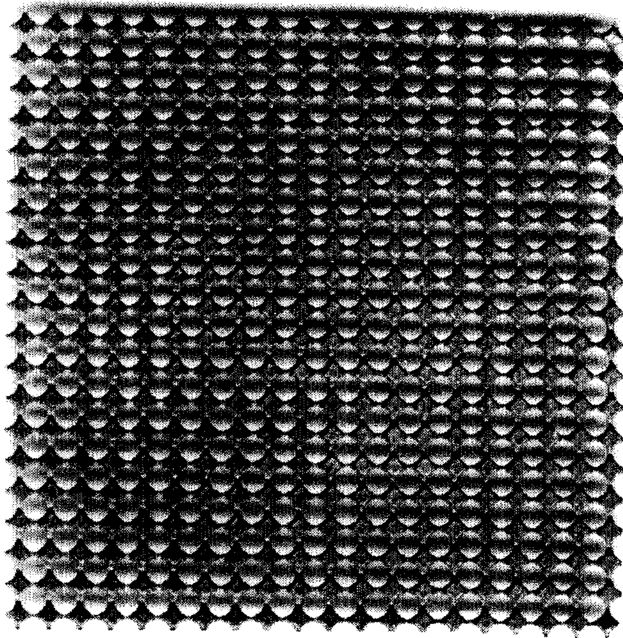
Both pick-and-place designs for BGA solder bumping involves rolling of solder spheres back and forth between the sphere tray and the reservoir. This inevitably oxidizes the solder sphere and may pose a soldering quality issue at a later stage. As for wafer bumping, there are at least two challenges facing the sphere placement approach. First of all, at sphere size or smaller than 4-5 mils, precision sphere dimension control, such as +/- 5% in diameter, becomes very difficult. Secondly, static becomes a factor in handling such tiny spheres.

A systematic study of the reflow bumping process has been conducted [13]. For a bumping process involving Sn62 or Sn63 spheres, the use of solder paste for sphere attachment produces excellent alignment results. When using fluxes for Sn62 or Sn63 sphere attachment, the defect rate increases with decreasing flux viscosity, solvent volatility, and pitch dimension; with increasing flux deposition thickness, activity, and pad diameter. For overall better yield, a solder paste with a long stencil life, good printability, and good solder ball performance should be the most promising eutectic sphere attachment material. For systems using pastes for 90Pb10Sn sphere attachment, no missing has been observed, and alignment improves with decreasing paste deposition thickness, solvent volatility, and increasing sphere solderability, flux activity, pad dimension, metal load, and pad solderability. Paste viscosity, pitch, and reflow profile have negligible effect on the 90Pb10Sn bumping yield using Sn63 solder paste.

Integrated Preform

The integrated preform is a patterned solder preform, as shown in Figure 11. The patterned preform has a sub-preform corresponding to each pad of the BGA land pattern, and all neighboring sub-preforms are interconnected with a thin solder link. Bumping with integrated preform can be achieved by placing the integrated preform on top of either flux or solder paste printed onto the BGA substrates. This approach has been reported by Indium Corporation of America [13] to be

promising. Reducing the thickness and width of the solder link is considered essential for achieving a high bumping success rate. In addition to alloy link matrices other preform designs include designs such as the SolderQuick™ paper matrix which has 63/37 spheres integrated into a paper matrix which is placed on the top of the designated BGA component, shown in Figure 12. The entire design is then reflowed. The final stages include the removal of the paper matrix by utilizing a DI water bath to both dissolve and remove the unwanted paper fixture. The method has been shown successful for components with I/O's exceeding 700. [27]



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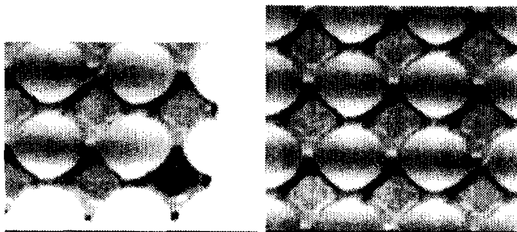

(2)

Figure 11 Integrated preform, (1) overall view, (2) close-up look.

4. Solder Paste Bumping

Solder bumping can also be accomplished with the use of solder paste alone. This approach becomes more and more attractive when the area array packaging becomes smaller and smaller, therefore the solder bumps become smaller and smaller. This is mainly due to cost. With the use of the sphere transfer approach, since the cost of the sphere remains the same regardless of sphere size, the cost per bump is accordingly steady as well, regardless of bump size. Conversely, the cost of solder paste is determined by its volume. Therefore, with decreasing bump size, the cost per solder bump will reduce significantly when employing the solder paste bumping approach. Processes of solder paste bumping include print-detach-reflow, print-reflow-detach, and dispense.

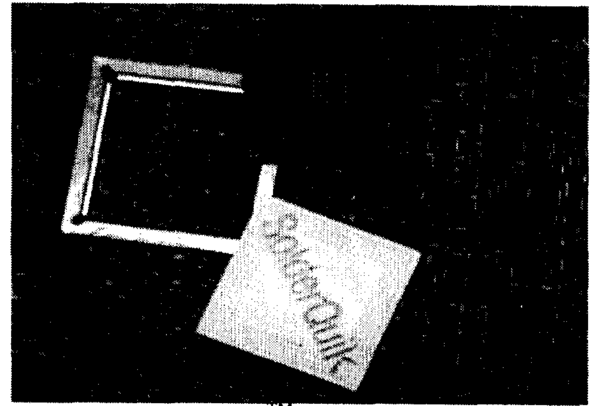

Figure 12 SolderQuick™ Integrated preform system.

Print-Detach-Reflow

Solder paste printing may be considered a viable low cost bumping process. The most desirable procedure is similar to the conventional surface mount process: print, detach the stencil, then reflow. It offers the greatest potential to cut the bumping cost markedly. However, in order to deliver sufficient solder volume to form an adequate bump height, the stencil aperture must be much larger than the pad dimension. This will be fine for peripheral pad design or staggered pad patterning. In both cases, an overprint can be tolerated without causing problems.

However, for full area array designs, the slumping of the overprinted solder paste will result in solder robbing at reflow, and consequently uneven solder bump size. The appropriate solder volume can also be achieved using a thick stencil instead of a large aperture. The potential problem here is typically poor paste release from the stencil aperture. Therefore, an easily releaseable solder paste is crucial for area-array BGA processes if a regular print-release process is desired for bumping with solder paste alone. In addition, the paste has to have a minimal slump performance in order to avoid solder robbing.

Furthermore, the solder should wet to the pad quickly during the coalescence so that the molten solder bead will not drift away from the pad. In general, it has been found that a pre-bake treatment, for instance, 100°C for 10 minutes in a forced air convection oven prior to reflow, is very helpful in reducing the bumping defect rate. After pre-bake, running the paste through a profile with a long and hot soaking zone, for example, 175°C for 2.5 minutes, also helps reduce the defect rate. Presumably this can promote diffusion between the base metal and solder powder, and consequently allow the solder paste glob to anchor to the

pad better, minimizing drift of the paste glob during spiking. BGA solder bumping with this process has been reported to be successful for pitch 1.0 and 1.5 mm [14].

Reducing pitch will necessitate the use of a finer solder powder. Although 25-45 μ powder size is adequate for BGA solder bumping, powder size less than 25 μ is desired for wafer bumping. The excessive oxide caused by the large surface area of solder powder requires a flux with high capacity to prevent void formation. Results from Fraunhofer Institute [15] for wafer bumping using solder paste with powder size 15-25 μ showed a bump height of 125-150 μ (standard deviation 4.5-5 μ) achieved for 300 μ pitch device, and 80-115 μ (standard deviation 5-5.5 μ) bump height achieved for 200 μ pitch devices.

Print-Reflow-Detach

The second alternative involves printing the paste onto the area array packaging with the use of a metal stencil, then reflowing the solder paste with the stencil left on, and afterward the removal of the stencil, followed by cleaning. This process does not require very stringent stencil release and non-slump performance of the solder paste. However, additional sets of stencils as well as the stencil-securing fixtures and stencil cleaning steps add cost to this process. In addition, the solder bumps formed may tilt toward one side in some instances. Tilted solder bumps are caused by surface tension. At reflow, the flux may wick up one corner between the aperture wall and the molten solder bump, due to its tendency to form a minimal exposed surface area. In the meantime, the molten solder would also like to minimize the exposed surface area by maximizing the interface area between flux and solder. As a result, the molten solder dome will tilt toward the flux-rich corner in the aperture well, and consequently solidify into a tilted solder bump. This tilted solder bump can be corrected by reflowing the solder again with the presence of flux after removal of the stencil.

IBM-Charlotte has developed a process combining both print-detach-reflow and print-reflow-detach techniques, as shown in Figure 13 [17]. Here a metal mask is mounted onto a BGA substrate and secured with magnets. This temporary mask-BGA package is then sent through a conventional solder paste printing process, using printer equipped with a stationary stencil. Thus, the paste is printed through the stationary stencil onto the mask-BGA package, which is then reflowed, followed by mask-removal, and cleaning. This design allows the solder paste volume control at deposition stage split between the stationary stencil and the metal mask, therefore avoids the challenge of paste release using a single thick stencil for solder paste volume delivery. In addition, it also avoids the challenge of reflowing solder paste in the presence of a large thermal mass due to the use of a thick metal mask when using print-reflow-detach process. This screen printing method was applied to the bump forming of CSP (chip size/scale package) with pitch from 0.3 to 0.8 mm [14]. However, it should be pointed out that some attempts in the industry to duplicate these results turned out to be unsuccessful.

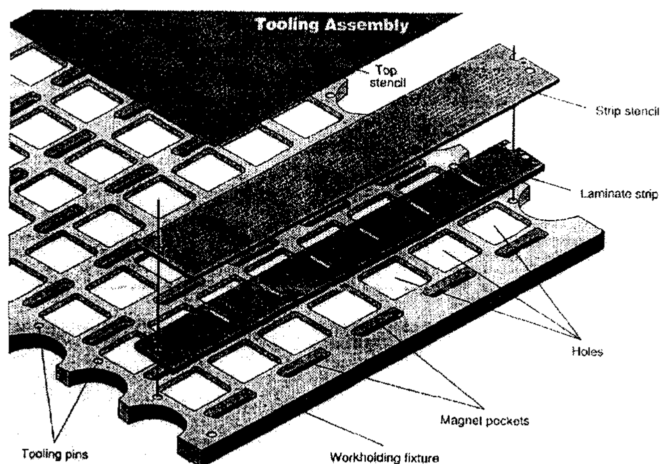

Figure 13 Solder bumping with solder paste alone, using combined print-detach-reflow and print-reflow-detach process [17].

Dispensing

BGA solder bumping may also be achieved with a solder paste dispensing approach. Although non-slump performance is still a required paste property, there is no issue related to an aperture non-clogging requirement. However, this approach may be more challenging than the printing approach. In order to deliver sufficient solder volume without slump, the paste volume dispensed should be low and the paste metal content should be high. The high metal content requirement directly conflicts with the low metal content requirement for a good dispensable paste. In addition, the paste volume control for a dispensing process is generally more difficult than that for a printing process. At this time, the dispensing approach remains of interest, but its feasibility remains to be proven.

ATTACHMENT AND CHALLENGES

Attachment Process

Attachment of area array packages onto printed circuit boards can be accomplished with a number of different techniques. The most common are the use of solder paste, or flux, or fluxless soldering, as described below.

Soldering With Flux Only

For flip chip in ceramic package (FCIP) applications, the solders used for flip chip solder bumping typically are high melting point alloys, such as 97Pb3Sn. The pad on ceramic package usually exhibits a Cu or Ni/Au surface finish. Conversely, flip chip on board (FCOB) involves flip chip with a 63Sn37Pb solder bump and a printed circuit board with 63Sn37Pb coating on the pads. In both cases, soldering for flip chip attachment is achieved with the use of flux only (see Figure 14). In one process, a low viscosity flux may be brushed or sprayed onto the substrate,

followed by flip chip placement and subsequently reflow under an inert atmosphere. In the second type of process, a relatively viscous and tacky flux is printed onto the substrate pads, followed by flip chip placement and reflow. A third way of applying flux is through a rotating drum process. Here a fixed thickness of a medium viscosity flux is constantly formed by a blade horizontally positioned on top of a rotating drum. The flux is first dispensed onto the rotating drum, with the thickness of flux film controlled by the clearance, which is usually around 2-3 mils, between the blade and the drum surface. The flip chip is then dipped into the flux film, with solder bumps partially immersed in the flux. This flip chip, with the bottom of the solder bumps coated with flux, is then placed onto the package substrate and followed by reflow.

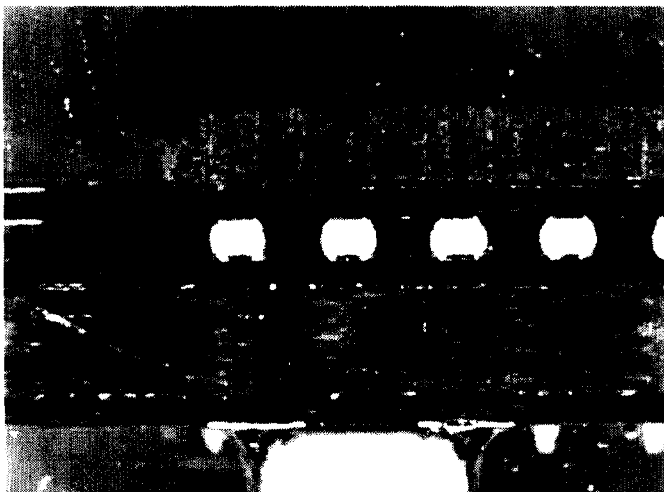

Figure 14 BGA Attached with flux only.

For a no-clean process, the flux residue level has a great impact on the subsequent underfill process. If the residue is not nearly zero, the underfill may have difficulty wicking through the underside of the flip chip to achieve uniform coating. In addition, the adhesion between underfill and both top and bottom sides of the solder joint layer may also be weakened by the flux residue, particularly in the presence of moisture.

For a PBGA attachment process, soldering with flux only may also be acceptable, particularly at the rework stage. The flux is often applied by brushing or dispensing.

Soldering With Solder Paste

For flip chip on board applications, solder paste may be used to mount the chip onto the PCB. However, the thin stencil required and the fine solder powder needed make it difficult to combine both flip chip paste printing and conventional surface mount paste printing into one stroke printing process. The stencil thickness needed for flip chip is about 2-3 mils, while that for conventional SMT applications is about 6 mils. The clearance between the flip chip footprint and the neighboring SM components footprint would dictate whether a proper stepdown stencil design is possible or not. The solder powder needed for flip chip paste printing is recommended to be no larger than 25 μ in diameter, while that for conventional SMT processing is about 25-45 μ. Therefore standardizing the solder paste material may compromise either performance or material cost.

BGA and CSP attachment onto PCBs is typically performed along with other SMT components. Accordingly, the primary process steps include printing solder paste (either Sn62 or Sn63), placing the component, followed by reflow. Thermal cycling results indicate that each BGA pad must have a certain minimum volume, V_{mo} of solder paste. The maximum amount of paste has a more flexible limit because the coarse pitch of BGA makes bridging less likely. The acceptable pad volumes are found to be in the approximate range $V_{mo} < V < 2V_{mo}$. For paste a printing, 5 to 7 mil stencil is acceptable for PBGA. One mil undersized on each side of the aperture is recommended to provide proper gasketing. For TBGAs and CBGAs, the solder volume per pad required is 4,800 to 10,000 cubic mils (7000 cubic mils nominal). The aperture diameter should be about 1.25 times of the solder pad diameter, and a stencil with 8 mil thickness is recommended. For CSP applications, more paste volume is more desirable for better reliability and better compensation for non-coplanarity. Stencil design with square apertures (with round corners) is recommended for CSP, for delivering higher paste volumes without bridging and solders paste aperture release problems.

Fluxless Soldering

Due to the potential adverse effect of flux residue on underfilling process and the resulting flip chip reliability concerns, one may want to evaluate a fluxless soldering process. With this process, developed by MCMS Inc. [28], a plasma dry soldering process which can be used not only on flip chip components but also on new and reworked PBGA package styles, shown in Figure 15 This process utilizes a plasma gas mixture consisting of oxygen and argon under moderate vacuum conditions to create a wettable interface. This process has been shown to be extremely effective for use during the re-balling process on macro scale PBGA's and for CBGA components. Further studies are currently being conducted on extremely high I/O flip chip devices on FR-4 substrates with Ni/Au lands to determine the extent at which these items may be stored in various environmental conditions. Other potential uses may include solder laden leaded chip-carriers and advanced application, which require zero flux residues for both high frequency, and Rf applications.

Figure 15 SEM of solder bumps utilizing fluxless soldering method [27].

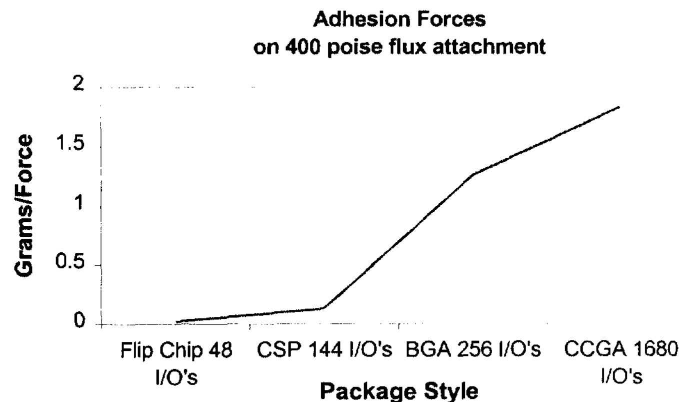

Fig. 16 The effect of "green" strength on various I/O devices [28].

1. Challenges for Flip Chip Soldering Attachment

Although flip chip offers a reasonably wide processing window, care should be taken to avoid unnecessary defects, and to insure that the maximum yield resolution is obtained after the process has been clearly defined. This can cause advanced process development to continue into the production cycle. Hopefully, by utilizing the practices and knowledge below one can enhance the process introduction and reduce development lead times.

Misalignment

When using flux only for flip chip attachment, [17], misalignment can be caused by (1) low flux tackiness; (2) the conveyor not being flat and stable; (3) an unbalanced oven gas flow; (4) poor support of the PCB during reflow; and (5) an inadequate reflow profile. Reflow under air has also been reported to aggravate misalignment problems It can also be assumed that the placement equipment is to blame for the majority of flip chip and even PBGA errors. It is critical that the mounting equipment use a stationary platform and that the placement heads are arranged a gantry system. Although this is not as critical with the larger I/O PBGA's and CGA's, it is most defiantly an issue with the small CSP and flip chip components. Part mass per attachment area site grows on a linear scale. Like wise the inertia momentum of parts per attachment site is also increased greatly. This causes the parts to "fly off" the land arrays when table velocity is introduced into the equation. As can be seen from Figure 16, low I/O components are a primary threat to this phenomenon. Manufactures have seen this happen with high mass DRAM devices and it is now turning full circle. One must be acutely aware of such issues well in advance of equipment purchases due to the fact that most often they cannot be returned.

Bridging

Bridging in flip chip attachment may be caused by movement of die during self-alignment [17]. In addition, the flux has been seen to cause random movement of the chips before they are finally drawn back to their normal position by the self-alignment force of the solder [18]. It may also be caused by too high a bond load force when using a bonder [19].

Open

Opens may be caused by misalignment and too high an oxygen level during reflow [17].

Poor Wetting

Poor wetting is often caused by too high an oxygen level during reflow, poor solderability of parts, and inadequate fluxing. For this reason it is important to use a reflow atmosphere with less than 180 ppm of oxygen. It is also obvious that the flux properties and the proper equipment selection be completed to insure that a smooth and transition free conveying process of the component array to the reflow chamber is achieved. Not only will this increase product yields but it will insure that the yield for this process is maximized.

Delamination

Delamination, as exemplified by Figure 17, is considered the first important failure mode of flip chip packaging [20]. For traditional underfilled (highly filled) flip chip packages, delamination between the passivation and underfill is more critical. Although the exact failure modes are not fully understood yet, inadequate fluxes or soldering process often are considered the causes of poor underfill performance. For instance, too much of flux residue can result in poor underfill flowing and poor underfill bonding. For the reflowable underfills (typically has no filler content), the fracture occurs through the solder interconnect near the substrate surface.

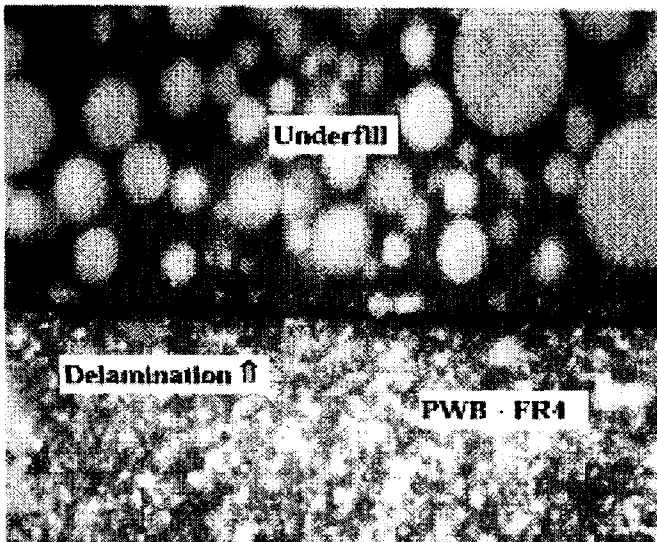

Figure 17 Delamination near the board side [22].

Cracking

Cracking is reported to be the second most important failure mode, including die cracking, under bump cracking, underfill cracking, and substrate PTH/microvia cracking [20]. Cracking in solder joints, as shown in Figure 18, has also been reported in fluxless soldering [18], and could be attributed to the entrapment of oxide within the joints. This is a particularly hard item to pin down and for the assembler may be impossible. It is important to remember that is critical that an extensive engineering evaluation be conducted before a specific underfill is selected. This may not alleviate the common problems of CTE mismatch. However, it does improve the odds of having a verified process which is infinitely more reliable. It is important that this process be designed around the specific result/goal for the project. It is very chancey to assume that process variables (at all levels of interaction) behave equally through time and product life cycles.

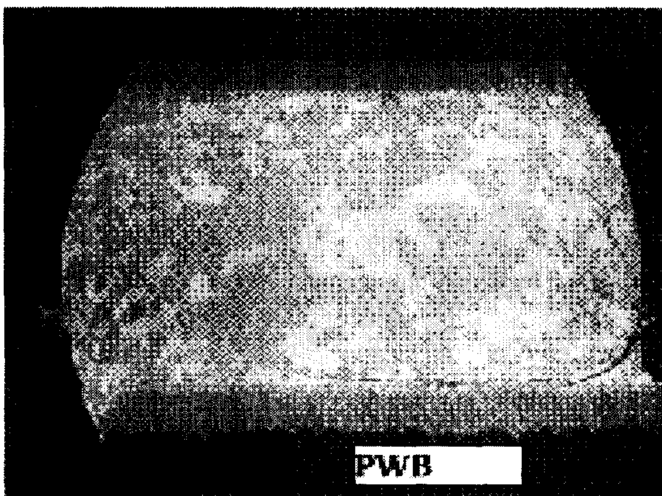

Figure 18 Crack in eutectic SnPb solder joint of flip chip [22].

3. Challenges for BGA Attachment

Following are the defects commonly encountered during the BGA attachment process.

Misalignment

Misalignment with BGA's as with other J-leaded components is caused by misplacement (see Figure 15). However, self-alignment of packages allows 40 –50% linear offset prior to reflow [21], if all other paste parameters are kept consistent. However slight misalignment of larger array packages such as the IBM CCGA package can cause deleterious reliability issues in long life applications. This is shown in Figure 19.

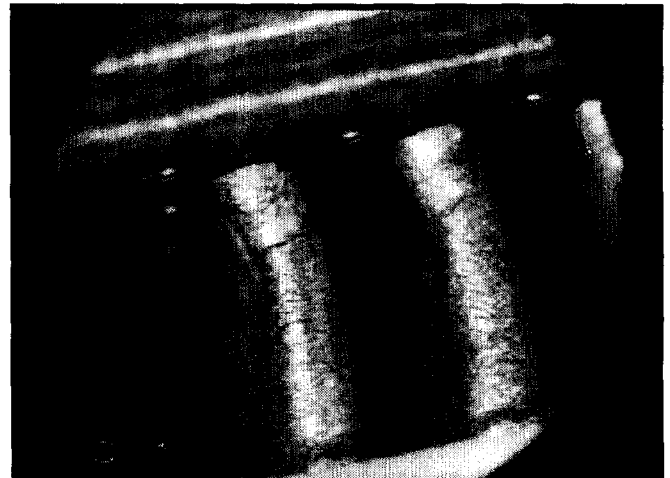
Figure 19 Off alignment columns showing deleterious crack propogation

Delamination

Delamination is a common problem in FR-4 and BT laminated devices, which are either undermolded or transfer molded encapsulation techniques [22], The delamination phenomenon is most commonly caused by the slow long-term moisture absorption by the PBGA, and can be prevented by minimizing exposure time of the PBGA to a humid environment, or by pre-baking the components. The slightly hygroscopic laminate materials causes the slow absorption of moisture over a long period of time. A bake under the right temperature profile will reduce 80% of the moisture concentration in the first few hours of the process. The remaining moisture will take an extended amount of time to dry out. The exponential drying curve can be used as a guideline for handling baking of components. This behavior, however., does not take into account the encapsulation material of the components itself. A recommended bake profile should be received from the manufacture to insure component integrity.

This moisture pick up issue, however, can be avoided by the utilization of proper packaging and storage techniques. A good recommendation is to insure that parts are stored in vacuum-sealed moisture barrier bags which will not be opened until placement. Another and highly successful method is the use on nitrogen cabinets. These cabinets are designed to provide a low level nitrogen purge capable of keeping moisture concentration levels to almost zero. This also enhances flexibility with storage and transport issues.

Poor Wetting

Poor wetting may occur more frequently when high lead content solders are involved. This is mainly due to the poor wettability of lead oxides. Use of inert reflow atmosphere, such as nitrogen, can be a shortcut in providing a better wetting.

Voiding

Voiding in BGA assembly using Sn63 solder bumps is primarily introduced at the board-level assembly stage. On pretinned PCBs, voiding of BGA joints increases with increasing solvent volatility, metal content, and reflow temperature, and with decreasing powder size. This can be explained by a viscosity dictated flux-exclusion-rate model. In this model, a higher viscosity in the fluxing medium at reflow temperature could hinder the exclusion of flux from the interior of molten solder, and thereby increase the incidence of outgassing due to the higher volume of entrapped flux. This would consequently result in a higher incidence of voiding in BGA assembly. Flux activity and reflow atmosphere appear to have negligible effect on voiding when the solderability of the immobile metallization is not a concern. An increase in void content is accompanied by an increase in the fraction of large voids. This suggests that, similar to voiding phenomena in the SMT process, factors causing voiding in BGA assembly will have an even greater impact on joint reliability than shown by total-void-volume analysis results [23].

Voiding also tends to occur more frequently in BGA joints when soldered onto vias in pads. This can be attributed to the outgassing of flux entrapped in the via. Similar phenomena can also be observed in BGA joints soldered onto microvias. With via-in-pads, the voids typically are caused by flux outgassing, as shown in Figure 20 (1). However, the voids occasionally can be caused by outgassing of the PCB through the porous wall of via barrel of which plating quality is poor (see Figure 20 (2)). Problems like this may be remedied by pre-baking the boards prior to reflow [24] as a short term solution.

Bridging

Excessive amounts of solder paste, or poorly printed paste, often result in bridging. The open time of solder paste can also affect the bridging performance. It has been seen that high humidity and high temperatures can result in paste thickening, therefore reduce the slumping and consequently the bridging. For this reason it is important that this be taken into account. During reflow, a slow ramp up rate is desired in order to minimize the hot slump [25] and bridging. In some instances, manual handling of components during soldering may also cause bridging. It is also extremely important to keep all screen apertures clean and in good condition. There is no engineering solution for a poorly made or designed solder paste stencil. It is therefore important to put in the time necessary to design apertures and foil combinations which best suit the specific needs of the product. This can be a daunting task when hundreds possibly thousands of different products are introduced through out the manufacturing environment.

Opens

Opens may be caused by insufficient solder, poor coplanarity of component or board, poor solderability of pads, or a missing solder bump. However, sometimes opens result from solder ball detachment from the pad, and can be attributed to a mismatch in TCE between BGA and PCB or too much stress introduced due to an inadequate soldering profile. This can be prevented and better yet inspected for after the reflow cycle. The use of 2 and 3 dimensional x-ray techniques has rapidly increased in the assembly industry. The ability of a particular piece of equipment should be verified. In most situations the goal for these products is to provide visual queues for such deleterious deformities such as a missing or poorly shaped solder mass.

Elongated Joints

In some instances, the PBGA may be warped, and the peripheral solder joints are stretched longer than the center joints The stretched joints display a rough surface, and often exhibit some microvoids, particularly near the board surface. The warpage is believed to be caused by mismatch in the TCE of the PBGA molding compound and the PBGA substrate, with the molding compound having a higher TCE than the PBGA substrate. When the package begins to cool down, warpage ensues. The warpage rate should be fairly significant at temperatures whereby the solid solder is still fairly soft and malleable. Therefore, the center joints are compressed to a shorter height and the edge joints are cold-drawn to a taller height. The microvoiding and surface fracture phenomena are probably caused by cold-drawing. Under highly tension-strained conditions, the solder begins to deform and microvoids start to develop, presumably between grain boundaries. The surface under high tension-strain condition also can exhibit a ruptured texture. These phenomena are expected to be more profound near the board surface where the solder cool down is slower [24].

Another cause of joint geometry anomalies is easily prevented with the proper Design For Manufacturing (DFM) techniques. As seen in Figure 21 the pads are not properly designed for the round solder spheres being attached. Although this is not a common problem, adequate communication between the customer designs and the manufacturing facilities often can prevent a

majority of such issues. It is important to remember that during engineering qualifications, it is common to use cards, which may not be inherently designed, for the specific component and this is entirely acceptable. However, under engineering qualification conditions it is desirable to experiment with these new design formulations.

Among the defects described above, misalignment, delamination, and elongated joint may be considered problems caused by inadequate handling or inadequate packaging materials, while voiding, opens, poor wetting, and bridging may be considered mainly soldering related .

SUMMARY

Soldering is the primary interconnection technology for area array packages. Methods for solder bumping for area array packages can be categorized as follows: (1) build-up process, (2) liquid solder transfer, (3) solid solder transfer, and (4) solder paste bumping. The first group includes both evaporation and electroplating processes, while the second group includes meniscus bumping and solder jetting. The third group includes wire bumping, sphere welding, decal solder transfer, tacky dot solder transfer, integrated preform, and pick-and-place solder transfer processes, with the last one (pick & place solder transfer) being the current prevailing option. Solder paste bumping exhibits great potential to reduce bumping costs dramatically, and includes the print-detach-reflow, print-reflow-detach, and dispense approaches. For area array package attachment process, depending on the type of packaging, either flux, flux-less or solder paste disposition may be used as the bonding medium. Although area array packaging offers a robust process, care should be taken to prevent defects such as delamination, misalignment, elongated joint, voiding, bridging, opens, cracking, and poor wetting.

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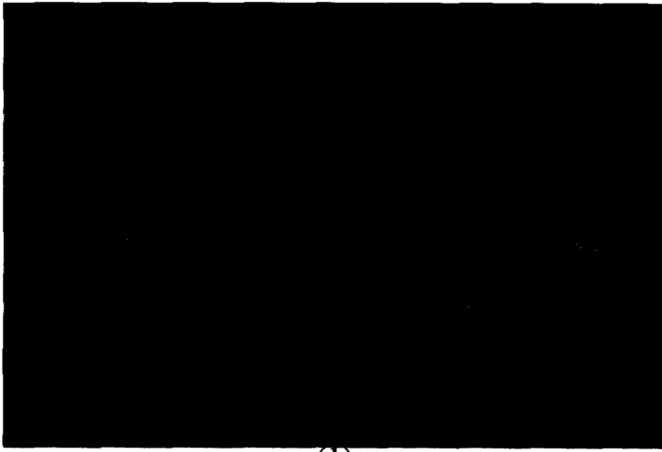

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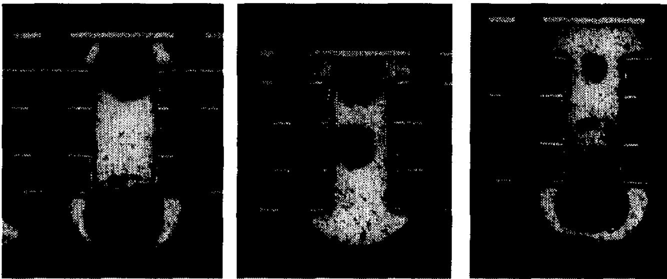

(2)

Figure 20 Voiding in BGA joints at via-in-pad system, (1) with normal via barrel plating quality, (2) with poor via barrel plating quality.