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Engineering White Paper

The Low Mass Solution to 0402 Tombstoning

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Contents

Introduction

Suntron shares a common goal of Quality with its Customer's. IPC workmanship standards are used to provide uniformity and consistency in the product that is built. To ensure that the Quality level is maintained, the Cost of Poor Quality is monitored with respect to internal process controls. The subject of component Tombstone as a recorded internal process control defect has become an increasing concern.

CCA's having this type of defect need special attention due to the high risk in late delivery and rework times associated with the replacement of parts and PCB repair.

With no direct cause and resolution to any single aspect of this type of defect, an in-depth investigation was needed to determine the Root Cause of this defect with an acceptable resolution.

Problem Statement

Have you ever thought or experienced questions or statements that sound like:

- Process Defects are the responsibilities of the Manufacturer and not mine…
- My CAD Libraries are up-to-date, why is this my problem …
- I continually change my CAD library for every Manufacturer, why do I have to change it again…
- Other Manufacturers have built this assembly before with no problems…
- Quality, On-Time-Delivery and Cost are the responsibilities of the Manufacturer and not mine …

Why is the 0402 such a problem?

DEFINITION

By definition, a *tombstone* is a defect where a 2-leaded, wrap-around lead style termination chip component has failed to lay down and allow the solder to make the required electrical/mechanical connection to the target pads simultaneously. The effect is where only one side of the 2-leaded chip component has been soldered to the target pad and the sister termination of the chip component is not in contact to the target pad.

Picture courtesy of IPC -610

By definition of the tombstone defect; it is therefore plausible, that if one side of a 2-leaded component is not soldered, then both sides are in question with the end result that an additional defect (missing part) can exist.

The experience of the Tombstone effect drives special attention to ensure that additional defects (or damage) are not incurred to the component and/or printed circuit board (PCB) pads. After Surface Mount placement and reflow (SMT); the assembly is then immediately re-routed from its intended next process step, to a rework station to inspect, rework and/or repair what has occurred.

HISTORICALLY

This defect may or may not be reported to the Customer. To determine if this defect is a process and/or design related issue is a difficult task to discern. There have been many assumptions from

- The Manufacturer has poor process controls and/or has failed to ensure that there is sufficient solder volume and deposition to the target pads…
- To Stencil design; where for resolving a Tombstone issue, a home-plate design should be incorporated…
- To CAD designers creating a specific pad geometry (home-plate design) to eliminate this issue.

It is agreed that SMT process controls, Pad Geometry and Stencil design are factors in the Tombstone effect. However, the question still remains. What is causing the chip component to tombstone if the process controls are tuned; the stencil and pad geometry is of a home-plate design and the Tombstone effect is still present?

Some studies have looked at solder composition;

- Varying grain sizes
- Tin/Lead (SnPb) vs. Lead-Free
- Dual reflow solder paste, where one alloy would reflow and secure the chip component into position prior to the second alloy reflowing to make the electrical connection.

IPC has performed studies and found that the IPC-SM-782A (1993/1999) was in error in many areas. The standard was rewritten to become IPC-7351B (2005/2010) Generic Requirements for Surface Mount Design and Land Pattern Standard. To provide consistency and stability, an equation to calculate the proper pad geometry was included. As well as 3 acceptable Density Levels that is based on the component population density of the PCB.

OVERVIEW & REASSESSMENT

All of the above has helped to mitigate the Tombstone effect; however, when the goal is to eliminate the issue, the question of "What is causing the chip component to tombstone?", still remains.

With respect to the information that has been provided, one aspect appears to have been overlooked. That aspect is the physical component. Although the physical component may be in compliance the EIA 0402 standard, the physical characteristics of the component must be understood and ruled out.

A dimensional evaluation (comparison) was performed on 7-Capacitor and 6-Resistor Component Manufacturers most commonly used by Suntron's Customers. The analysis looked at the component body and its terminations. What was revealed was that 86% (6 out of 7) of the Capacitor and 50% (3 out of 6) Resistor Manufacturers, had different Body and Termination dimensions and tolerances. See Appendix A for dimensional details.

> *Note, for validation of this discovery, the same comparison was performed using the same Component Manufacturers with respect to the EIA 0201 and EIA 0603 package type. In all cases, each Manufacturer produced an identical part. Therefore, the conclusion is that the EIA 0402 is but one facet to the root cause to the Tombstone issue.*

Utilizing the research information that has been provided, it is quite clear that the Tombstone effect is not limited to one root cause. Many efforts have influenced the behavior and therefore cannot be discounted. Now that the understanding is clear, a reformulation with respect to a proper solution can now be derived.

POINTS FOR CONSIDERATION

There are 3 major factors effecting tombstones; Component, Layout and Solder flow behavior. Each influences the Tombstone effect. Understanding the relationship between these 3 factors is critical for understanding and resolving the issue.

- Component
  - Mass, Body & Termination Size, and associated Tolerances
- Pad Geometry
  - Size & Spacing
  - IPC Standard
  - CAD Library
- Copper Exposure
  - Stencil & Solder Volume
  - Soldermask Clearance & Coverage
  - Soldermask Defined (SMD) pads verses Metal Defined (MD or non-soldermask defined – NSMD) pads with respect to Signal trace and Planar connections.
- Copper Density
  - Soldermask Defined (SMD) pads verses Metal Defined (MD or non-soldermask defined – NSMD) pads with respect to Signal trace and Planar connections.
  - Via-in-Pad designs
  - Balance

COMPONENT

With respect to the physical component dimensions and their differences from manufacturer to manufacturer, one must also not discount that the mass of the component plays a factor as well. The lower the mass, the more susceptible it is to the influences of solder flow behaviors. The EIA 0402 is considered as a low mass component. Therefore, solder flow behaviors must be controlled and implemented from a layout perspective.

> *With respect to this whitepaper and its focus on the EIA 0402 as a low mass component, the EIA 0603, 0201, and 01005 chip components must be considered as low mass components as well.*

PAD GEOMETRY

As noted earlier, IPC has rewritten the old IPC-SM-782 standard to become IPC-7351. This standard will show that it has the best layout for EIA 0402's. However, when the physical body and termination dimensions (tolerances included) of the component were superimposed onto the IPC-7351 recommended pad geometries, it was found that not in all cases did the recommendation accept the component as fabricated. The pad geometries appeared to be focused strictly around the nominal component body dimensions and did not take into account the tolerances. IPC focused strictly on the termination tolerances and its variations with regards to the length of the part. The width was found to be in error and only states the nominal conditions. This error was found during the evaluation of the Component Manufacturers. See Appendix B for details of Component on Pad Layout.

> *For clarity in understanding the IPC-7351 standard, the pad geometry is only good for the component selected. If alternant components (manufacturers) are selected (typical on Bills Of Materials), the physical dimensions must be the same. Any variation in the component when the pad geometry was not designed for that component, the Tombstone effect may be present.*

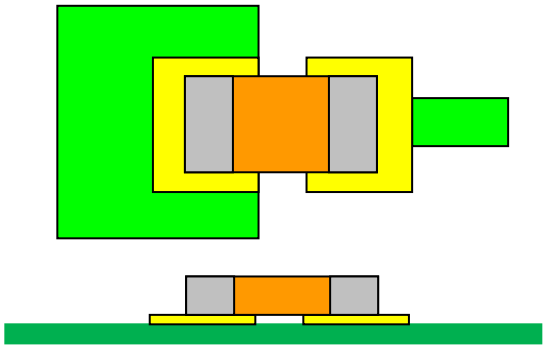
It is quite clear that proper pad geometry is critical in controlling the behavior of the Tombstone effect. Since IPC had taken the initiative in rewriting the standard, it is highly suspect that the designers CAD Library would lag in its update. Therefore, the library is suspect to remain in non-compliance. To ensure industry compliance, the validation of compliant pad geometries is needed.

In summary for Pad Geometries, the Suntron EIA 0402 Recommended Pad Geometry illustrated in Appendix B is designed around maximizing the exposed surface area to accept all component variances, yet minimizing the amount of real-estate needed to achieve the critical goal.

> *For clarity, Suntron EIA 0402 Recommended Pad Geometry is good for <u>multiple</u> components (manufacturers) as typically selected alternates are used on Bills Of Materials.*

COPPER EXPOSURE

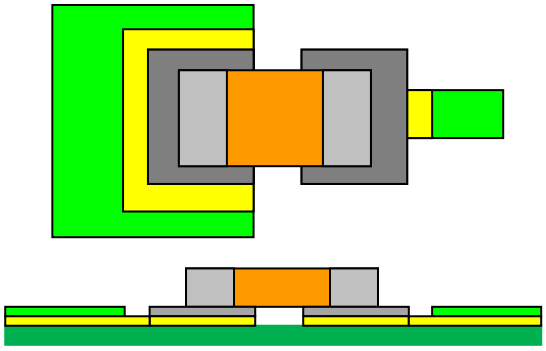
With the clear understanding on the criticality of a proper pad geometry (*Suntron EIA 0402 Recommended Pad Geometry*) and its relationship to the EIA 0402 physical component, the focus will now shift to solder flow behaviors and the effects on low mass components.



From a conceptual layout, a pad geometry is the ideal amount of copper that is needed for a component.

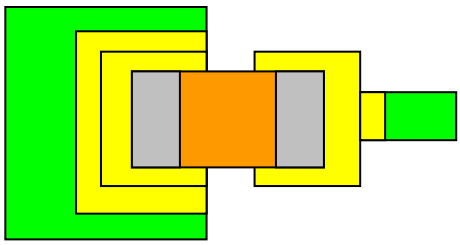
Top View

Side View



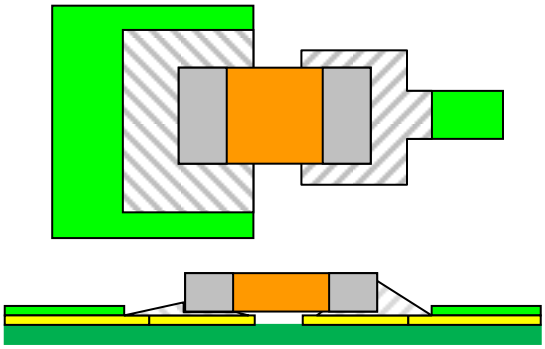
This illustration represents a released layout for PCB fabrication and Circuit Card Assembly (CCA). Layers illustrated are Copper, Solderpaste and Soldermask. Where the Soldermask Clearance is illustrated at 5mils beyond the intended (target) pad geometry

Shown is a typical 0402 layout where one pad (Metal Defined - MD) has a connecting trace and the sister pad is Soldermask Defined (SMD) on either a wide trace or plane.



When the PCB is fabricated with respect to fabrication process tolerances and controls, the effective surface area for the SMD pad is now greatly increased from the original intent.

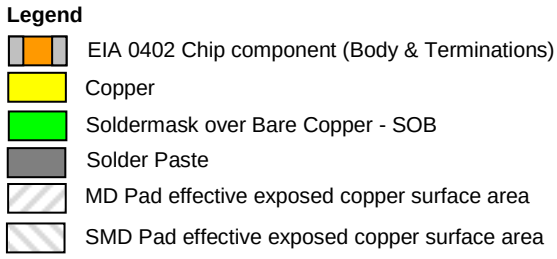
(*no side view shown*)



This increased surface area is ~65% larger than the MD sister pad.

This increased surface area has a dramatic effect on the containment of the intended solder volume originally targeted to be the same as the MD pad illustrated in the solder paste layer.

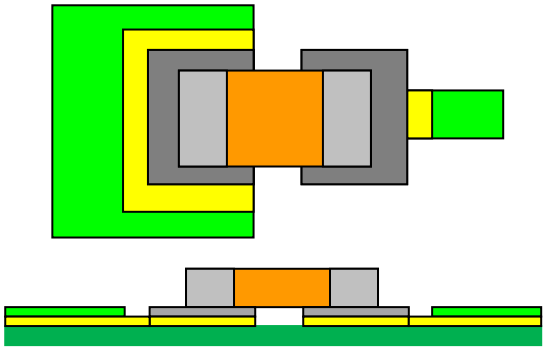
Solder will flow to any exposed copper surface area. Since the SMD pad is larger than the MD pad, the SMD pad solder volume (height) will be reduced by ~65% when compared to the MD pad and its original intent.



If the Soldermask Clearance were to be reduced from 5mils to 2mils, the exposed surface area will only increase by 25%. Although this may provide better control, the aspect of Copper Density must now be considered.

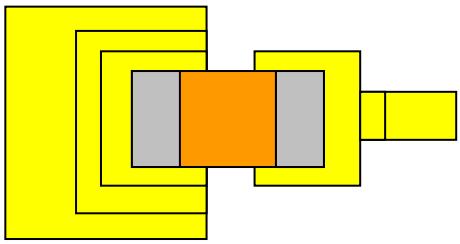
COPPER DENSITY

Copper density is the amount of copper that is required to heat up to a temperature to reflow solder with respect to a component termination and its target pad. In the simplest approach, this definition is often overlooked or sacrificed in terms of electrical considerations. However, with respect to low mass components, pad geometry thermal balance is a key factor in the Tombstone effect.



This illustration represents a released layout for PCB fabrication and Circuit Card Assembly (CCA). Layers illustrated are Copper, Solderpaste and Soldermask. Where the Soldermask Clearance is illustrated at 5mils beyond the intended (target) pad geometry

Shown is a typical 0402 layout where one pad (Metal Defined - MD) has a connecting trace and the sister pad is Soldermask Defined (SMD) on either a wide trace or plane.



To better understand the amount of copper that is used, it is necessary to remove the soldermask layer since it does not control heat transfer.

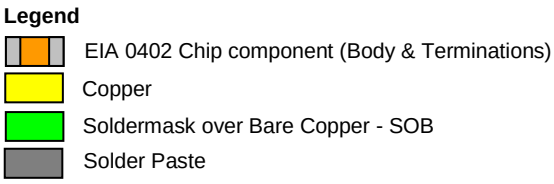
When the PCB is sent through the SMT Reflow oven, it is conceptually thought that the PCB will heat up evenly. From a copper density point of view with respect to low mass components, this is an incorrect assumption.

The MD pad has a much lower copper density when compared to the SMD pad. Therefore the MD pad will heat up before the SMD pad.

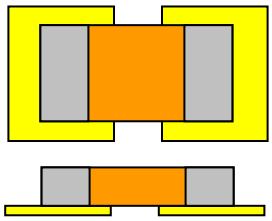
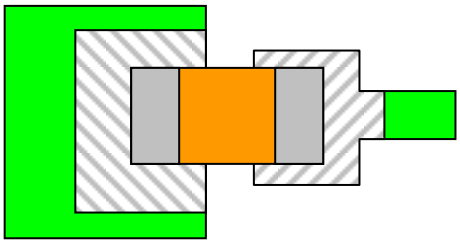
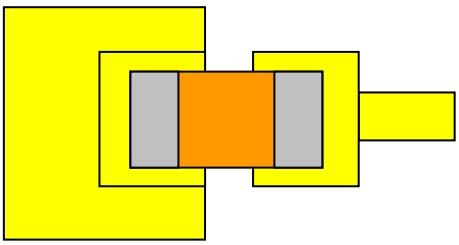
Another way to think about it is, understanding that the connecting trace acts as a thermal heat relief to the MD pad; thus, keeping all of the necessary heat onto the target pad. With respect to the SMD pad, there is no thermal heat relief present; therefore, all of the necessary heat for the target pad is being sinked away to the plane.

> *The Via-in-Pad design concept of an internal layer being the plane is the same as a SMD pad on an outer plane.*

With consideration for low mass components, thermal balance for the pad geometry is a key factor. Each pad must be considered as a group and not independently.

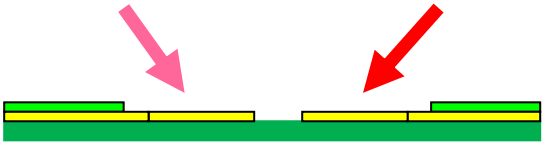
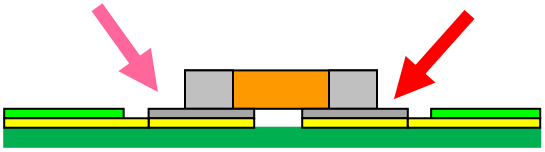
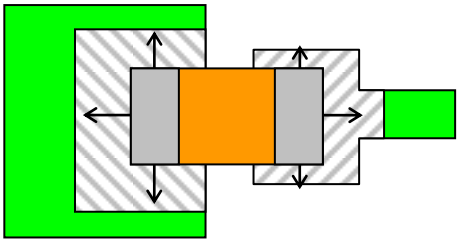
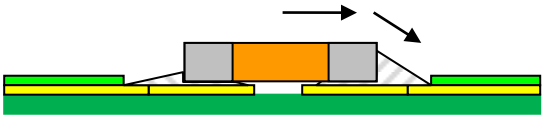
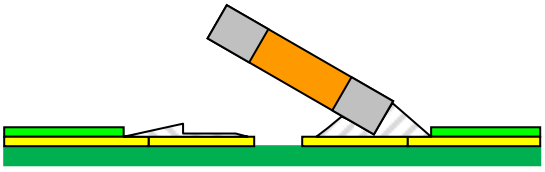


SUMMARY - POINTS FOR CONSIDERATION

Component Appendix A Pad Geometry Appendix B		Component & Pad Geometry An optimally designed pad geometry is only one facet of the Tombstone effect.
Copper Exposure		Solder Volume Imbalance SMD vs. MD Where the soldermask clearance can cause a 25% to a 65% increase in surface area which equals the amount of imbalance.
Copper Density		Copper Density Imbalance SMD vs. MD Where the SMD pad (left) has a greater copper density when compared to the MD pad (right). This equates to a thermal imbalance.

SUMMARY – ROOT CAUSE OF THE TOMBSTONE EFFECT

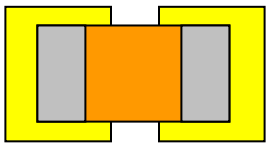
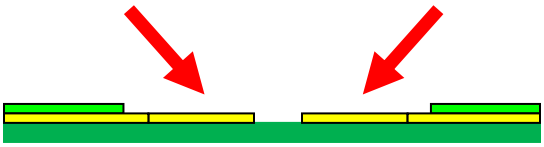
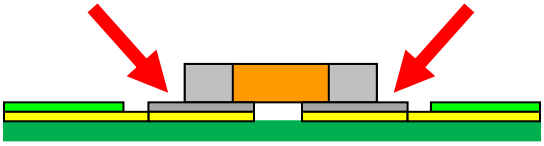
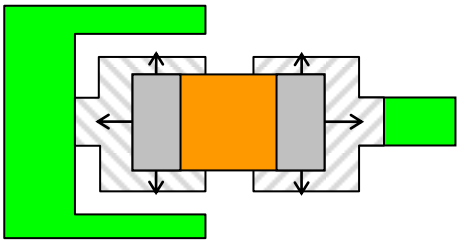
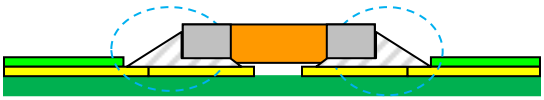
Component, Layout and Solder Behavior

	Solder Behavior	
SMD pad (left) MD pad (right)	SMD pad	MD pad
	Target temperature lags MD pad	At target temperature before SMD pad
	Solder approaches liquidus	Solder has already become liquidus
	Solder continues to flow to exposed copper due to soldermask clearance	Solder has already flowed to exposed copper
	Reduced solder volume (height), causes the capillary action surface area to be reduced	Solder capillary action surface area is optimal
 	At the time of SMT reflow; the MD pad will heat up before the SMD pad. This means that all solder behaviors are performing at different rates. The MD pad will have become liquidus, flowed to any exposed copper and achieved capillary action before the SMD pad (Surface Tension imbalance). The overall MD pad solder flow behavior, with respect to a low mass component, will draw the component to the right and down. *Tombstone*	

REFORMULATION TO THE SOLUTION

With the clear understanding that there are many contributing factors to the Tombstone effect; Component, Pad Geometry, Copper Exposure, Copper Density and Solder Flow Behavior, *balance* is the key to the solution for low mass components.

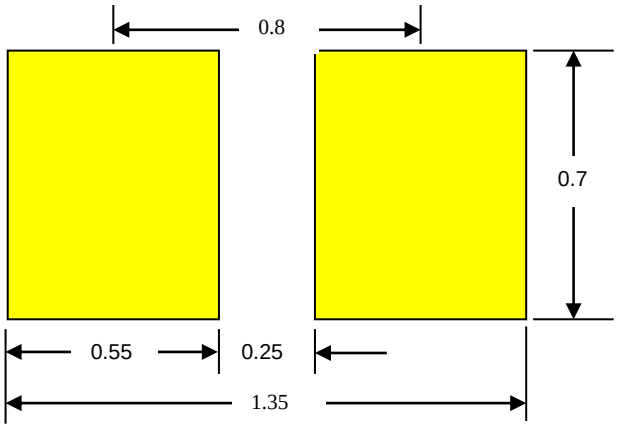
- Pad Geometry - must be present in order to accept many manufacturers of the component
- Layout - each pad must be treated as a group and not independently
- Copper Exposure - each pad must be equal (or very close)
- Copper Density - each pad must be equal (or very close)

	Solder Behavior	
MD pad (left) MD pad (right)	MD pad	MD pad
	Equal Pad Geometry Accepts multiple component manufacturers	
	Equal Copper Density Both pads will achieve the same temperature at the same time	
	Both pads will achieve the liquidus at the same time	
	Equal Copper Exposure Both pads will achieve solder flow to exposed copper at the same time	
	Both pads are equal in solder volume necessary to control capillary action to be equal in its influence to the component termination	

SOLUTION RECOMMENDATION

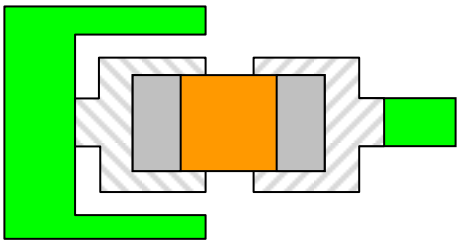
This recommendation is provided in a 3 step approach in which both must be used to resolve the Tombstone effect.

1. Use the Suntron EIA 0402 Recommended Pad Geometry. This provides the best layout solution to accept multiple EIA 0402 Component Manufacturers with the minimal amount of PCB real-estate needed.



Dimensions shown are in millimeters (mr

2. Set Soldermask Clearance to be 2mils
3. Use a connecting trace between pad and plane (or very wide trace) to be equal as the sister pad



   a. See Layout examples in Appendix C for available options.

SUMMARY & CUSTOMER BENEFIT

The provided information was to correlate an age-old issue that seemed to never to be completely resolved. With the understanding of each of the aspects and their relationships to each other, it has become quite clear that balance is the key to providing consistency from solder joint to solder joint. The implementation of the Suntron Recommended Pad Geometry and Layout provides many benefits in which not all may be listed:

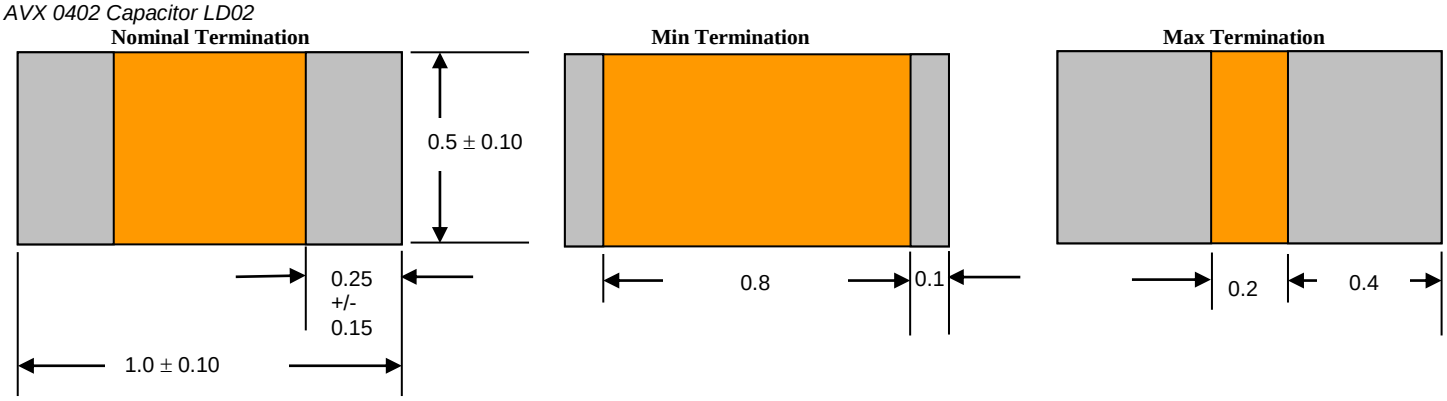
- Pad Geometry - Accepts multiple EIA 0402 component manufacturers while using only one pad geometry
- Minimized Real-estate used
- Balanced Copper Density
- Balanced Copper Exposure
- Tombstone effect virtually reduced to zero including associated defects such as PCB damage and missing components
- Layout concept is not limited to just EIA 0402
- Improved Solder joints regardless of component termination

APPENDIX A

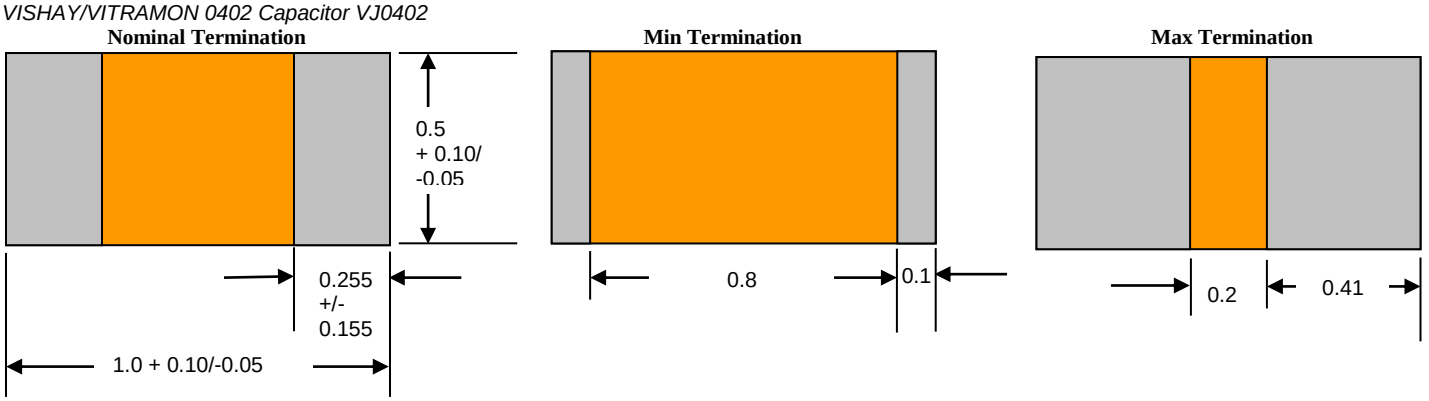
Capacitor and Resistor component specifications are EIA 0402 per their respective datasheets. Pictorial representations are based on the nominal component body size with specific focus to termination tolerances.

Capacitor Specification *dimensions (mm)*

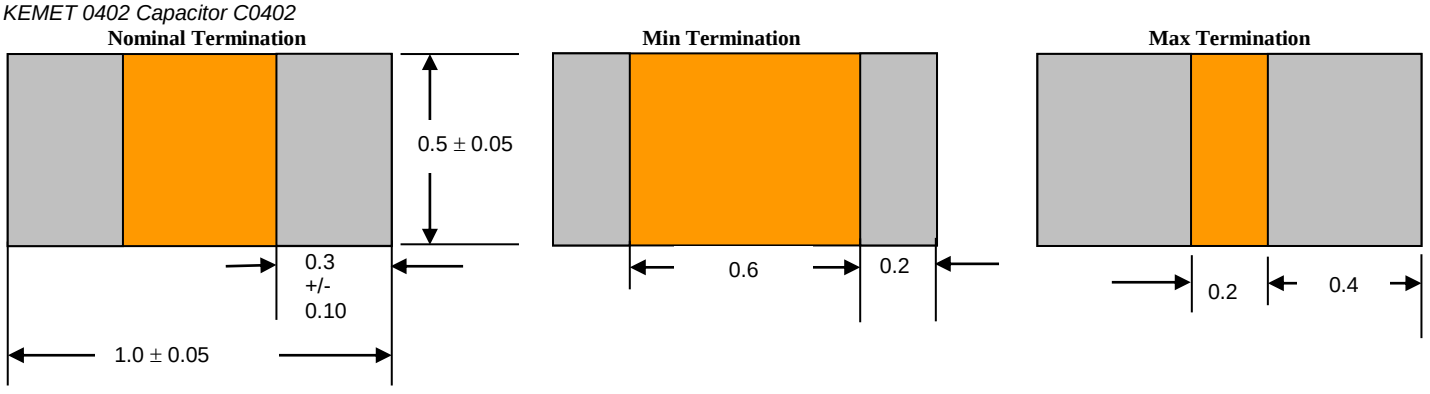
AVX 0402 Capacitor LD02



VISHAY/VITRAMON 0402 Capacitor VJ0402

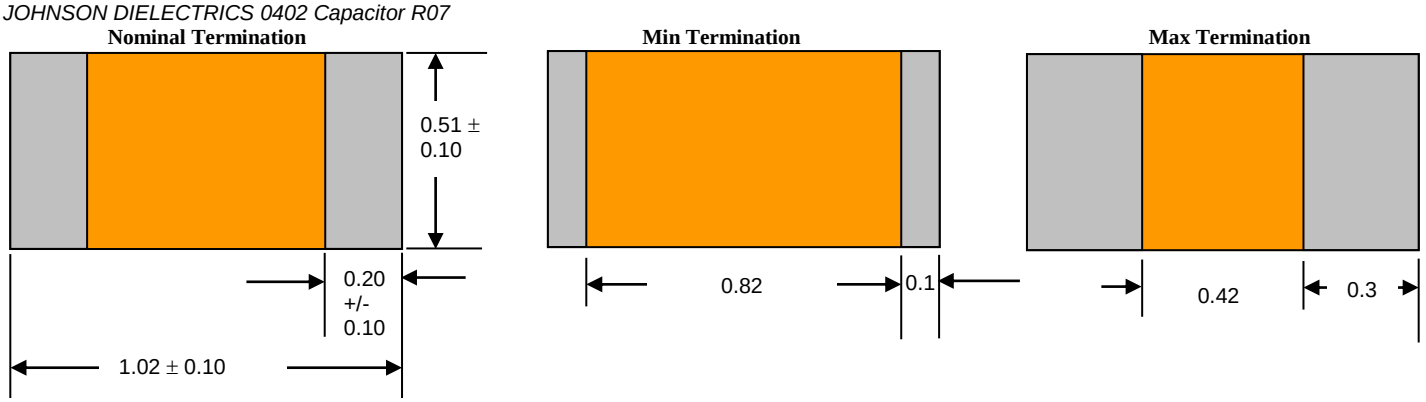


KEMET 0402 Capacitor C0402

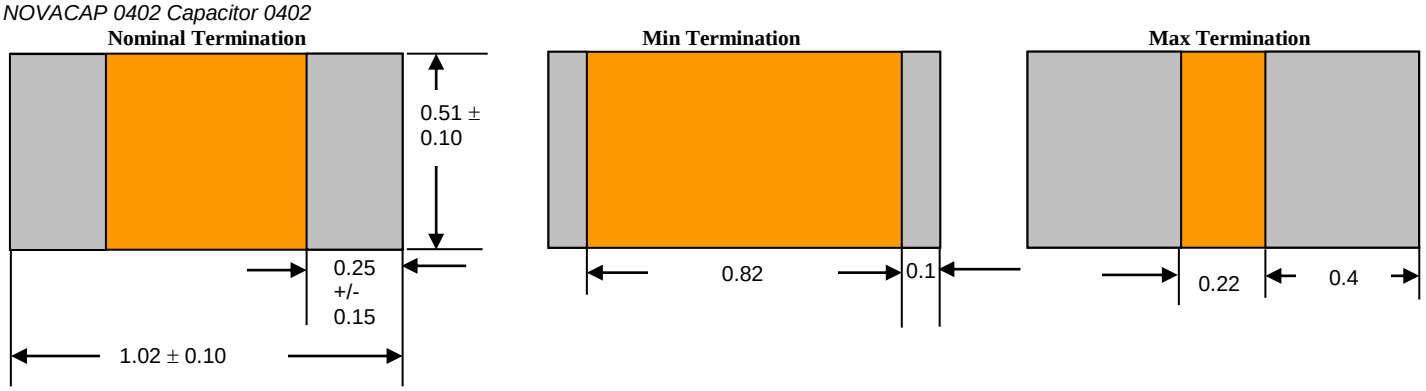


July, 2011

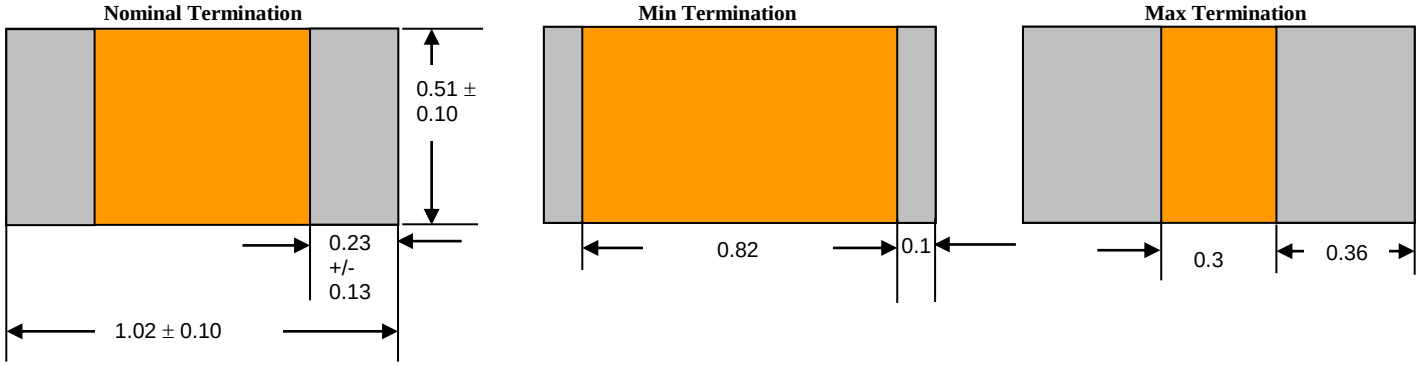
JOHNSON DIELECTRICS 0402 Capacitor R07



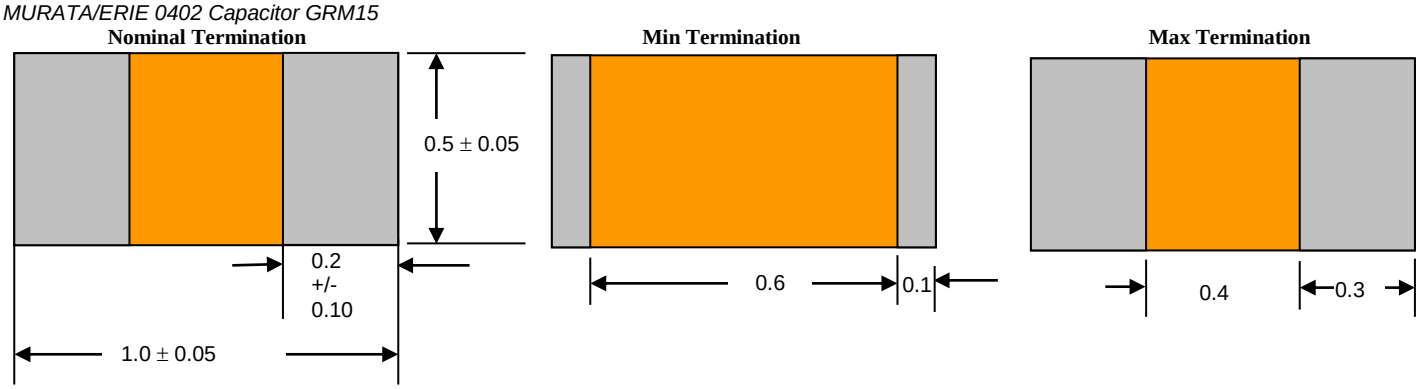
NOVACAP 0402 Capacitor 0402



AMERICAN TECHNICAL CERAMICS 0402 Capacitor 0402

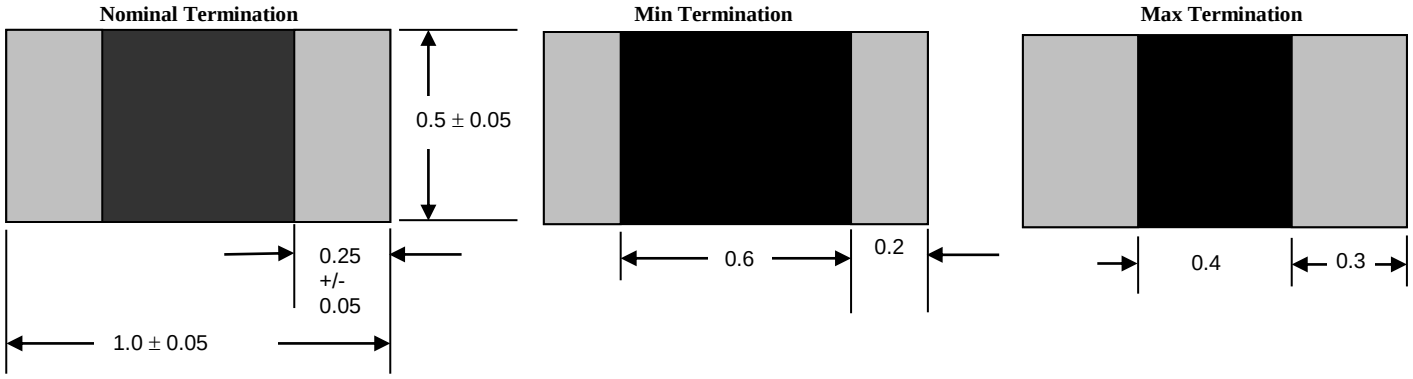


MURATA/ERIE 0402 Capacitor GRM15

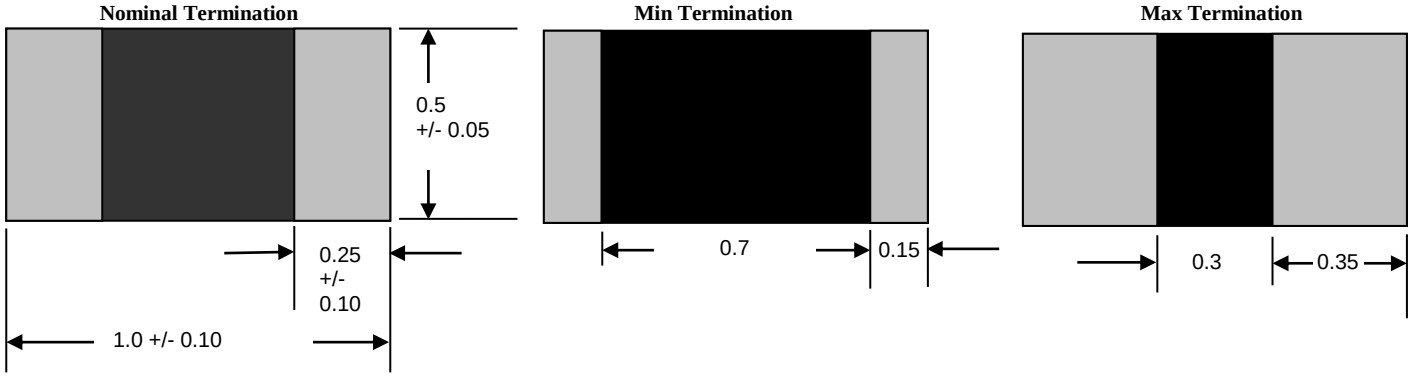


Resistor Specification *dimensions (mm)*

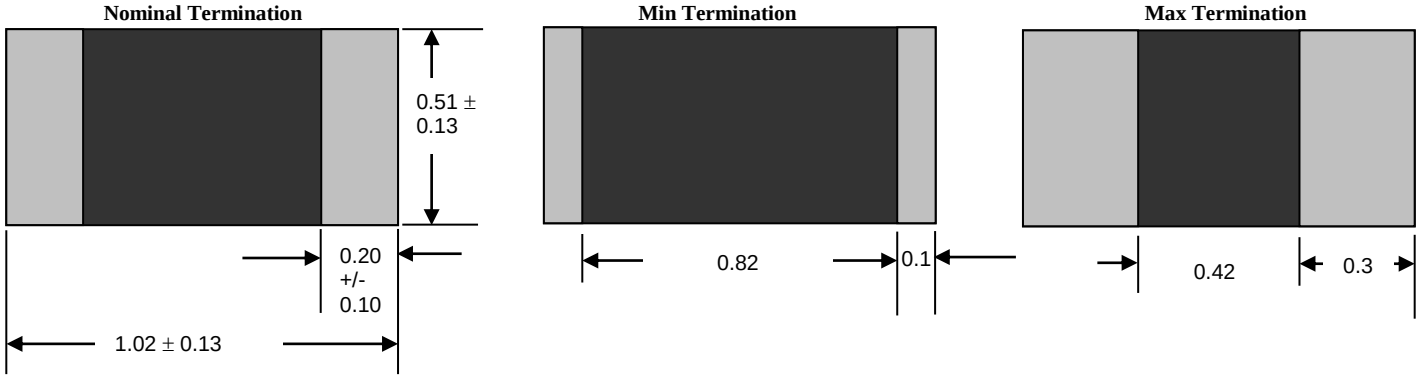
PANASONIC INDUSTRIAL CORP 0402 Resistor ERJ2G



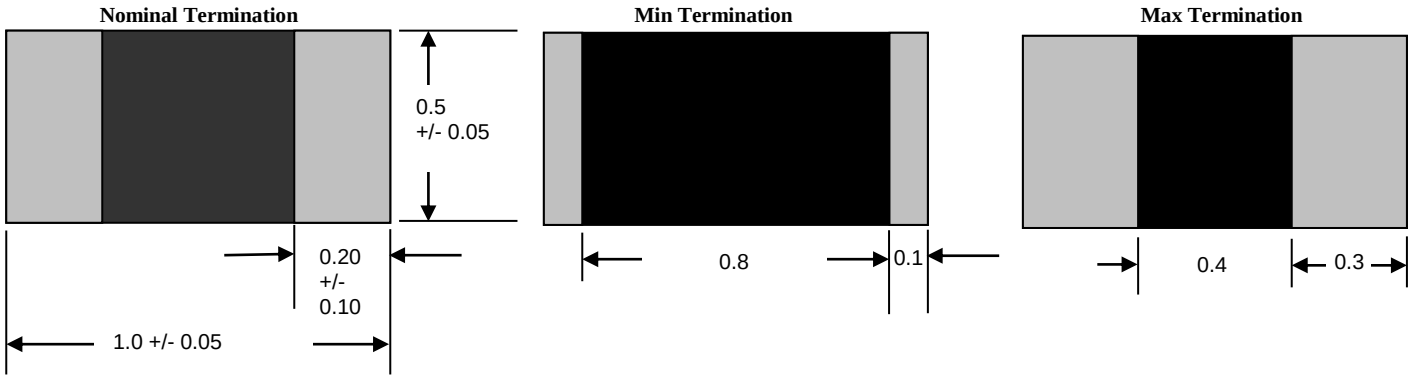
SKYWELL ELECTRONICS 0402 Resistor RC02, ASJCOP 0402 Resistor CR10, BOURNS INC 0402 Resistor CR0402



INTERNATIONAL MFG. SERVICE INC 0402 Resistor RC1-0402



SUSUMU CO. 0402 Resistor RR0510

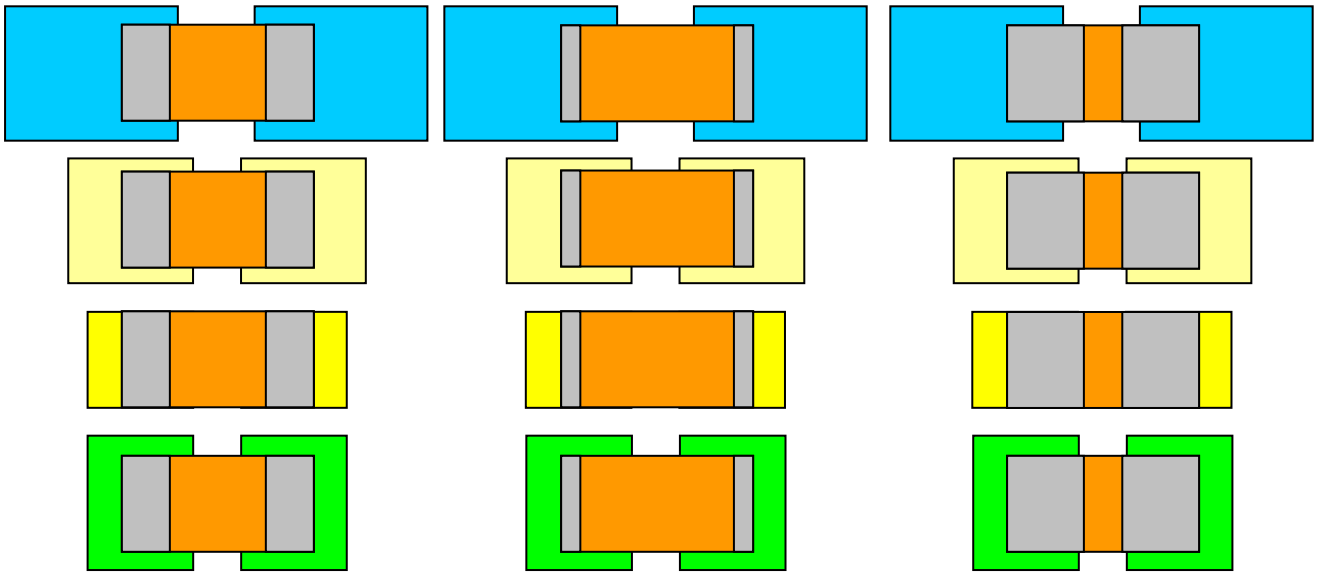


APPENDIX B

The AVX component presented is only 1 of 13 Manufacturers reviewed. The AVX component is used for pictorial purposes only. Component, Pad Size Geometry and Spacing are scaled 1:1.

AVX Component (NOMINAL Body dimension) is superimposed onto a Pad Layout

Nominal Termination **Min Termination** **Max Termination**

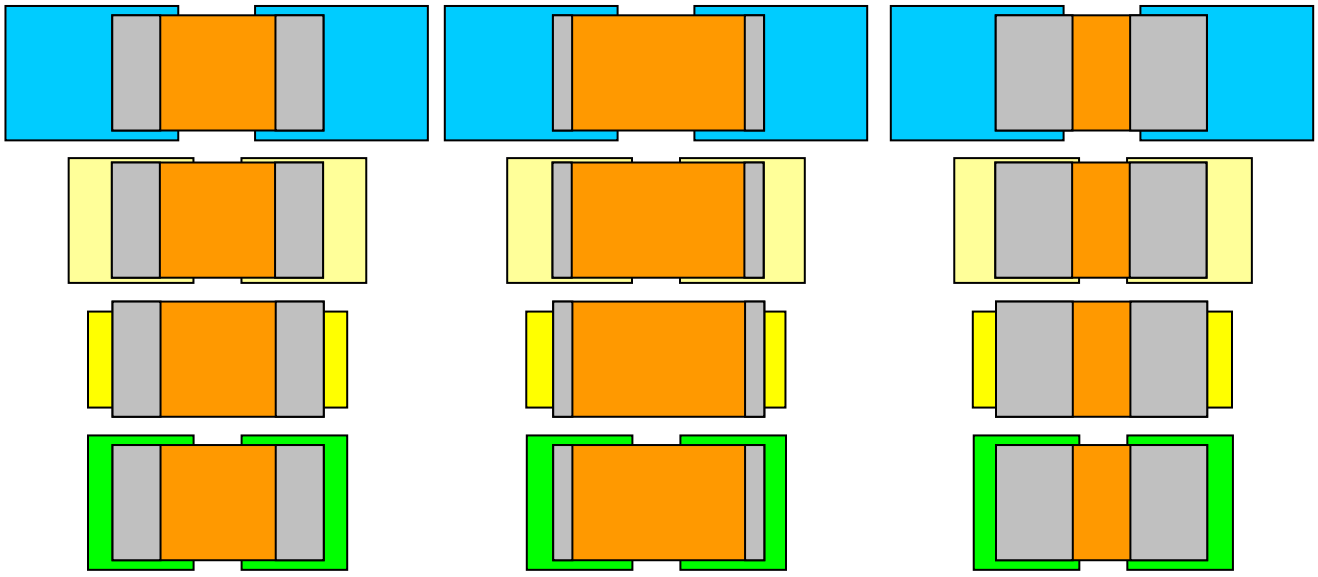


Legend

- IPC-SM-782A (OLD - Replaced with IPC-7351A)
- IPC-7351A (SMN (NOMINAL) - Normal DENSITY LEVEL B)
- IPC-7351A (SML (LEAST) - HIGH DENSITY LEVEL C)
- Suntron EIA 0402 Recommended Pad Geometry
- EIA 0402 Chip component (Body & Terminations)

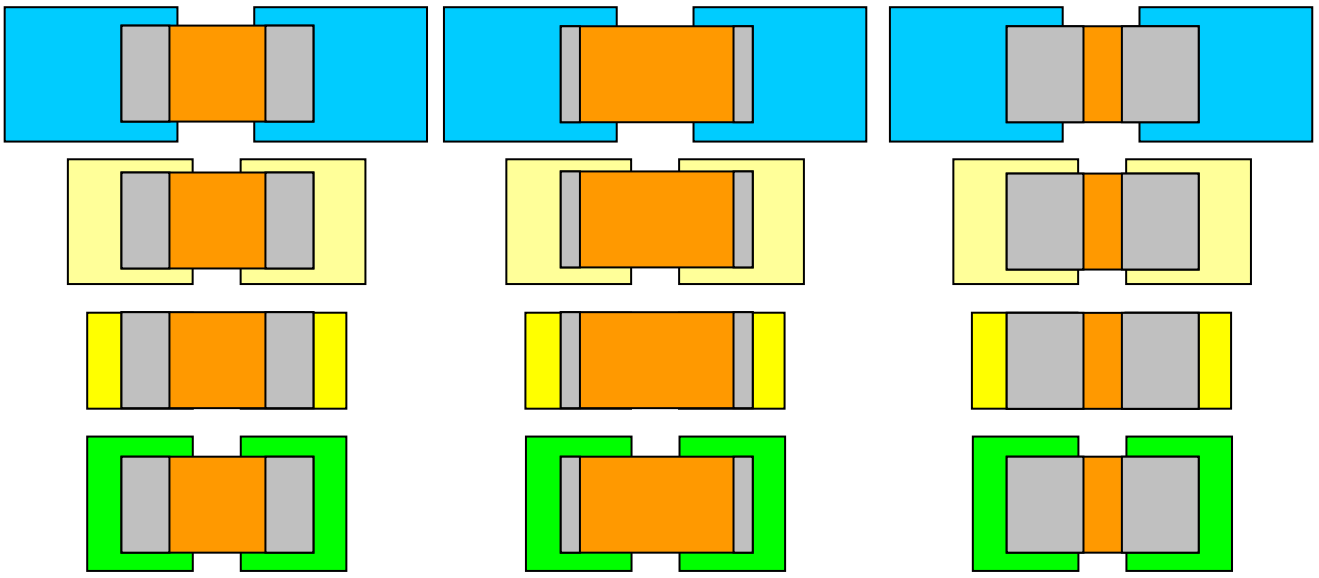
AVX Component (MAXIMUM Body dimension) is superimposed onto a Pad Layout

Nominal Termination **Min Termination** **Max Termination**

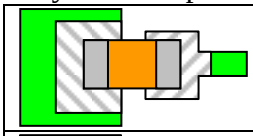
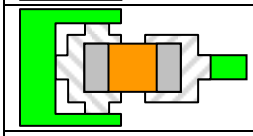
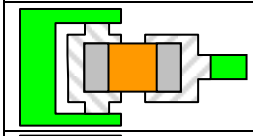
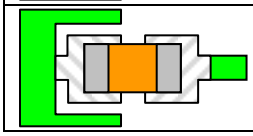


AVX Component (MINIMUM Body dimension) is superimposed onto a Pad Layout

Nominal Termination **Min Termination** **Max Termination**



APPENDIX C

Layout examples	EIA 0603	EIA 0402	EIA 0201	EIA 01005
	***NOT Recommended***	***NOT Recommended***	***NOT Recommended***	***NOT Recommended***
	Acceptable	Acceptable NOT Recommended	***NOT Recommended***	***NOT Recommended***
	Acceptable	Acceptable	Acceptable NOT Recommended	***NOT Recommended***
	Preferred *RECOMMENDED*	Preferred *RECOMMENDED*	Preferred *RECOMMENDED*	Preferred *RECOMMENDED*

TERMINOLOGY DEFINITION

NOT RECOMMENDED
This means that the Copper Exposure and Density will have a great influence on the low mass component. Pads are unbalanced and will generate defects

ACCEPTABLE (NOT RECOMMENDED)
This means that the Copper Exposure and Density will have an influence on the low mass component but is suspect to be minimal. Pads are technically unbalanced and may generate defects

ACCEPTABLE
This means that the Copper Exposure and Density will have a minimal influence on the low mass component but is suspect to be slight. Pads are slightly unbalanced but not expected to generate defects

PREFERRED (RECOMMENDED)
This means that the Copper Exposure and Density for each pad is balanced with respect to the influence on the low mass component. This layout should not generate defects.

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