目錄表 Table of contents

圖表 Table of Figures

1.0 印刷回路板裝配設計指導原則 Design Guideline For Printd Circuit Board Assemblies

1.1 目的 Purpose

表面貼裝設計是團隊共同努力的結果，設計者不可能自己去制定一份表面貼裝設計，因爲那要用到所有的表面貼裝技術並具備成本競爭力的優勢。該設計團隊包括了設計、採購、工藝工程、產品工程、元件工程、測試與品質保證等。整個團隊的協調執行、是確保其成功的有效方式。

Surface mount design is a team effort. Designers cannot ,by themselves ,produce a surface mount design that will utilize all of the benefits of a surface mount technology and be cost competitive . The implementation of a surface mount team,consisting of Design,Purchasing,Process Eng.,Product Eng.,Component Eng.,Test and QA is the most effective way of ensuring success.

1.2 範圍 Scope

檔中的資料舉例說明了一些關鍵性的項目，這些專案高度影響著組合技術裝配的製造能力。對這份資料的使用和對所參照規範的更充分的理解將有助於 Solectron 在 SMT 與 PTH 裝配生產中獲得最大的成功。對這個機板設計的推薦是基於 Solectron 設計中心和它全世界的製造生產場所的集體知識的結晶。像蜂窩電話、傳呼、攜帶型電腦等，因爲要求高密度連接設計，因此請參考 Soletrion 的或蜂窩電話的高密度機板製造設計指導書。這些資料針對那些產品類型提供專門的參數。

The information in this document illustrates the key items that highly influence the manufacturability of mixed technology assemblies. Use of this document and the more comprehensive specifications referenced will maximized Solectrons success in this production of surface mount technology(SMT) and pin through hole(PTH) assemblies. This recommendations for board design are based on the collective knowledge of Solectron’s

Design Centers and its worldwide manufacturing locations.

For products requiring High Density Interconnect(HDI) design,such as cell phone,pagers,mobile computers,ect.,please reference Soletrion’s or “Cell Phone |High Density Boards Manufacturing design guidelines”.That document provides the parameters unique to those product types.

1.3 定義 Definitions

用於該設計工藝的定義可在檔 SDC-10-011719 中查閱。

Refer to document SDC-10-011719 for definitions used in this design process.

1.4 DFM 參考文件 References Documents for DFM

IPC 插孔 IPC Pin through hole IPC-SM-780

IPC 表面貼裝設計與區域式樣

IPC Surface Mount Design& Land Pattern IPC-SM-782

IPC 作業標準 IPC Workmanship Standards IPC-A-610C

IPC 設計與裝配工藝實施

IPC Design and Assembly Process Implementation IPC-7095

1.5DFF 參考文獻 References Documents for DFF

PCB 製作規範序

PCB Fabrication Specification Procedure CORMTL-10-004019

印刷板設計的通用標準

Generic Standard on Printed Board Design IPC-2221

剛性印刷板可組合設計標準

Sectional Design Standard for Rigid Printed Boards IPC-2222

HDI 與微型通路的設計指導書

Design Guide for HDI and Micro-vias IPC-2315

1.6 安全性要求 Safety Requirements

由 Solectron 設計的所有產品都必須滿足客戶的要求和所有的應用安全性標準,但更重要的是,任何表明對安全有危害的設計,都必須要確認。管理處有責任確保設計的安全。任何有關安全性的問題都必須文件化,同時要接受客戶的審核。在安全性問題解決之前，

整個設計計畫將不得進入下一個發展階段。

All products designed by Solectron must meet customer requirements and all applicable safety standards, but more importantly,any design that presents any safety hazard must be identified. Management has the responsibility to ensure design safety.Any safety issues must be properly documented and reviewed with the customer. Safety issues ,until resolved,will prevent the program from moving to the next stage of development.

1.7 尺寸 Dimensions

除非另有注明，否則所有以英寸表示的尺寸精確到三位小數，以毫米表示的尺寸精確到兩位小數，並置於括弧內(1.000〔25.40〕。

Unless otherwise specified ,all dimensions are in inches to three decimal places,with millimeters to two decimal places in brackets(1.000〔25.40〕).

重要備註：對墊片的大小、間距、區域範圍等，如同使用標準增量(0.001inch,0.05mm)一樣，米制尺寸可以不需精確的轉換。極力建議的是，設計不僅僅是轉換單位，而要利用一套制定尺寸的體系。

Important Note: Metric dimensions may not be exact conversions as the intent is to use standard increments (0.001inch,0.05mm) for pad sizes,spacings,clearances,etc.. It is strongly recommended that designs utilize a single dimensioning system and not simply convert units.

1.8 變更要求 Change Requests

有需要對參考文獻作出變更、修正、附加或通知的，請聯繫 Solectron 技術中心的設計主管或者直接派當地的代表前往。地址：Solectron Technical Center,Building 1,Milpitas, California, 95035

To make request for a change, correction, additions or information on references contact Director of Design, Solectron Technical Center,Building 1,Milpitas, California,95035 or your local Site representative.

2.0 印刷電路板裝配製造指導書 Manufacturability Guidelines For Printed Circuit Board Assemblies

2.1DFX（X 設計） DFX (Design For X)

2.1.1 簡介 Introduction

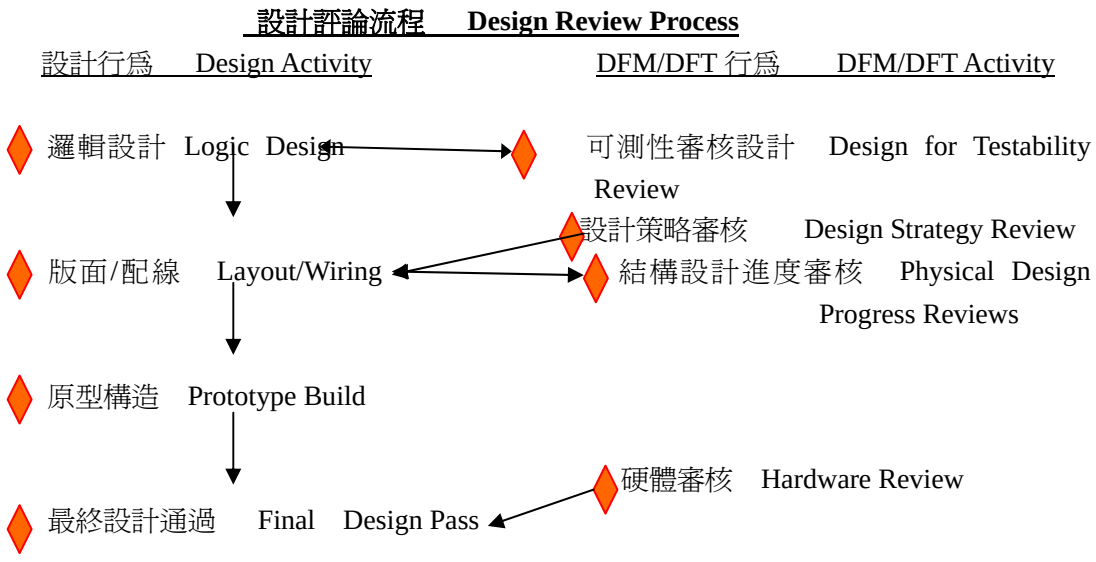
在設計機板的過程中，影響 PCB 板組裝的品質與成本的多數因素，就已經確定。在組裝平臺談及 X 設計時，鍵盤設計的諸因素將被重提。此中的 X 分別意謂，F 表示機板的“製作”之意，A 代表裝配，T 代表測試，M 代表製造能力等等。

The majority of factors affecting the quality and cost of a PCB assembly are determined during the design of the board.At the assembly level a summary of the key board design factors will be restated under the topic DFX,Design for X,where X can mean F for the PCB fabrication,A for assembly,T for test,M for manufacturability,etc..

2.1.2PCB 裝配之 DFX DFX for the PCB Assembly

爲了達到一片 PCB 裝配的高品質、低成本的效果，設計過程必須及時，並基於高度合作之上。這些設計、DFX、DFM 和 DFT 的工程師都是作爲該設計過程的一個整體。，對互動式 DEX 設計而言，一塊好的範本評論流程爲：

DFX To achieve high quality cost effectiveness on a PCB assembly, the design process must be done on timely and highly collaborative basis. The Design, DFX, DFM and DFT engineers must all be in an integral part of the design process.A good template for an interactive DFX design review process is:



2.2DFM（製造能力設計）DFM (Design for Manufacturability)

2.2.1 簡介 Introduction

在機板開始設計之前，爲了使已完工小板的組裝儘量適於製造，下面的 DFM 因素必須加以考慮。它們包括：焊接工藝的類型，自動控制的相關因素，元件參數選擇，面板的利用，加工孔的位置，基準位置，標籤位置，小板 finish 與測試要求等，在盡可能低的成本條件下使設計適於製造，以上提到的都是些關鍵性步驟。

The following DFM factors must be considered before beginning a board design so that the completed board assembly will be as manufacturable as possible.The type of soldering processes, automation considerations, component preferences, panel utilization,tooling hole positions, fiducial positions,label positions,board finishes and testing requirements are all critical steps in making the design manufacturable at the lowest possible cost.

2.2.2 安裝焊接工藝複雜性 Assembly Soldering Process Complexity

PCB 安裝應使用盡可能簡單的工藝設計，從而做到安裝成本最小化，產出與可靠性最大化。在複雜的工序漸增趨勢下，可用的焊接工藝流程有：

PCB assemblies should be designed to use the least complex process possible, thus minimizing the assembly cost and maximizing yield and reliability.The process types available, in increasing order of complexity,are:

Card Layout	Component Types	Solder Process
Single sided	SMT only	1 reflow
Single sided	SMT, reflow compatible PTH	1 reflow
Double sided	SMT only; passives only on back	2 reflow
Double-sided	SMT only; actives on back	2 reflow
Single sided	SMT; standard PTH	1 reflow, wave solder
Double sided	SMT; passives only on back; standard PTH	1 reflow, 1 epoxy cure, wave solder or 2 reflow,wave solder
Double sided	SMT; actives on back; PTH	2 reflow,wave solder w/selective fixture or Pin-In-Paste

注意：任何特殊通孔元件（非浸潤、熱敏、背面、壓配合等），需增加一個制程步驟和/或一個手工焊接制程。

Note: Any special PTH components(non-wettable,heat sensitive,back side,press fit, etc.) will add a process step and/or a manual soldering process.

2.2.3 自動控制通用指導書設計 Designing for Automation-General Guidelines

- 與安裝工程協作以建立各種標準安裝次序 Work with assembly engineering to establish various standard assembly sequences.
- 特別要避免那些要求手工去插入、放置、分發或焊接的工序的設計

  Particularly avoid designs that will require manual insertion,placement ,dispensing or soldering.
- 維持板的尺寸在所有安裝工藝所需設備的限制以內。相關的設備有：

  Keep the board size within the limitations of all of the equipment needed for the assembly process .This following equipment to be considered is:

  * 篩 Screener
  * 膠合設備 Glue equipment
  * 拾取與放置 Pick and place
  * 插入設備 Insertion equipment
  * 機器人放置/插入設備 Robotics placement/insertion equipment
  * 波焊系統 Wave solder system
  * 迴流焊系統 Reflow system
  * 清潔設備 Cleaning equipment
  * 測試與檢查設備 Test and inspection equipment
  * 在使用拾取與放置/插入重工、測試、檢查和治具設備時，要注意正確的元件放置，最大須在合理的製造公差範圍內。

    Observe the proper component spacing and maximize to allow for the proper manufacturing tolerance when using pick and place/insertion reworking, testing, inspecting, and fixture equipment.
- 特殊元部件的數量最小化 Minimize the number of unique component part numbers.

2.2.4 元件參數選擇 Component Preferences

- 小板的尺寸和連接器結構是由此個別系統包裝設備所規定的。這些規定在決定

要求進行一項 PCB 組裝的工藝時非常重要，同時這些規定還影響著 DFM 決議的制定。

The board size and connector configuration is dictated by the individual system packaging requirements. These decisions are critical in determining the processes required to manufacture a PCB assembly,and influence the DFM decisions to be made.

• 選擇既能提供必須的功能又簡單易行的包裝。當有標準的間距元件且符合設計時，要避免選擇細距元件。當板的密度允許使用更大尺寸的晶片像 0603,0805 和 1206 型，要避免使用非常小的晶片如 0201 or 0402 型。

Choose the least complex package that will provide the required function. Avoid selecting a fine pitch device when a standard pitch device is available and fits the design .Avoid the use of very small chips like 0201 or 0402, when the card density would allow for larger devices such as 0603,0805,and 1206.

• 確保所有的零件和他們精心設計的裝配工藝相一致。那就是說，元件必須能夠承受 240 °c 的洄流焊或波焊制程。所有零件應能承受水洗工藝。

Ensure all parts are compatible with their intended assembly process. That is ,components must be to withstand the reflow temperature of 240°c or the wave soldering process, if applicable.All parts should be able to withstand the aqueous cleaning process.

• 避免某些元件在底面使用 Avoid use of certain components on the bottom side。

• 暴露在波焊的地方，要避免使用 0603 和更小的晶片，如 SOTs,鉭質電容, D-packs,MELFs 和 SOIC R-packs。

In areas exposed to wave solder avoid 0603 and smaller chips,SOTs,tantalum capacitors, D-paks,MELFs,and SOIC R-packs.

• 重的零件和高的零件如 PLCC,oscillator,MQFP。

Heavy parts and tall parts such as PLCCs,oscillators,MQFPs.

• 經兩個洄流週期壓緊的零件如 BGA。Parts impacted by two reflow cycles such as BGAs.

• 在波焊面上，要避免使用的零件高度超過 0.150[3.75] (首選 0.120[3.00]) 。0.200[5.00]的間距可以依 DFM 工程正式批准的使用。

Avoid the use of parts taller than 0.150[3.75] (0.120[3.00] preferred),on the wave solder side. A spacing of 0.200[5.00] may be used with DFM engineering approval.

2.2.5 SMT 元件放置　SMT Component Placement

• 配圈模式決不可共用。不可將兩個或更多的配圈墊片連接在一起以便在同一墊片上有效放置兩個的元件。而不可連接墊片造成重印以適應兩種不同封裝類型。Land patterns must not be shared. Do not combine two or more land pads together to effectively place two devices on the same pad 。Do not combine pads to create a dual footprint to accommodate two different package types.

• SMT 元件放置的位置，應該使得元件體和配圈模式不會防礙 SMT 制程中的傳載器的正常工作。首要配圈範圍是從傳載器邊緣開始的 0.200[5.00]最小值。在雙面板上， 在第一個經過 SMT 的面上，其配圈範圍必須是 0.200[5.00] ，第二次經過面配圈範圍爲 0.150[3.80]。

SMT components should be placed such that their body and land patterns do not interfere with the conveyor in the SMT process. The preferred clearance is a minimum of 0.200[5.00] from a conveyor’s edge . On double side boards , the clearance on the first pass SMT side must be 0.200[5.00],the second pass side clearan ce must be 0.150[3.80].

• 如果滿足下列條件的話，元件可以是從插件邊緣 0.100[2.50]的一個最小距離。Componets can be a minimum distance of 0.100[2.50] from the card edge if :

* 所討論的邊緣不是個傳輸邊緣 the edge in question is not a conveying edge .

* 插件在面板上或有附加斷路器上 the card is in padel or has breakaways added.

* 插件將被安放在治具裏（請教你們 DFM 工程師是否這些條件是適合於設計的） the card will be processed in fixtures(Consult your DFM engineer to determine if these conditions are applicable to the design.)

因考慮到可供選擇的波焊設備，在通孔設備引線與板背面的 SMT 元件之間必須有足夠的區域範圍。對小型晶片的一般爲 0.150[3.80] ，對大型晶片的最小值是 0.200[5.00]（參見規範“SMT 間距規則”中的 PTH /SM 尺寸）。 測量時，要從通孔邊緣到 SMT 元件體或墊片邊緣，此間距正越來越縮小。

There must be adequate clearance between PTH device leads and SMT components on the backside of the board to allow for a selective wave solder fixture. This general clearace is

0.150[3.80] for small chips and 0.200[5.00] minimum for larger devices. (See the PTH /SM dimensions in the "SMT Spacing Rules" for specifics). The measurement is taken from the edge of the PTH land to the edge of the SMT component body or pad ,which ever is closer.

2.2.6 Pin-In-Paste 設計參數 Pin-In-Paste Design Parameters

2.2.6.1 簡介 Introduction

P-I-P 組裝是一種錫焊通孔元件的方法，這種方法不使用波焊或手焊就可以將其焊到插卡裝配上。此種技術亦稱爲孔內膠或插入式洄流焊。P-I-P 能夠減少在一次組裝中從選擇點到點錫焊與手工作業的數量。這將增加大規模制程的生產能力，同時消除由膠粘元件與手工錫焊所帶來的品質問題。這種 P-I-P 制程，常規上是用在雙面 插卡組裝的第二通由面，但是在帶有恰當長度引線和具有保持力的元件條件下，此制程也能用於雙面 。

Pin-in-paste (P-I-P) assembly is a method of soldering pin through hole components to a card assembly without using wave soldering or hand soldering . This technique is also referred to as Paste-in-hole or intrusive reflow.Pin-in-paste soldering can reduce the amount of selective point to point solder and hand work on an assembly. This will increase throughput in a high volume process and elimilate the quality problems associated with glued components and hand soldering . The P-I-P process is normally used on the second pass side of a double sided card assembly but can apply to both sides with the correct lead length and retention propertied of the component.

設計參數 Design parameters

• 對於使用 P-I-P 所推薦的最大原材板的厚度爲 0.063[1.60]。厚板上電鍍孔更難填充，並且會導致錫焊連接不充分。在 P-I-P 錫焊連接中，由於一些孔內填充不足 100%，因此一份組裝製作注意點指明必須有 50%的填充（IPC-A-610 class 2 建議爲 75%) 。要確保電路的設計者意識到此孔填充的局限且又是合乎電路性能的 。

The recommended maximum raw cards thickness for using P-I-P is 0.063[1.60]. The plated hole is harder to fill on thicker cards and can result in insufficient solder joints. Scince some hole fill will be less than 100% on some P-I-P solder joints an assembly fabrication note is required indicating 50% hole fill(IPC-A-610 class 2 recommends 75%) is allowed when

P-I-P used. Insure the electrical designer is aware of the hole fill limitation and this is appropriate for the circuit performance .

• 推薦使用 0.010[0.25]最小環孔。在重工制程中，在插腳引線與分層周圍元件的下面，更小的環孔直徑會引起焊球。 在所有（包括珠狀物在內的）可能的電路線路上，其連接到電極寬度都要少於 0.020[0.50]。見例 1（圖 1）

A minimum annular ring of 0.010[0.25] is recommended. Smaller annular ring diameters can result in solder balls under the component around the PTH leads and delamination during the rework process. Where possible, include teardrops on all tracks less than 0.020[0.50] connected to the pad. See example 1(Figure 1).

• 插腳剖面與孔面的比率應 1：1.5-1.7。更大的比率則要求更多的焊錫膏，而這會引起錫膏印刷問題。更小的比率，尤其是圓的插腳，則會導致錫焊不充分。 見例 2 和例 3（圖 1）。

The pin cross section to hole area ratio should be 1 to 1.5-1.7. Larger ratios require more solder paste and can cause paste printing problems. Smaller ratios,especially with round pins can result in insufficient solder. See examples 2 and 3(Figure 1).

• 沒有通孔時，元件墊片或接地墊片可以貼在通孔插腳元件引線周圍的錫膏印刷面上。每一通孔元件位置可以要求不同的印刷面積和焊錫膏厚度。對於早期的 DFM，設計者們需要對用 P-I-P 工藝去結合的元件加以確認。焊錫膏的尺度須提供給設計者，並且盡可能早的確認設計中所必需的錫膏印刷清潔區域。（**注意**：所有被確認的位置都應以錫膏面與墊片面比率爲 1：1。這將確保它們在鋼板設計中易於定位和改善。）

No vias, component pads or ground pads are allowed in the solder paste print area around the PTH component lead. Each PTH component location may require a different print area and thickness of solder paste. Early DFM needs to be done with the designers to identify components that will be attached using the P-I-P process . Solder paste dimensions need to be furnished to the designer as early in the design as possible to identify the required paste print clear area.(NOTE: All identified locations should be included in the solder paste layer at 1:1 with the pad . This ensures these will be addressed and modified in the stencil design).

• 元件要求適宜於回流焊。設計者務必要瞭解在 P-I-P 工藝中，哪些通孔元件可以爬上錫膏 ，從而能設計或指定能承受 240°C 的高溫元件。

Components are required to be reflow compatible. The designer needs to know which PTH components will be attached using the P-I-P process so he can design or specify high temperature components able to withstand 240^{o} C.

• 元件要求一個最小值爲 0.012[0.03]的支架。元件體支架對每個部件都是必須的，同時位於印刷面的外部。假如沒有足夠的支架高度，那麼在回流焊之後，元件體表面將被錫膏塗汙而導致焊錫球與短路。見例 4（圖 1）。

Components require a minimum of a 0.012[0.03] standoff . A component body standoff is required for each device and located out of the print area. If there is not adequate standoff height the solder paste will be smeared by the component body resulting in solder balls and solder shorts after the reflow process. See example 4(Figure 1).

• 像連接器那樣的多引線數元件，要求插腳陣列板，這是連接器設計的固有部分。陣列板應有 0.012[0.30] 高度的支架，如此，陣列板就不會接觸錫膏。

High lead count components like connectors require a pin alignment plate which is an intrinsic part of the connector design. The alignment plate should have 0.012[0.30] standoffs so the aligment plate will not contact the solder paste.

• 對叉鎖型保留式插腳，建議使用叉鎖型。 此將減少叉鎖厚度以維持面積比，同時提高孔內填充。叉鎖型保留式圓孔的直徑要求很大，錫膏易從孔內掉出來從而導致錫焊連接不充分。爲了減少 PCB 裝配問題，最小寬度在 0.030[0.75] 到 0.040[1.00]範圍的插槽很受歡迎。見例 5（圖 1）。

Slots (elongated holes) are recommended for fork lock type retention pins. This will reduce the fork lock thickness to hold area ratio and improve the hole fill. Round holes with a fork lock type retention will require too large of a diameter and the solder paste will fall out of the hole and result in an insufficient solder joint. To reduce PCB fabrication problems a minimum slot width of 0.030[0.75] to 0.040[1.00] is recommender. See example 5(Figure 1).

• 突出的元件引線長度應是從 0.010[0.25] to 0.030[0.75]。太長的引線會使焊接遠離電鍍通孔，這將導致焊錫 fillet 不充分。

Component lead protrusion should be from 0.010[0.25] to 0.030[0.75] long. Longer leads can push the solder too far from the plated through hole,which can result in insufficient solder fillets.

• 像 0603,0402,0201 小的表面貼裝元件和小的 r/c-paks 設置在距通孔墊片 0.075[1.90] 處，以考慮到 P-I-P 制程中套印 PIH 連接處的空間。

Small surface mount devices such as 0603,0402,0201 and small, should be placed 0.075[1.90] from through hole pads per Figure 2 to allow space for overprinting the PIH joint for the paste in hole process.

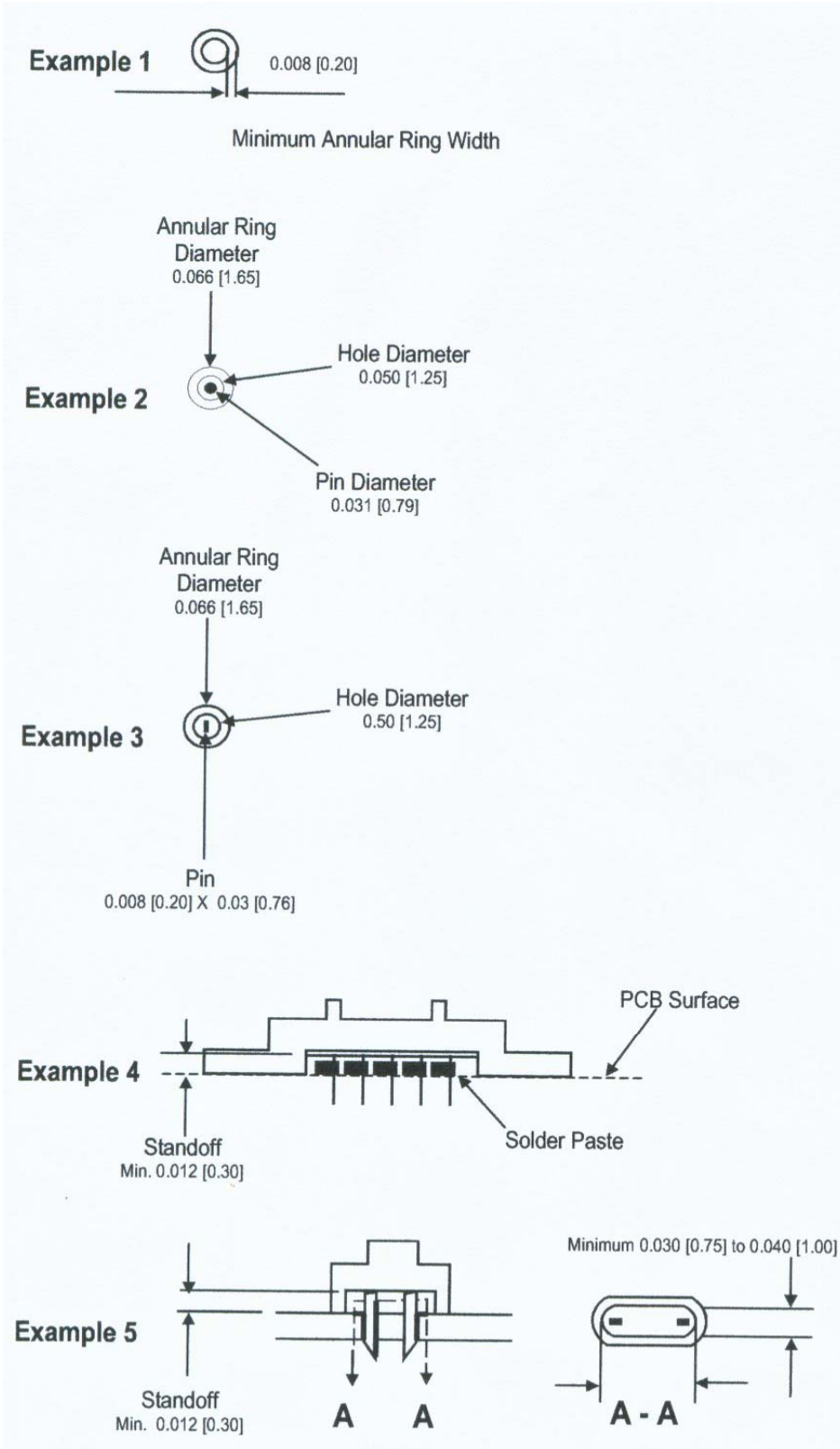


Figure 1-Examples of Pin-In-Paste Design Parameters

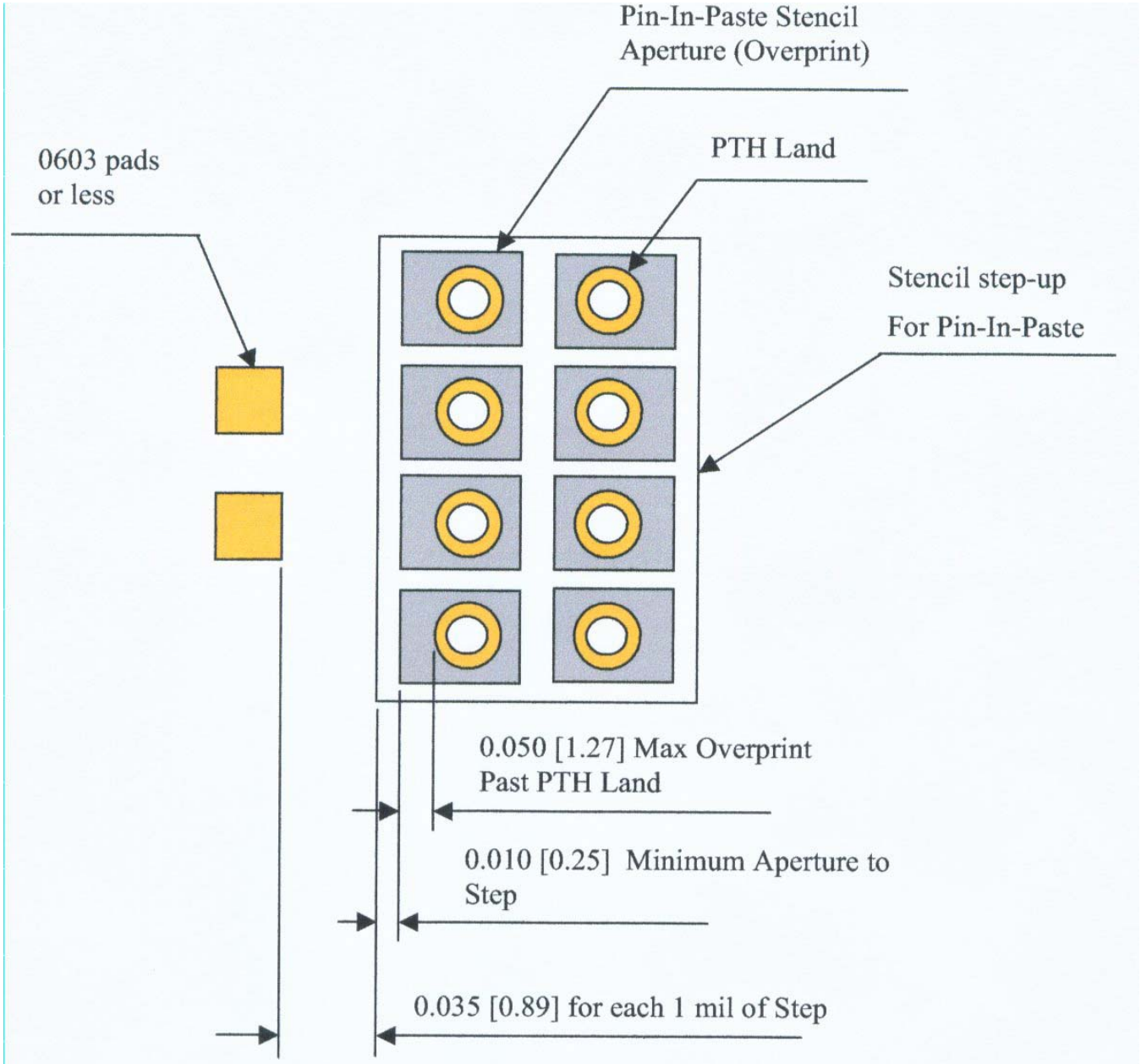


Figure 2-Examples of Pin-In-Paste Design Parameters

2.3 面板製作設計 Design For Panel Fabrication

2.3.1 簡介 Introduction

必須留心這部分的指導原則，要確保最低成本和最高品質的印刷電路安裝。

The guidelines in this section must be observed to ensure the lowest cost and highest quality printed circuit assembly.

PCB 可以在裸板面板上設計成一合一的或多合一型，此有賴於須組裝小板的

尺寸、形狀及數量，板上元件的類型及數量，PCB 的厚度。爲使生產時能進行有效的組裝，插卡小於 4.00[100.00] x 4.00[100.00]將更適合於面板化。（見圖 3）

Depending on size and shape,volume of boards to assembly, type and number of components on board, the PCB thickness-the printed circuit board (PCB) may be designed one-to-one (1-up) or many –to –one (x-up) on the bare board panel. Cards smaller than 4.00[100.00] x 4.00[100.00] will likely be panelized for efficient assembly in production .(See Figure3)

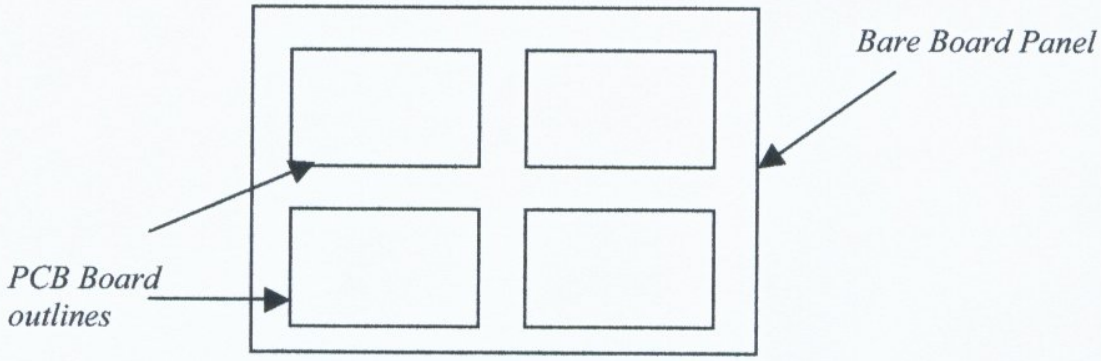


Figure 3-Printed Circuit Boards outlined on a Bare Board Panel (4-up configuration)

2.3.2 面板化的一般板尺寸相關因素 general board size considerations for panelization:

• 小板尺寸–小板的尺寸與形狀對板材原料成本有重要性影響。

Board Size – The size and shape of the board has a significant influence on the raw card cost .

• 首選最大小板尺寸爲 18.00[457.00] x14.00[355.60]。標準最大尺寸爲 20.00[508.00] x18.00[457.00]。在某一 Solectron 位置、要求特別設備與制程可以是更大的尺寸。（對任一特殊板的優先面板化，諮詢你們 DFM 工程師）

The preferred maximum card size is 18.00[457.00] x14.00[355.60]. The standard maximum size is 20.00[508.00] x18.00[457.00]. Larger sizes can be accommodated at certain Solectron sites and require special equipment and processing .(Consult your DFM engineer for the preferred panelization for any specific board.)

• 當關鍵性元件如 BGA/CSP 、微距、遮罩等組裝時，必須要考慮到相對於板厚度的

板寬度（在傳送器內）。DFM 團隊所包含的元件是重要的。

Width of the board (in the conveyor) relative to the board thickness has to be taken into account when critical components such as BGA/CSP,fine pitch,shielding,etc., are assembled. Early involvement by the DFM team is essential.

2.3.3 標準面板尺寸 Standard Panel sizes

工業中可用到的典型的面板尺寸是 12.00[304.8] x 18.00[457.00]x21.00[533.4], 18.00[457.00] x533.40] and 19.00[482.60]x 25.00 [635.00] 。更大的面板一般用到很少。基於電路板的形狀與尺寸，可以把幾個電路板製成在一塊面板上。只要使用下面的指導原則，將多重電路製成在一塊面板上可提高製造流程的成本效率。

Panel sizes typically available in the industry are12.00[304.8]x 18.00[457.00] x 21.00[533.4], 18.00[457.00] x533.40] and 19.00[482.60]x 25.00[635.00]. larger panels are generally lesss available. Depending on the sizes and shape of the circuit board , several circuit boards can be contained on one panel. Putting multiple images(x-up) on a panel can improve the cost effectiveness of the manufacturing process as long as the following guidelines are used.

2.3.4 面板化設計指導原則 Panelization Design Guidelines

- 在面板陣列中建立標準的加工孔位置，同時確定一個面作爲面板基準面。加工孔應可以從任一面對板進行安裝，同時，可在設備加工面上使用同一加工插腳設備。

Establish standard tooling hole locations in the panel array and establish one as the panel datum. Tooling holes should allow the board to be assembled from either side and use the same set of tooling pins on the machine toolings plates.

- 爲了使安裝更容易加工，選擇安裝小板的最小尺寸面板。Choose the smallest panel size on which the boards will fit in order to make the assembly easier to process.

- 對一塊面板上貼標籤的兩小板首選間距爲 0.093[2.40]+/-0.008 [0.20]（router 直徑）

preferred spacing between boards for a breakaway tab on the panel is 0.093[2.40]+/-0.008 [0.20] (router diameter).

- 在板的生產製成高處應預先佈線。

- Pre-routing should be done at the board fabrication shop underneath any overhanging beyond the end of the part by at least the amount of the radius of the slot.

- 每塊板至少應該有兩個最小半徑爲的 0.100[2.5]小孔。如果使用一個 router，則在面

板化制程中這些孔就很有用。

There should be at least two holes per board with a minimum diameter of 0.100[2.5]. These holes are used during the depanelization process if a router is to be used.

• 根據陣列的製圖量，在 PCB 裝配製圖中指定這些板子要在同一陣列中供應。

Specify on the PCB fabrication drawing that the boards are to be supplied in an array, according to the array drawing number .

• 受控的阻抗板要求爲 TDR 留有額外的間距。

Controlled impedance boards require additional space for TDR coupons.

2.3.5 必需的面板製圖尺寸 Required Panel drawing dimensions

所示面板的尺寸僅作參考，並不代表任一具體面板的尺寸。所示面板的尺寸僅作爲標準面板製圖所必需尺寸的指示而已（見圖 4）。

The panel dimensions shown are for reference only and do not represent the size of any specific panel. Dimensions shown are indicators only of the dimensions required to be shown on a typical panel drawing .(See figure 4)

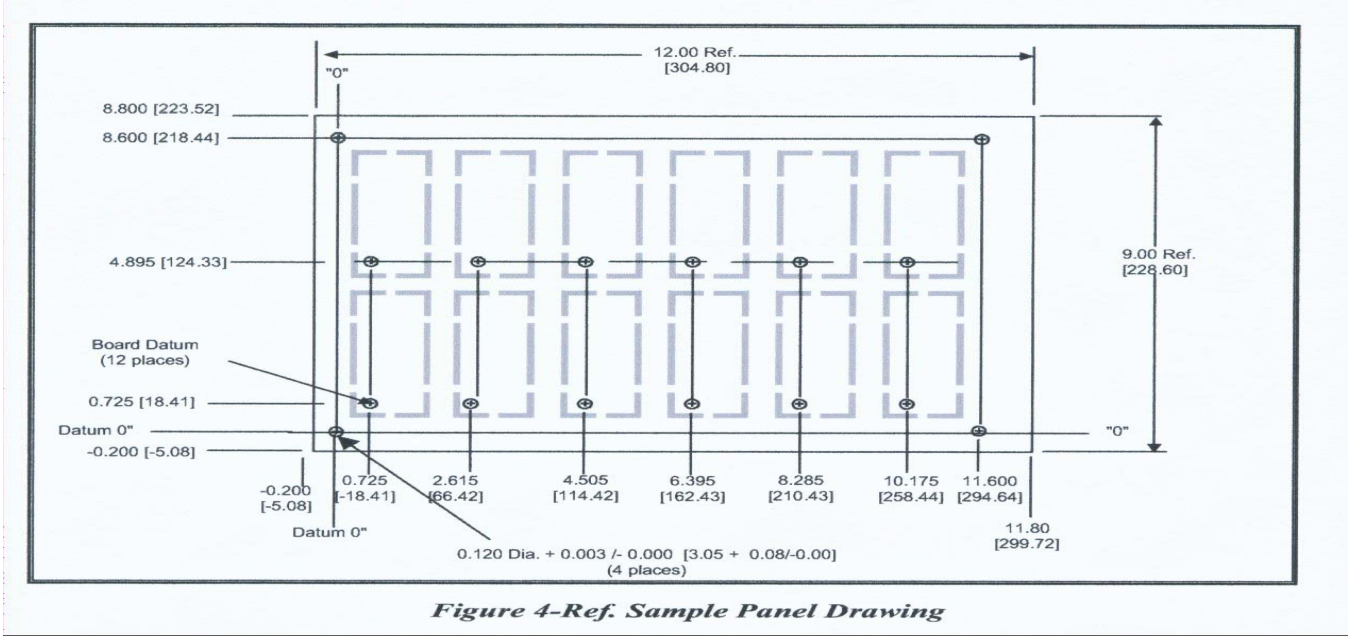


Figure 4-Ref. Sample Panel Drawing

2.3.6 陣列面板化分解 Dipanelization of Arrays

面板化制程在一塊面板上劃分了多個小板圖樣，這些小板圖樣就是一個陣列。陣列設計必須遵循間距指導原則 ，以使恰當的面板分列可行。

The panelization process puts multiple board images-an array –within the panel. The array design must adhere to spacing guideline to permit proper depanelization:

從面板上分割電路小板。特別指明的裝置通常要求面板分割。面板化分割方法包括：

Separating circuit boards from the panel. Specialized equipment is usually required for depanelization. Depanelization methods include :

• 佈線路法—每一塊獨立的小板的線路佈置來自面板。製作者或者將其留在面板內或者部分的布於板面。PCB 安裝必須完成佈線。這樣成本很高又費時，但對邊緣有陶瓷電容的小板來說，這是必需的。同時，在更厚些的安裝件中，多餘區域線路必須要布開來。要確保在佈線端面零件的高度不可高於 0.350[8.90] ，而線路端面在第二線路路徑中心線 0.775[19.70]的距離內。零件的高度超過尺寸就會撞到線路端頭並毀壞板子。

Routing method –the dididividual boards are routed from the panel. The fabricator will either leave the panel solid or partially route the board profile. The PCB assembly must perform or complete the routing. This is costly and time consuming, but is necessary for small boards with ceramic capacitors near the board edges. At times on thicker assembles the waste area must be routed away. Insure that there are no parts taller than 0.350[8.90] on the route head side that are within 0.775[19.70] of the centerline of the secondary route path. Parts taller than this dimension could hit the router head and damage the board.

• 線路與穿孔簽法－－機板供應商會沿著每一片 PCB 板留下間隔爲 2.00[50.00]的連接孔簽，以維持小板仍鑲於面板內。爲了使安裝後易於分離，在每一個 tab 處都設計了鑿孔模式。見 Route and Tab 法圖表選項”A” 和 “B”，此是爲厚度小於的 0.093[2.40]且大一些的小板設計的（圖 5、6）。元件與線路須在匣孔周圍區域的外部（見圖 8）。爲防止損壞元件和線路，要保持下面的間距：

Route and perforated Tab method- the board vendor will route around each PCB board,leaving connecting tabs 2.00[50.00] apart on each edge to hold the board within the panel. Each tab has a perforated drill pattern design for easy separation after assembly. See Route and Tab Method diagram(Figure 5and 6) option”A” and “B” for card less than 0.093[2.40] thick and greater. For component and trace line keep out areas around the perforated tabs see figure 8. To prevent damage to components and trace lines maintain the following clearances:

• 所有的 1206 尺寸的陶瓷零件或更小的與 RNETS 距穿孔處 0.150[3.80]的最小距離。

All ceramic parts 1206 size or smaller and RNETS should be a minimum of 0.150[3.80] from perforations .

• 更大尺寸的晶片與 RNETS 應距穿孔最小距離爲 0.350[8.90] 。 排列任一有軸、大於 1206 的陶瓷零件，要與穿孔線相平行。

Larger chips and RNETS should be a minimum of 0.350[8.90] from perforations. Align any ceramic part larger than 1206 with the axis parallel to the line of perforations.

追蹤線與引腳連線應距離穿孔爲 0.062[1.60]的最小值。

Trace and leaded components should be a minimum of 0.062[1.60] from the perforations。

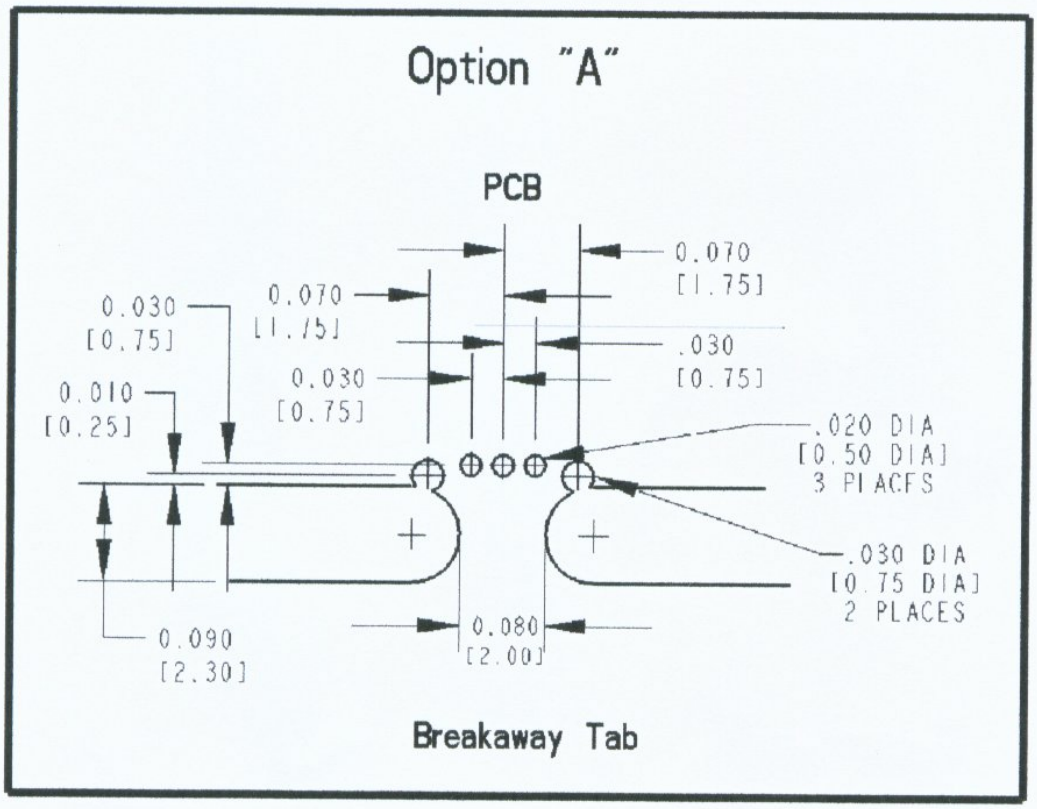


Figure 5-Route and Tab Method of Depanelization (Option A)

注意:分離完成後,這種分離模式防止了任一板材突出所定義的小板之外。 **Note :** This breakaway pattern prevents any board material from protruding outside the defined board edges after the break has been performed.

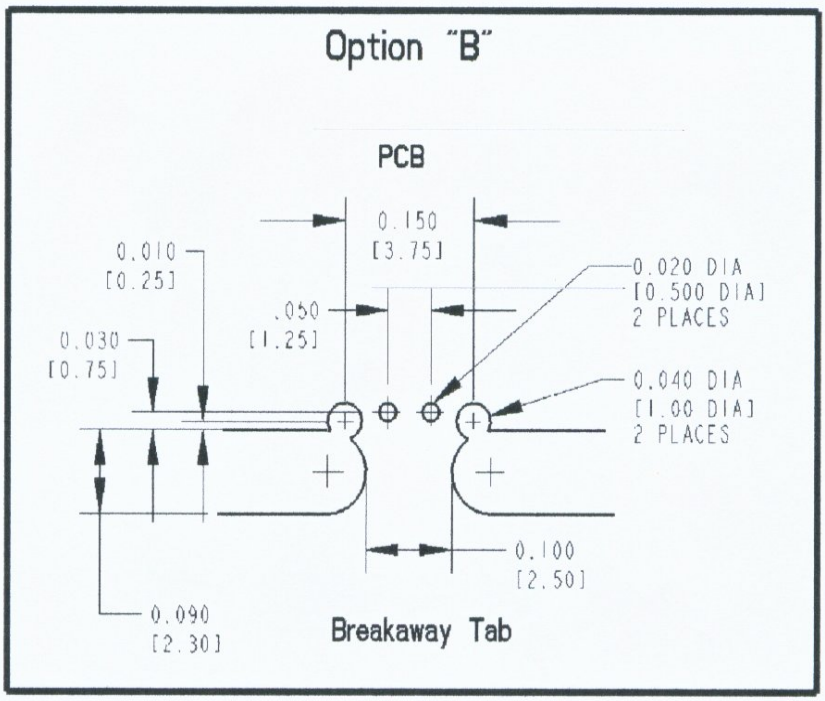


Figure 6-Route and Tab Method of Depanelization (Option B)

Note: *This breakaway pattern prevents any board material from protruding outside the defined board edges after the break has been performed.*

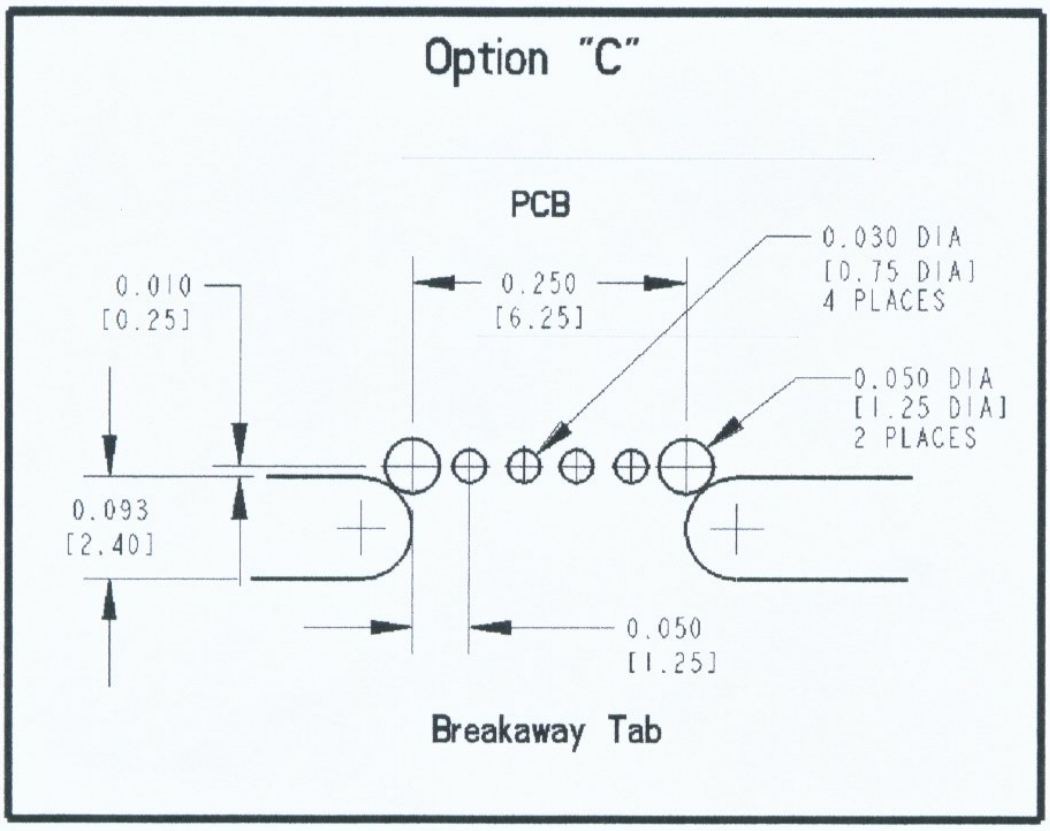


Figure 7-Option "C" Breakaway Tab for Thick Cards .094" and Greater

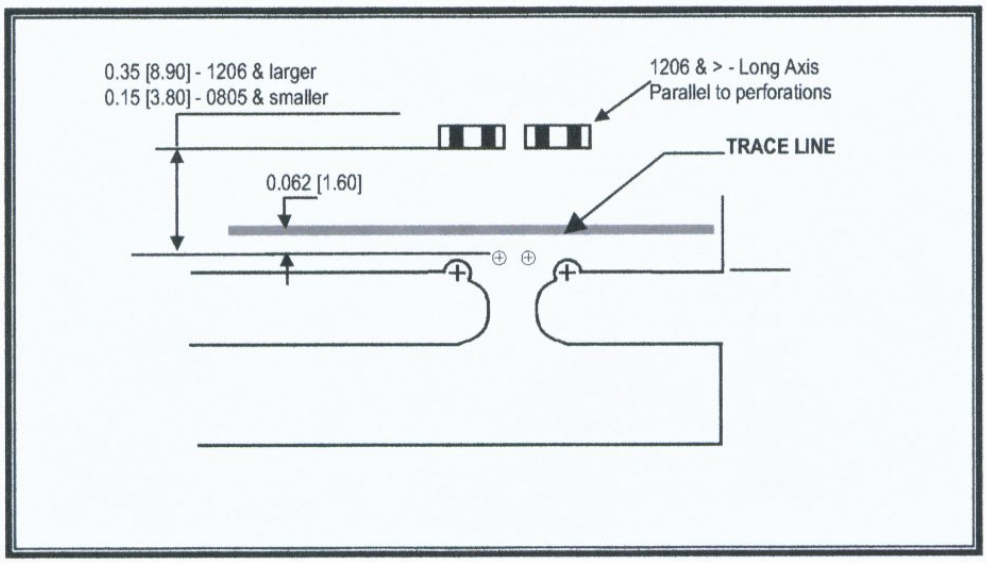


Figure 8-Component and Trace Line to Pre-Route Clearance

• 刻錄法–刻錄是許多事項一種功能，諸如材料類型，材料厚度，陣列圖間距以及需要多靠近的刻錄線。一個好的刻錄，可以允許手很容易的將小板與面板分開，但如果板太薄，則在焊接制程中會弄彎（例如彎折）。重的元件如板或陣列中心的變壓器就需要一個附加的固定設備以支撐此加工。

Scoring –Scoring is a function of many things-such as material type, material thickness,spacing of array images and how close the score lines need to be. A good score allows for the board to break off easily by hand but if the board is too thin it may warp during the coldering process (i.e. bow or bend). Heavy components such as transformers in the center of board/array could require additional fixturing to support the process.

• 在可能的地方刻錄直線。PCB 形狀比較複雜的情況下，刻錄法是不精確的。刻錄法與與佈線路法的結合也許是必須的。

Always score in straight lines where possible. Scoring is not accurate in the case of complex PCB shapes. A combination of scoring and pre-routing may be necessary.

• 刻錄法不允許交叉基準、不合格標記、開脫的標籤或加工孔。材料成本必須考慮到任一刻錄輪廓。

Scoring is not allowed across fiducials, reject marks, breakaway tabs or tooling holes. Material costs must be considered for any scoring outline.

• 要意識到任一客戶對品質優勢的要求。決定是否機器切割更適合於保持一個好的

品質優勢而沒有缺陷。

Be aware of any customer requirements for edge quality. Determine if machine cutting is more appropriate to maintain a good quality edge without burrs.

• V 切割或刻錄—對 0.062[1.60]的厚板來說，用刻錄將小板與面板分離是一可行的方法。槽是沿著板兩面的輪廓線切割出的。然後，用合適的切割或鑽孔設備沿著面板上的刻錄線將小板分離出。

V cuts or scoring –For 0.062[1.60] thick boards, scoring is a visible approach for separating the boards from the panel. Grooves are cut along the line of the board profile on both sides of the board. The boards are then separated with appropriate equipment or tooling alone the score line from the panel.

• 分離刻錄—裸板供應商會完成刻錄，就如上說的，有代表性的選用 Lihr Hermann 機器。切割的最大長度爲 24.00 [60.960]。在可用的面板區域內，有三個要求的加工孔，通過銷將面板連接到機器上。跡線必須離刻錄中心線至少 0.060 [1.50]，離分離鑽孔邊沿 0.0025[0.65]。刻錄線寬度是深度的大約 1.15 倍。

Breakaway Scoring – The bare board vendors can perform scoring as described above, typically using a Lihr Hermann machine. The maximum lenth of cut is 24.00[60.960]. Three tooling holes are required inside the usable panel area for pinning the panel to the machine. Traces must be at least 0.060[1.50] away from center line of the score and 0.0025[0.65] away from the edge of the breakaway drilled holes. The width of the score line is approximately 1.15 times the depth.

• 推薦的刻錄深度爲材料厚度的 30-33%。Web 厚度的標準值爲 0.062[1.6]，FE-4 板的爲 0.016[0.40]（見圖 9）。

Recommended scoring depth is 30-33% of material thickness. The typical value for web thickness for 0.062[1.6] FR-4 board is 0.016[0.40].(See Figure 9)

• 確保所有尺寸爲 1206 或小些的陶瓷零件（電容，電阻 RPaks 等）距刻錄線 0.150[3.80]，同時確保所有大於 1206 尺寸的零件距刻錄線爲 0.250[6.35]。將任一尺寸大於 1206 的陶瓷零件沿軸平行於刻錄線排列。跡線應距刻錄線 0.062[1.60]，被連接元件應距刻錄線 0.075[1.90]。

Keep all ceramic parts (capacitors , resistors, RPaks,etc.) 1206 size or smaller 0.150[3.80] from the score line, and ceramic parts larger than 1206s 0.250[6.35] from the score line. Align any ceramic part larger than 1206 with the axis parallel to the score line. Trace lines should

be 0.062[1.60] from the score line and leaded components should be 0.075[1.90] from the score line.

例如 Example

Z = 厚度範圍 0.030”到 0.125” Thickness range 0.030”to 0.125”

Y = Remaining score web, typically 0.016”[0.40]

X = 刻錄尺寸資料（公差=“F”） Dimension of datum to score line (tolerance =”F”)

W =未注明；不受控 Do not specify ; cannot be controlled

V = 未注明；刻錄線的寬度隨整體厚度的改變而改變。

Do not specify; width of score line wi ll vary as overall thickness changes.

F = 注明 v-切割的最大偏移量 0.005[0.125] Specify v-Cut maximum offset to be 0.005[0.125]

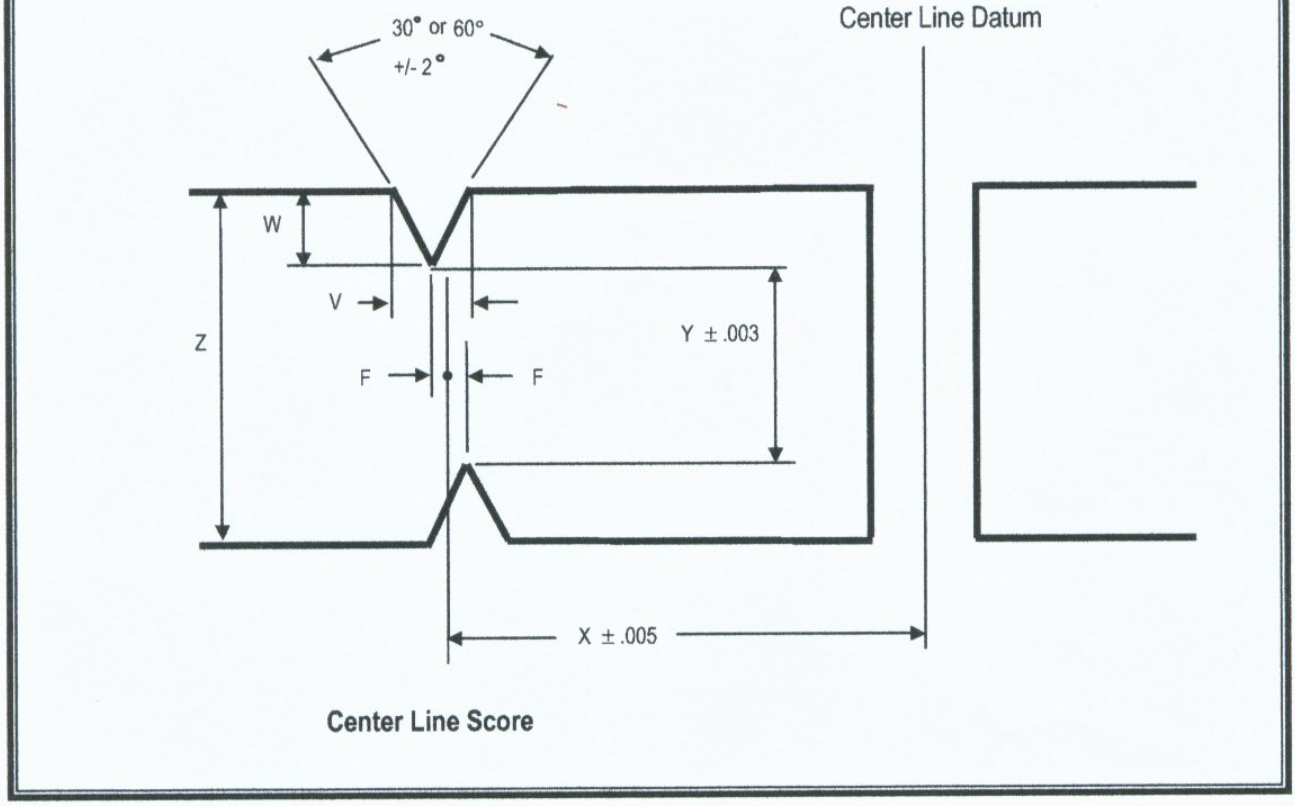


Figure 9-Breakaway Scoring diagram

2.3.7 對小板與面板的安裝與測試加工孔指導原則 Assembly and Test Tooling Hole Guidelines for Boards and Panels

• 爲便於在安裝與測試制程中記錄與排列，所有的小板都要求有加工孔。

All boards require tooling holes for registration and alignment in the assembly and test process.

• 爲便於在安裝與測試制程中記錄與排列，所有的小板都要求有加工孔。（見圖 11）

All boards require tooling holes for registration and alignment in the assembly and test process. (See figure11).

• 因爲必須預備好異常狀況下測試插卡，所以，即使面板或 breakaway tabs 已用過，插卡本身必須含有加工孔

Because there must be a provision to test the card singularly, tooli ng holes must be included in the card itself, even if a panel or breakaway tabs are used.

• 兩加工孔必須置與 PCB 上相對的拐角處，並離得盡可能的遠。須有三個首選加工孔。

Two tooling holes must be placed in the opposite corners of the PCB as far apart as possible. Three tooling holes are preferred.

• 沒有零件可置於加工孔邊緣 0.200[5.00]的範圍以內，或者從安裝測試點邊上 ICT 加工孔中心線 0.250[6.35]半徑的範圍內 。

No parts should be placed within 0.200[5.00] from the edge of the tooling hole or 0.250[6.35] radius from the ICT tooling hole center line on the test piont side of the assembly.

• 加工孔中心在(X 和 Y)上，距板的每個拐角處必須爲 0.200[5.08] 。 板上有三個孔的，孔位置成爲“X” 到 “Y”的基準面，它們的交點指定爲 0，0。

The tooling hole center must be 0.200[5.08] in (X and Y) from each corner of the board. With three holes,the locations become “X” to “Y” datums with their intersection designated as 0,0.

* 當元件放置於板的兩面，應定位出加工孔，如此在板翻轉進行第二面的安裝時仍可使用治具或 SMT 設備上的那套同樣的加工插腳，而這套插腳正是第一面安裝時所使用的。

When components are placed on both sides of the board,the tooling holes should be located so they allow the board to be flipped over for the second side assembly and still utilize the same set of tooling pins in the fixture or SMT equipment as was used for first side assembly.

• 板上加工孔將是非電鍍的，並且直徑爲 0.120[3.05] +0.003[0.08]/-0.000”。高度密集的設計或較小的插卡可以帶有半徑爲 0.093[2.40]加工孔。一個可供的 選擇方法是使用一個孔和一個小長氣泡插槽。插槽的最小長度應是孔直徑的兩倍。（見圖 10）

Board tooling holes are to be non-plated and have a diameter of 0.120[3.05] +0.003[0.08]/-0.000”. Very dense designs or smaller cards can have tooling holes with a diameter of 0.093[2.40]. An alternative is to use a hole and an elongated slot. The slot minimum length should be double the diameter of the hole.(See figure 10).

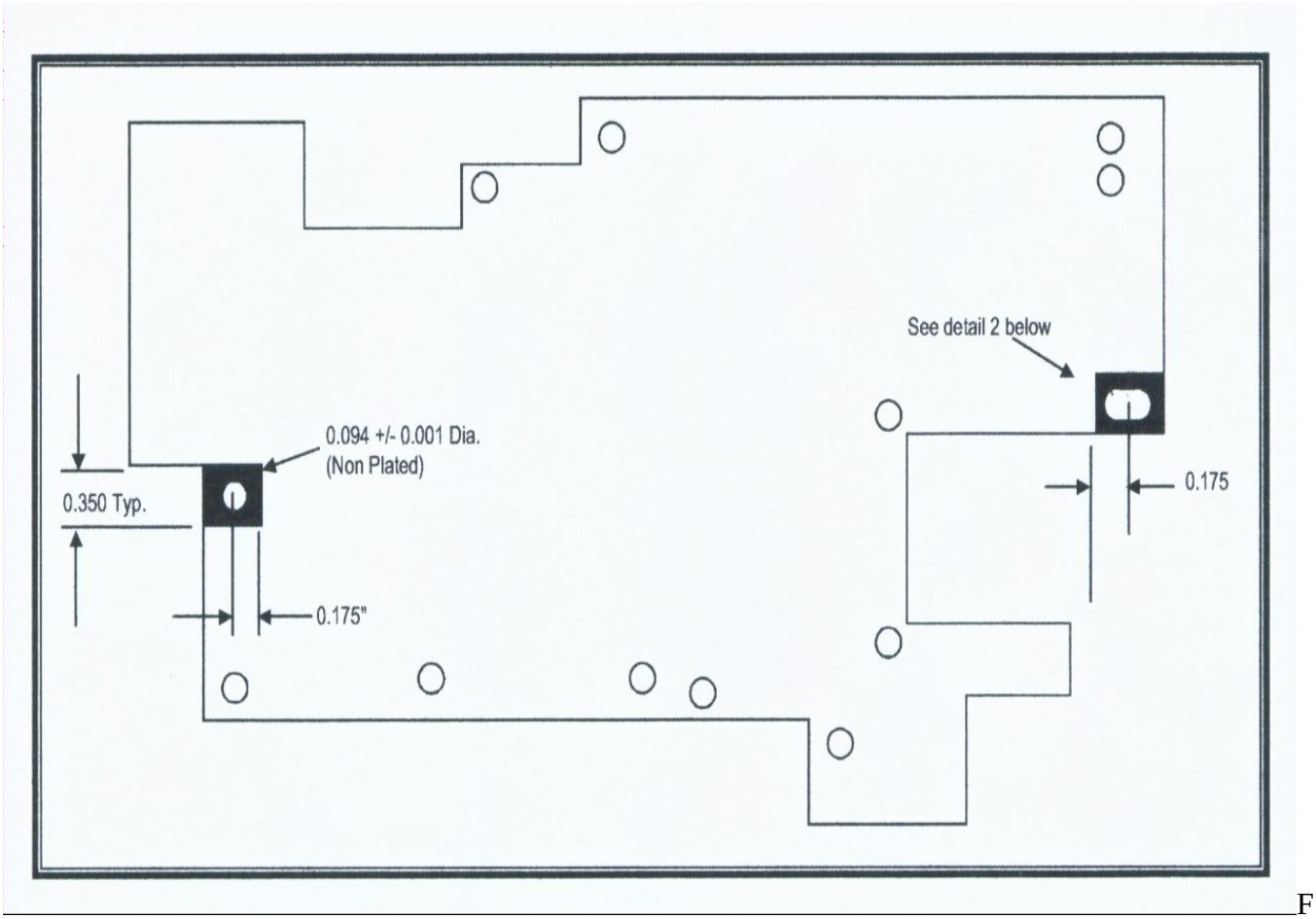
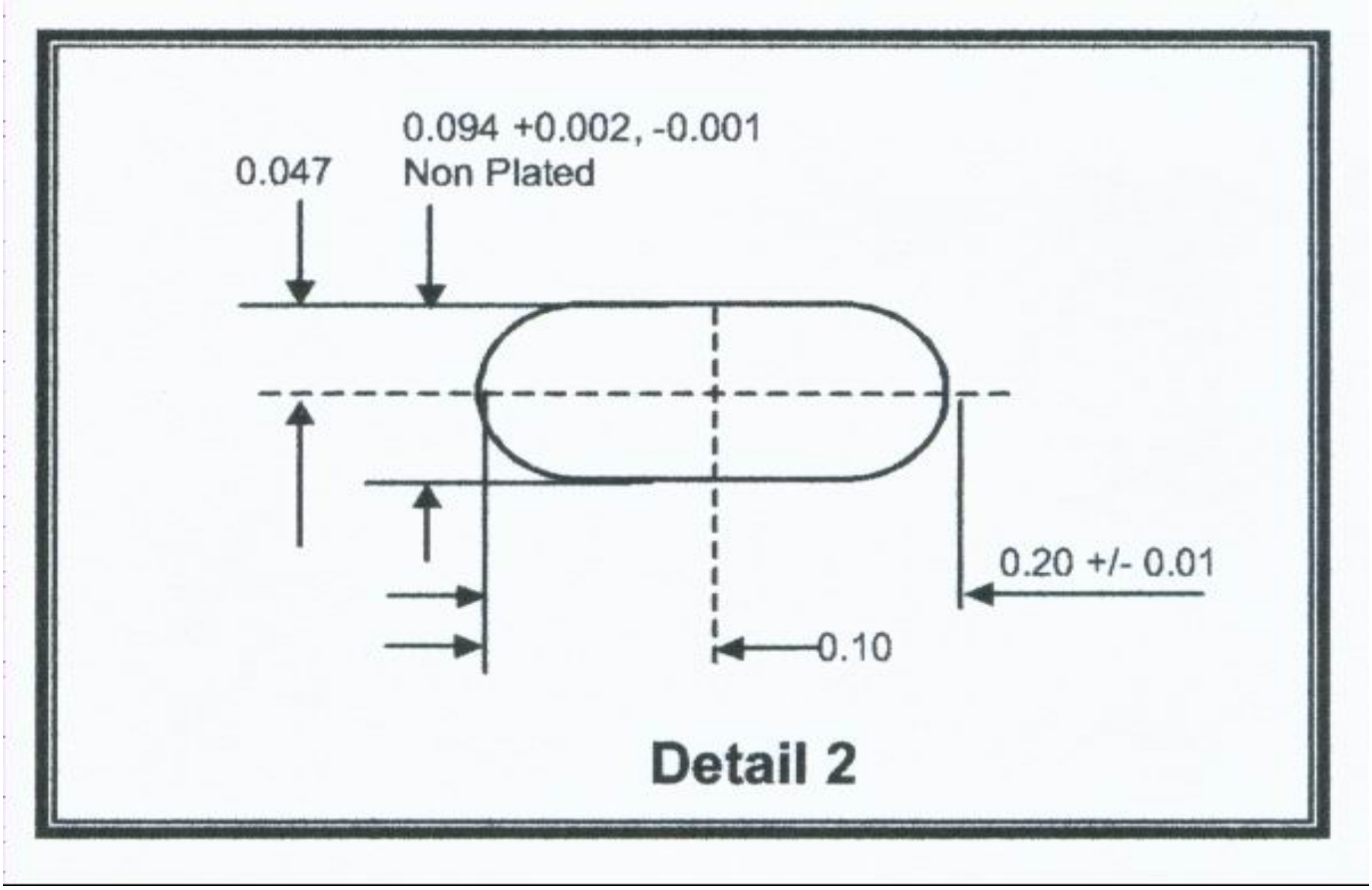


Figure 10-Basic Tooling Hole and Slot Recommendations for Cut Card



備註： Note:

制程工程師能多角度核查加工孔與插槽的位置。

Location of tooling hole and slot can vary-review with Process Engineer.

現實的加工孔與插槽的尺寸可以隨著產品設計的要求而變化。

Actual tooling hole and slot dimensions can vary with product design requirements.

在安裝制程期間，切削卡通常裝在機件板上。

Cut card are usually held in a work board during the assembly process.

元件不能放置於兩個地方（圖 10 中所指示的兩個黑盒子處）。

Components cannot be placed in the two areas indicated as black boxes in figure 10

2.3.8 面板指導原則應包括： Panel guidelines should include:

- 裸板結構特徵如面板尺寸內外層規格、孔與槽的規格。

Criteria on bare board physical characteristics such as panel size ,inner and outer layer specifications,hole and slot rules.

- 針對穩定性、被覆蓋金屬的相關因素和麵板化、面板分割而需調節銅箔均

衡規則

Rules governing copper balance for stability ,plating considerations and panelizing and de-panelizing.

• 功能性特徵標準如加工孔，基準，通道，環孔，定尺寸，soldermask，表面抛光和絲網遮罩。

Criteria for functional features such as tooling holes ,fiducials,vias ,annular ring, dimensioning ,solder mask,surface finish and silk screening .

• 目前所施行的線路與熱量的舒緩控制的局限性，其結構特徵的相關因素。

Considerations for physical attributes of current carrying limitations of the traces and thermal relief management .

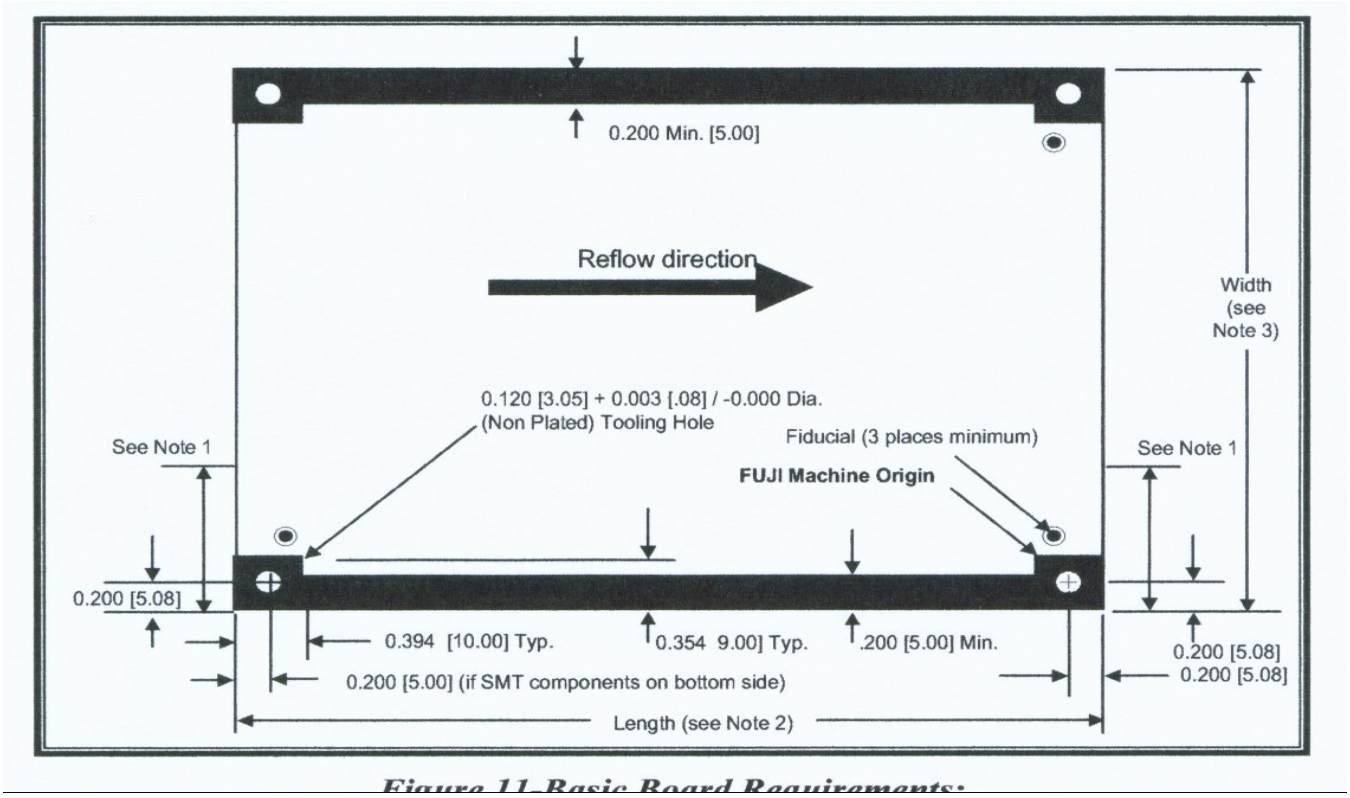


Figure 11-Basic Board Requirements:

Figure 11-Basic Board Requirement:
A summary of component ,tooling hole, and fiducial placement.

圖 11 注意點： Notes: (for figure 11)

1・底面主要拐角處剪切塊不可超過 1.00[25.00] 。

No cutouts allowed for 1.00[25.00] on bottom leading corners

2・小板長度：3.94[100.00]min.20.00[508.00]max

Board length:3.94[100.00]min.20.00[508.00]max.

3・小板寬度：2.36[60.00]min.-18.00[457.20]max

Board width:2.36[60.00]min.-18.00[457.20]max.

4・元件不可放於所示的黑盒子內（雙面）

Components cannot be placed within the areas indicated with black boxes (both sides).

5·底面右手邊位置和任一頂端位置必須是一個孔。其餘兩個安裝孔位置可以是個插槽。

Bottom right hand position and any one top position must be a hole. The rest of the other two mounting hole positions may be a slot.

2.4 基準指導原則 Fiducial guildelines

2.4.1 簡介 Introduction

在裸板上，基準是目的，因爲它爲拾取放置設備的機械顯示系統提供了參考。既有覆蓋全部機板的整體基準，也有涵蓋個別設置的局部基準。

Fiducials are targets on the bare board that provide a reference for machine vision systems in pick and place equipment. There are both “global” fiducials covering the entire board and “local” fiducial covering individual devices.

2.4.2 整體基準 Global Fiducials

• 在具有 SMT 元件插卡的每一面上進行 SMT 元件顯示與放置時，所有的板子必須具有光學整體化基準目標。

All boards must have optical global fiducial targets for SMT screening and placement on each side of the card that has SMT components.

• 必須有三個整體基準覆蓋插卡或面板（兩個最小的是關於一種小插卡）。典型地，這些基準位於鑽孔中心、最小值爲 0.250 [6.35] 的地方。一般來說，這些基準在插卡兩面同樣的位置處。 注意：確認該模式不是對稱的以預防加工一張帶有修正或顛倒了上下方向的插卡。（見圖 11）

There must be three global fiducials(two minimum on a small card) to cover the card or panel. Typically these fiducials are locate near the tooling holes,a minimum of 0.250 [6.35] from the center of the hole. Generally these fiducials are at the same location on both sides of the card. Causion: ensure the pattern is not symmetrical to prevent processing a card with a revised or upside down orientation.(See Figure 11)

• 包括元件放置資料中的基準位置，以使放置設備能更精確的放置它們。

Include the fiducial locations in the component placement data to allow the placement

equipment to more accurately locate them。

• 包括焊接膏層內的整體基準位，以便將它們當作目標包括在錫膏模版中。

Include the global fiducial locations in the solder paste layer so they can be included as targets in the solder paste stencil.

• 此整體基準中心應是距插卡邊緣爲 0.250[6.35]的最小值。如果插卡邊緣不用於該制程的的卡片傳輸，則距離可以爲 0.120[3.00] 。

The global fiducial center should be a minimum of 0.250[6.35] from the card edge. The center may be 0.120[3.00] from a card edge if that edge is not used to convey the card through the process.

• 基準中心將是距非電鍍孔邊緣 0.100[2.50] 的最小值。

Fiducial centers shall be a minimum of 0.100[2.50] from the edge of a non-plated hole.

2.4.3 局部基準 Local Fiducials

• 應有一套局部基準，其範圍在 BGA 元件或細孔（(0.020[0.50]或更小)的 2.00[50.00]半徑內。這套基準必須在設置的相對的拐角處。相臨基準的兩孔中心距不少於 0.200[5.00] 。

There should be a pair of local fiducial within a 2.00[50.00] radius of fine pitch (0.020[0.50] or less) or BGA device. This pair must be at opposite corners of the device. Adjacent fiducials must have a no less than 0.200[5.00] center to center.

• 有一個節省板上空間的方法就是佈置基準，這樣就可以安裝不止一個元件了。這是通過一組設置周邊的兩對角線的基準來做到的。這些基準必須都要在 6.00 [150.0]之內。

An alternate method that can save board space is to place the fiducials so that they are used by more than one component. This is done by two diagonal fiducials around a group of devices. These fiducials must be within 6.00[150.0] of each other .

• 元件基準必須是應用於 0.016[0.40]或以下間距的元件。

Component fiducials must be applied to 0.016[0.40] pitch devices or below .

• 不要將基準安置在會被元件覆蓋的地方。因此，基準不該在設置的中央處。

Do not place fiducials in a location where they will be covered by components. Therefore ,fiducials should not be in the center of the device.

2.4.4 基準的選擇 Fiducial options

• 首選的整體基準類型是在 0.120[3.00]半徑的空白區域內的一半徑爲 0.040[1.00]的圓點。局部基準應與整體基準是同樣的尺寸與區域；而一個 0.080[2.00]的區域也是許可的。此區域內不可有 soldermask，銅或鋼絲印刷網。也不該在層上有任何的銅直接位於基準之下，從而在區域內清晰可見。基準面板和區域的例子如圖所示：

The preferred global fiducial style is a 0.040[1.00] diameter dot in a 0.120[3.00] diameter clear area. The local fiducial should be the same size and clear area as the global fiducial; however,an clear area is permitted. The clear area should not contain any solder mask , copper or silkscreen. There should also not be any copper on the layer immediately beneath the fiducial as it will be visible in the clear area. An example of fiducial pad and clearance is shown as:

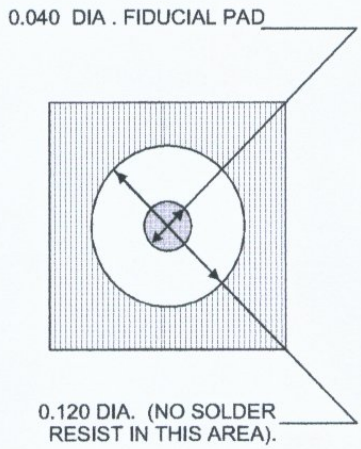


Figure 12- Preferred Global Fiducial

帶有 HASL 表面抛光板的輪換基準，是在基準孤立的地方使用一種圓環類型。這在 HASL 應用中起到了保護基準的作用。該區域圓環的尺度爲 0.089[2.25] OD ,0.039[1.00] ID, 和一個 0.095[2.40]半徑的區域。不能含有任何的 soldermask、銅或鋼絲印刷板。基準面板和相應的 soldermask 間距的例子如圖所示。

The alternate fiducial style for boards with HASL surface finish is to use a donut style where the fiducial is isolated. This protects the fiducial during the HASL application. The donut dimendsions are 0.089[2.25] OD ,0.039[1.00] ID, and a 0.095[2.40] diameter clear area. This clear area cannot contain any solder mask,copper, or silkscreen. An example of a fiducial pad and the associated spacing of the solder mask are shown as:

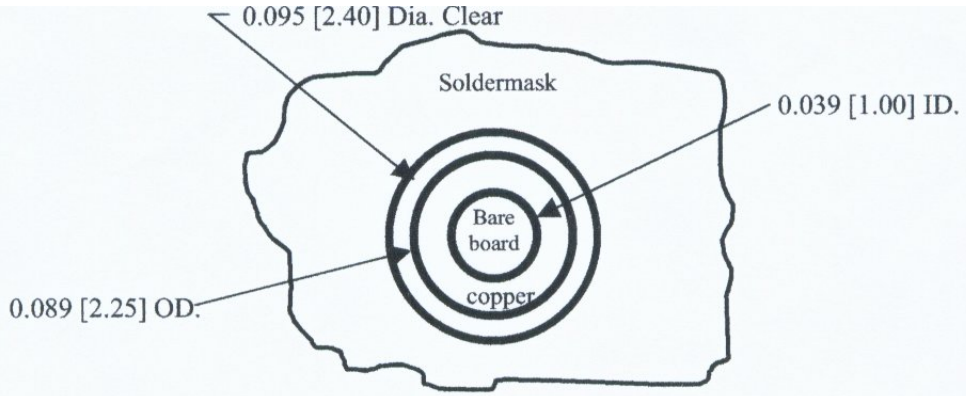


Figure 13- Alternate Style for an Isolated Fiducial

2.5 表面拋光　Surface finishes

2.5.1 簡介　Introduction

表面拋光爲銅線的外層提供了一層保護層以防氧化。在機板組裝生產期間要求爲提供最可能好的焊接條件所作的努力，有水平熱空氣焊接水準測量，有機覆蓋層（典型的 Entek 106A)，非電鍍鎳上浸金（RNIG），浸錫和浸銀，每一種不同類型的拋光都會對這些努力有其正面和負面的影響 。向你 當地的 DFM 代表諮詢基於該卡片目錄中的表面拋光建議。

A surface finish provides a protective coating over the outer layers of copper to prevent oxidation. Each different type of finish has its own positive and negative impact on the effort required to provide the best possible soldering conditions during the board assembly yields are Horizontal Hot Air Solder Leveling(H-HASL), organic coatings (typically Entek 106A), immersion gold over electroless nickel(ENIG), immersion tin, and immersion silver. Consult your local DFM representative for a surface finish recommendation based on the content of the card.

2.5.2 表面拋光類型　Surface Finish types

- HASL 一種表面和孔的軟焊料沉浸與熱空氣水平測量法，可在裸露的銅表面預先覆蓋一層錫。 HASL (Hot Air Solder Level) a molten solder immersion and hot air leveling of surfaces and holes to provide a “pre-tinned” coating on explosed copper surfaces.

  ＊ 被覆金屬厚度：見圖 12　　Plating thickness: See figure 12

＊ soldermask 之後的應用　　Applied after solder mask

＊ 共溶焊接點--63% tin 和 37%　　lead Eutectic solder-63% tin and 37% lead

*熔化油與助焊劑的使用　　Fusing oils and corrosive fluxes are used

*表面不像 OSP 與 NI/AU 一樣 是一個平面或扁平面

Surface is not an uniform or flat as OSP and NI/AU

*HASL 不是一個有關某一插卡的選擇，該插卡具有 0.016 [040] 或更小的元件或者小於 0.8mm 的插腳間距。

HASL is not an option on cards that have devices with a 0.016 [040] pitch or less or for ‹ 0.8mm pitch BGA’s.

•（有機覆蓋層）ENTEK(106) 和 ATT-imidazoles 是一個有光澤的有機體保護層，該保護層建於有機元件之上、含水的。 如此有選擇的連接銅片以提供一種有機金屬層，從而對銅層起保護作用。

(Organic coating). ENTEK(106) and ATT-imidazoles are anti-tarnish organic coatings which are water based organic compounds that selectively bonds with copper to provide an organicometallic layer that protccts the copper.

＊ 爲焊接提供一個扁平的平面表面

Provides a flat uniform surface for soldering SMTs

＊ OSP（有機體焊接性）是最常用的有機體抛光

OSP(organic solderability)is the most common organic finish.

＊ OSP Entek 106A 正常的厚度 （見圖 12）

Nominal thickness of OSP Entek 106A(See figure 12)

＊ 在會影響生產收益的測試制程期間，當通過 Entek 進行探測時就要求特殊的探針。一個可供選擇的方法是在測試點上篩選含水的可溶性焊錫膏。通過孔的測試點不必填滿焊料，以免引起焊料腫塊 。

Special probes are required when probing through the Entek during the testing process which will impact production yields. An alternative is to screen water soluble solder paste on the test points. Testpiont via holes must not be over filled with solder to cause solder bumps .

＊ 在波動焊接制程中，孔填充問題要面對沒有清潔工藝使用情況。這促使

了通孔焊接中清洗工藝的使用。

Problems with hole filling are faced when no-clean process is used during solder wave operation. This induces the use of clean process for plated through hole soldering.

* 成本與 HASL 等效。 Cost is equivalent to HASL.

• Ni/Au(ENIG-無電鍍鎳浸金) 一雙層金覆蓋的鎳金屬表層通過一種化學沉積工藝將其鍍到銅基體上。

Ni/Au(ENIG-Electroless Nickel Immersion Gold). A two –layer gold over nickel metallic surface finish plated onto the copper base by means of a chemical deposition process.

* 封蓋所有裸露的銅表面 。 Encapsulates all exposed copper surfaces
* 被覆蓋金屬的厚度：見圖 12 For Plating Thickness: See figure 12
* 成本不是關鍵的，但比 HASL 和 OSP 更昂貴 。 Cost is not significantly more expensive than HASL and OSP
* 極好的表平面利於焊接。 Execellent surface flatness for soldering devices
* 由於焊接與黑墊片問題，在 BGA/CSP 元件安裝時 ，不推薦使用無電鍍 Ni/Au。

Electroless Ni/Au is not recommended when BGA/CSP components are assembled due to solderability issues and black pad problems.

• 沉浸錫（無鉛塗層）---直接在銅基體上塗一薄層 。此錫爲貼裝某些表面元件提供了極端平坦的平面。此類表面元件爲 0.016[0.40] 或更小微距的元件或是‹ 0.8mm 間距的 CSP 元件。

Immersion Tin (non-lead finish) – plates a thin layer of tin directly on the copper base. The tin provides an extremely flat surface for mounting surface components with ultra fine pitch devices of 0.016[0.40] or less or for ‹ 0.8mm pitch CSP’s.

* 開始時有極好的可焊性 Excellent Solderability when fresh
* 非常平的表面 Very flat surface
* 無鉛塗層 A non-lead finish
* 短保存期 Short shelf life

沉浸銀（無鉛塗層）--直接在銅基體上塗一薄銀層。此塗層產品有一非常平坦的表面，對 0.016[0.040]或更小的微距 SMD 陣列或者對‹0.0315[0.80]間距的 CSP 都非常理想，同時甚至在多次加熱迴圈後仍能保持高的焊接性。

Immersion Silver (non-lead finish)-plated a thin payer of silver directly on top of the copper base. The finish product produces a very flat surface ideal for fine pitch SMD arrays of 0.016[0.040] or less or for ‹0.0315[0.80] pitch CSPs and maintains high solderability even after multiple heat cycles.

＊ 極好的焊接性（好於 OSP）	Excellent Solderability (better than OSP)
＊ 極平坦的表面	Very flat surface
＊ 一年的保存期	1 year shelf life
＊ 無鉛塗層	A non-lead finish
＊ 能承受多次洄流焊制程步驟	Can withstand multiple reflow process steps

Characteristic	HASL	OSP	Electroless Ni/ Immersion Au	Immersion Tin (Non-Lead)	Immersion Silver (Non-Lead)
Shelf life	Good	Fair	Good	Short (dissolution into Cu in storage)	One year
Handling	Normal	Finger print concerns in Cu	Normal. Max. 24 hour between 2 reflows	Some handing Issues	Sensitive to corrosion
SMT land surface topology	Difficult to achieve planar surface	Very Flat	Very Flat	Very flat	Very Flat
Multiple assy reflow cycles (SMT, wave)	Fair - (an increase of intermetallics with each reflow cycle. Sensitive to HASL thickness)	Fair -(depends on OSP thickness) Maximum 24 hour between 2 reflows	Good - Recommended less than 24 hours between 2 reflows	Fair - (Similar to OSP) narrow window for muti-pass reflow	Good - can withstand multiple reflow process steps
Soldering fluxes & atmospheres	No concerns	May require more aggressive fluxes and/or N2 atmosphere	No concerns	No concerns	No Concerns
Use on thick PCB	Barrels difficult to fill and clear	PTH hole fill concerns	Improved barrel reliability	No plugged holes produced	No plugged holes produced
Use on Thin PCB	NO (risk of warping)	Yes	Yes	Yes	Yes
Solder joint reliability	Good	Good – (Cu/Sn provides strong solder joint	BGA "blackpad concerns/brittle solder joints	Good	Good
Pressfit compatibility	Tin/lead finish on pressfit parts	Reliability concerns with dissimilar material contacts	Gold finish required on pressfit parts	Non-lead finish required on pressfit parts	Non-lead finish required on pressfit parts
Card edge contacts	Additional plating operation	Additional plating operation	Additional plating operation	Additional plating operation	Additional plating operation
Test point bonding	Good	Poor	Good	Good- (initial surface)	Good- (for ICT)
Coating thickness	1 to 25µm on SMT pads	0.3 - 0.4 µm	0.05 to 0.15 µm	1.0 to 1.5 um	0.1 to 0.4 um
Cost	Low Cost	Low Cost	Expensive	Additional Cost	Additional Cost
Solderability	Excellent	Good	Excellent	Excellent	Excellent

Figure 14-Surfaces Finish Characteristic

2.6 測試方法指導原則設計 Design For Test Access Guideline

2.6.1 簡介 Introduction

內部電路測試（ICT）爲製造工藝品質提供頗有價值的分析，就是開路與短路，糾正元件值，元件組裝價值和一些基本邏輯功能的狀況。爲了獲得 ICT 的最大益處，必須達到最高可能的測試覆蓋。必須要分析與修改功能性原理圖以提高對時鐘、三態元件及其它功能性邏輯元件的控制。另外，倘若擴大邏輯功能的覆蓋，測試點有需要增加對信號輸入的測試。此分析優先於所送至編排的原理圖的改進並被作爲是電子測試評估。

In – Circuit testing (ICT) provides valuable information on the quality of the manufacturing process, namely, open and shorts, correct device values, worthiness of components assembled and in some cases, the basic functioning of logic. To get the maximum benefit of ICT the highest possible test coverage must be achieved. The functional schematic must be analyzed and modified to provide control over clocks, tri-state devices,and other functional logic elements. In addition, test points may need to be added to allow for signal injection providing expand coverage of the logic functions. This analyzing is prior to the schematic development being sent to layout and is known as the electrical test review.

2.6.2 測試方法設計 Design for Test Access

• 板的每個網上都應有一個測試點，包括不使用的與沒連接的信號。

There should be a test point on every net on the board including unused and no-connect signals.

• 測試點應置於板底部。可以使用頂部測試點，但只有在底部的通道面積用完的時候才可以。

Test points should be placed on the bottom side of the board. Topside test points may be used but only after the bottom side access area is exhausted.

• 測試點尺寸如下表。如果空餘面許可，則儘量用最大的測試點。如使用的測試點小於 0.030[0.75]，將會對測試量與良率產生影響。

Test point sizes are shown in the chart below. If space permits, the largest test point size possible should be used. There will be test yield and throughput impacts with use of test points smaller than 0.030[0.75].

Board Diagonal	Testpoint Pad size	Pad Shape
12.00 [304.80] or greater	0.035 [0.90] to 0.040 [1.00] preferred	Square or Round
12.00 to 8.00 [304.80 to 203.20]	0.035[0.90] to 0.040 1.00] preferred 0.030 [0.75] to 0.032 [0.80] acceptable	Square or Round
8.00 [203.20] or less	0.025 [0.64] absolute minimum	Square or Round

• 測試點與測試點的間距應爲 0.100[2.50]。沒有達到的地方，0.070[1.75]的間距是可以接受的(0.050[1.25]的交錯)。依然達不到的，可以接受 0.050[1.25]的間隔。0.050[1.25]的間隔雖可接受，但會增加固定設備成本並會減少測試可靠性。

Test point to test point spacing should be 0.100[2.50]. Where not achievable, 0.070[1.75] spacing is acceptable (0.050[1.25] staggered). Where still not achievable, 0.050[1.25] spacing is acceptable. 0.050[1.25] spacing, although acceptable, may increase fixture cost and reduce test reliability.

• 由於不斷集中化的 net 與相關連的插腳間距的高度密集化， BGA 爲測試每個 net 提出了巨大的挑戰。爲提供足夠的測試方法，在決定正確的選擇時，板的密度扮演了重要的角色。在 BGA 上面或下面，使用下面的指導原則決定最優先與最不優先的測試方法。

BGAs provide the greatest challenge for testing every net because of the high density of converging nets and associated pin pitches. The board density plays a large part in determining the proper options to choose for providing adequate test access. Use the following guideline to determine the most preferred to the least preferred test access under or surrounding BGAs:

* 將所有的輸出電極測試點遠離 BGA 與 CSP 輪廓線，最大可接受的間距(0.100[2.50]/0.070[1.75]/0.050[1.25])。

Fan out all test points away from the BGA and CSP outlines on the largest acceptable pitch (0.100[2.50]/0.070[1.75]/0.050[1.25]) as possible.

* 0.070[1.75]中心具有接收不可用與沒連接信號的最小優先權的插

腳，在此分離通道上的交叉測試點。

Stagger test points on the breakout vias for pins on 0.070[1.75] centers with “unused” and “no- connect” signals receiving the least priotity.

＊ 定位測試點在 0.050[1.25]中心最小處。每平英尺的測試點密度不應該超過 40 個。如果增加另外的板層，要求提供測試方法，不可用的與沒連接的信號將收到最少的優先權，也可以放棄。

Location test points on acenter minimum. Probe density should not exceed 40 test points per square inch. 時 “Unused” and “no-connect” signals are to receive the least priority and may be left off if adding additional board layers would be required to provide test access.

• 在測試點作業中使用下面的優先順序-- Use the following priority in test point assignment –

震盪器與時鐘打澆口	Oscillator and clock degating.
設備癱瘓與三態	Device disabling and tri-stating.
邊界流覽 TAP	Boundary scan TAPs.
可編程零件通道	Access to Programmable Parts

• 不可直接連接信號到地或電壓 。在每個 net 上使用一個拉閘式電阻。

Do not tie signals directly to ground or voltage. Use a pull up or pull down resistor on each net .

2.6.3 測試墊片位置公差 Test Pad Location Tolerances

• 對小於 0.015[1.27] 高度的元件，其測試點區域間距到 SMT 測試區域邊緣的最小間距 0.010[0.25]，並遠離測試墊片邊緣（短邊）。測試點墊片邊緣到元件體（長邊）間距應該是 0.015[0.38]（備註：該測量是從墊片或元件邊緣（任一可用的都可）到測試墊片邊緣或中心）。

For devices less than 0.015[1.27] high the testpoint land spacing to SMT land edge should be 0.010[0.25] minimum away from the (short side) test pad edge. The testpoint pad edge to component body (long side) spacing should be 0.015[0.38]. (Note : This measurement is from the pad or device edge, whichever is applicable , to the edge of the testpad , not the center).

• 如果元件的高度在 0.050[1.27] 和 0.250[6.35]，測試墊片邊緣到元件邊緣應是

0.00[2.54]的最小距離。

If the component height is between 0.050[1.27] and 0.250[6.35],the test pad edge to component edge should be a minimum of 0.00[2.54].

• 除了 ENTEK 要求在通由面 1 間距爲 0.200[5.00]，在通由面 2 間距爲 0.150[3.80] ，測試墊片邊緣到板邊緣的最小距離應爲 0.125 [3.20]。

Test pad edge to board edge minimum distance should be 0.125[3.20]; except on ENTEK which requires 0.200[5.00] distance on the pass 1 side and 0.150[3.80] distance on the pass 2 side.

• 測試墊片邊緣到通孔最小距離應爲 0.125[3.20]同時到 ICT 定位插腳 0.250 [6.35]。

Test pad edge to tooling hole minimum distance should be 0.125[3.20] and 0.250[6.35] distance from the ICT location pin.

• 在一個波峰焊接區域，測試電極到通孔墊片間要求一個最小 0.075[1.90]間距以防止短路。

Test pads to through hole pads in a wave solder zone requires a minimum distance of 0.075[1.90] to prevent solder bridging .

備註：增補的細節化 ICT 和功能測試資訊見“可測試性指導原則”Solectron 檔編號 TST-10[008175。

NOTE: For Supplemental detailed ICT and functional testing information see “Testability Design Guidelines” Solectron document number TST-10-008175.

3.0 配圈排列方式和元件間距的指導原則

Land Pattern and Component Spacing Guideline

3.1. Pin 插孔元件 PinThough Hole Component

3.1.1 簡介 Introduction

爲孔排列方式和間距而做的規則反映了在裝配期間自動化插入元件的應用和配合整個自動化進程的檢測和反修工具與技術。

The rules for hole pattern and hole spacing reflect the use of automated insertion equipment during assembly, and the tools and techniques of inspection and repair that accompany a fully automated process.

由於電子工業和電路封裝技術的提高而更趨向於 SMT 的更高領域，自動化插入進程 PTH 元件的應用正在逐漸降低。結果在裝配中 SMT 相關的制程不斷增加的數目集中了手工放置和 PTH 零件插入兩個方面。因爲手動規則比自動化插入規則限制較少，考慮間距方面限制少。換句話說，元件在用機器放置比人工放置的之間間距最小極限要大。

The use of automated insertion processes PTH components is decreasing as the electronics industry and circuit packaging technologies gravitate more toward SMT which has higher yields. As a result a growing number of SMT-oriented processes are integrated with manual placement and insertion of PTH parts in the assembly. Because the manual rules are less limiting than automated insertion rules, spacing considerations can be less restrictive. In other words, when components are manually placed rather than machine place, the minimum space between can be closer.

在這段中出現的指導原則運用於自動化插入進程。如果有嚴格的設計要求，強調更緊密的間距和手工放置，設計者應該徵求 DFM 工程師有關實際間距的極限值問題。這些原則是從 PTH 生產原則中選取的，要想看更完整的資料，就要看 IPC-SM-780。

The guidelines presented in this chapter apply to an automated insertion processes. If more severe design requirement dictate closer spacing and manual placement, designers should consult the DFM engineer about practical spacing limitations. These guidelines are selected excerpts from the full range of PTH manufacturing guidelines. For complete guidelines, see IPC Pin Through Hole reference IPC-SM-780

3.1.2 孔的排列方式 Hole Patterns

PTH 部分的孔排列方式能適應圓形，正方形或者四邊形電子元件或連接器的 PIN 。連接長度與波焊的參數和孔直徑或最大間距的形式和大小這些都作爲重要的設計考慮問題。

Hole patterns for PTH parts can accommodate round, square or rectangular pins from electronic components and connectors. The parameters of clinching length vs. wave solder, and hole diameter or lead type and size are important design considerations.

元件孔的直徑應該在 0.004 中間選擇。當元件最大間距在 0.032(0.80)或更大的時候，孔直徑與最大直徑或元件最大間距的 pitch 偏差應該在 0.016(0.40)-0.020(0.50)。如果元件比最大間距 0.032(0.80)小，元件孔應設計比 0.012(0.30)-0.016(0.40)大。

The diameters of the component holes should be selected at even 0.004(0.01) intervals. The difference between the hole diameter and the maximum diameter or diagonal of the components lead shall be 0.016(0.40)-0.020(0.50) when the components leads are 0.032(0.80)or larger. If the components leads are smaller than 0.032(0.80), the component hole must be designed 0.012(0.30)-0.016(0.40)larger.

對於電鍍通孔，有專門的規則用來定位離元件多遠，在下面通孔元件的間距中有一部分作爲它的解釋。

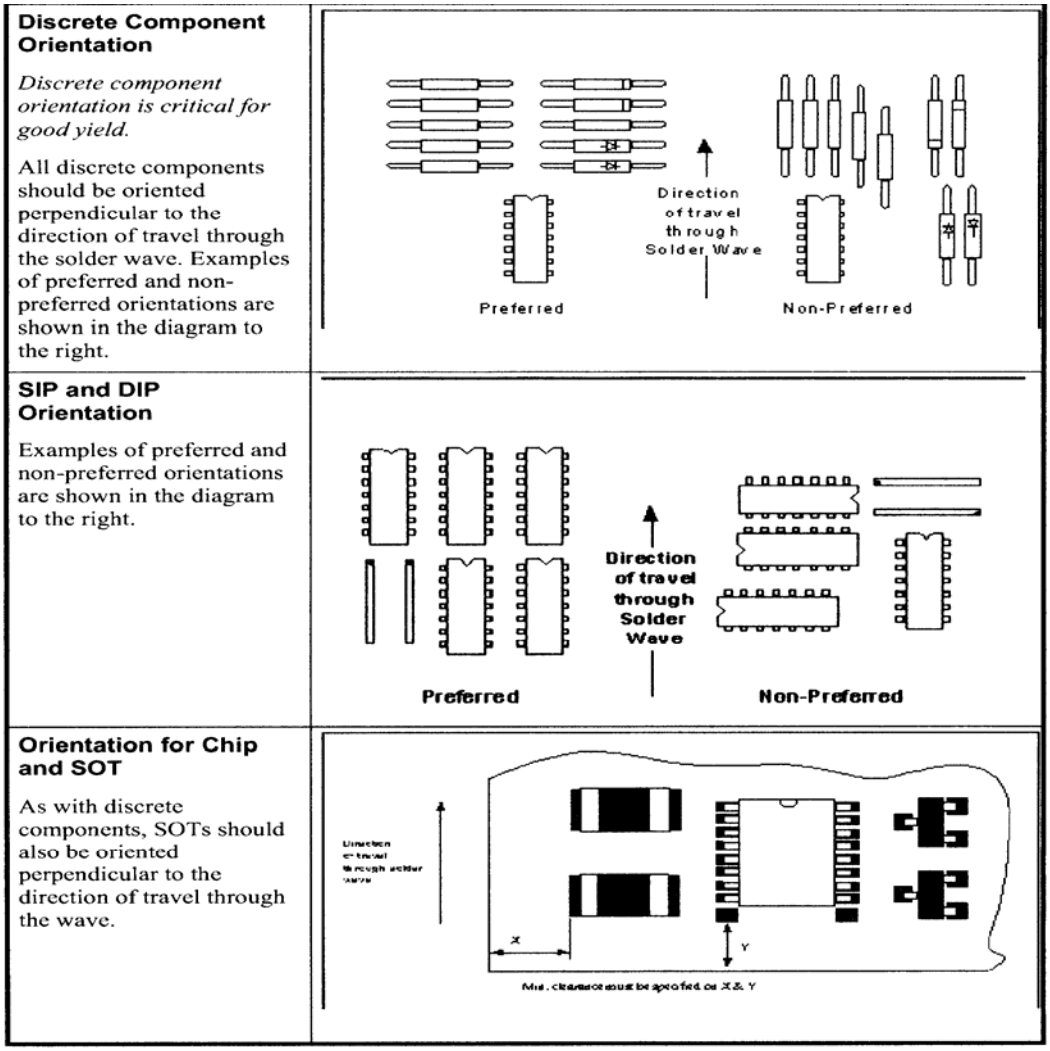
For plated-through holes, special rules apply for positioning them near components. These are explained below in the section Spacing of Through Hole Components.

電鍍通孔應該從 0.008(0.20),0.012(0.30),0.020(0.50),0.024(0.60),0.031(0.80) and 0.040(1.00)系列直徑中選取。（如果用 HASL 作爲表面處理，最小孔直徑是 0.012(0.30)）。選取儘量大的孔直徑，從生產角度來說，當電鍍通孔在單面上直徑是變化的，如果僅一個最小直徑孔能適應到所有，這板是較強的。

Plated-through holes, should be selected from the diameter series 0.008(0.20),0.012(0.30),0.020(0.50),0.024(0.60),0.031(0.80) and 0.040(1.00). (If using HASL as surface treatment, the minimum hole diameter is 0.012(0.30).) Choose as large a diameter as possible. From the manufacturing perspective, when the plated-through holes are in a variety of diameters on a single board, the board is stronger than if only the smallest diameter hole was used for all.

3.1.3 PTH 定位的通用指導原則

General Guidelines for PTH Orientation



3.1.4 通孔元件的間距 Spacing of Through Hole Components

設計成自動插入零件時，下表列出了推薦元件間距。

The table below shows recommended component spacing when designing automated insertion equipment.

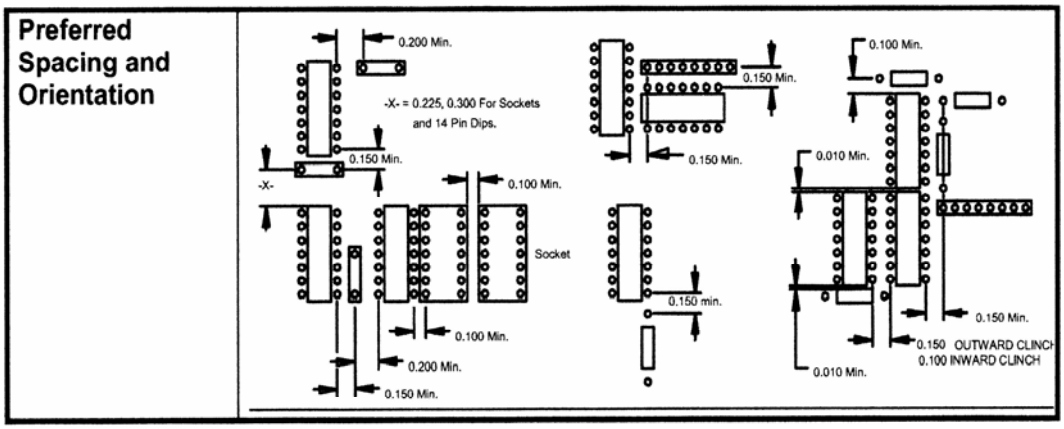
Description	Spacing-inches
IC side pin to side pin centers	0.100[2.54]min.0.150[3.81] preferred
IC top to bottom (last pin to pin)	0.200[5.08]min.if no cap 0.300[7.62]with cap
IC to parallel axial component	0.150[3.81] body to IC pin
IC pin to axial component pin in line	0.200[5.08] pin to pin
IC body to axial component perpendicular	0.010[0.25] body to body clearance min
Axial component to axial component	(body 1 dia.+body 2 dia.)/2+0.010[0.25]min.
PGA Body other device Body or Pad	0.150[3.81]typical,0.125[3.18]min

注 1：當放置通孔元件，重要的是考慮自動裝配產量同時還有檢測和返修的問題。

Note 1:when placing through-hole components, it is important to consider the outcome on automated assembly as well as inspection and repair task .

注 2：如果不是自動插入，間距能縮減到 0.100(2.54)。

Note 2: If not automatically inserted, spacing can be to a 0.100(2.54) grid .



A. Via to Pi Spacing

Feed through locations:

No exposed c is allowed wi 0.080 [2.00] terminal pad.

Avoid feed th in the inward outward clinc zones of axia radial and dip components.

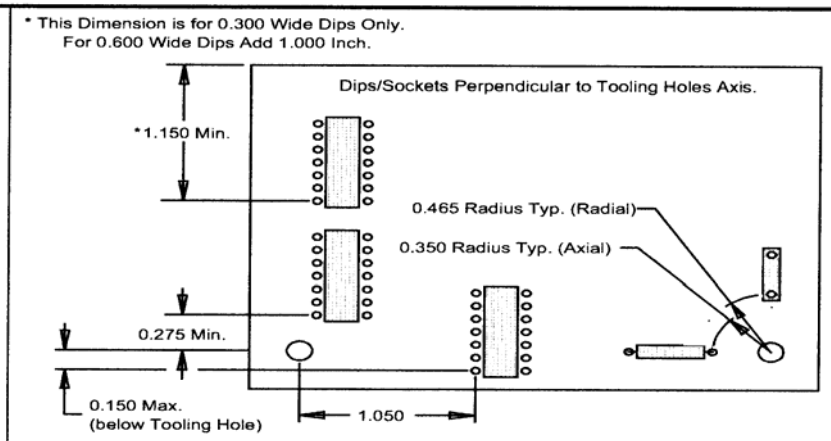
Axial and R spacing

Minimum axi lead compone spacing is equ the sum of th component b diameters div by 2 plus 0.0 [0.38].

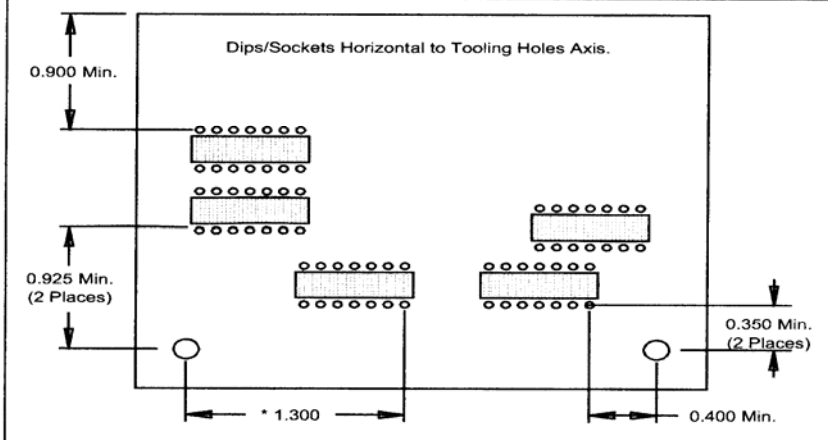
Minimum spa is 0.100 [2.54

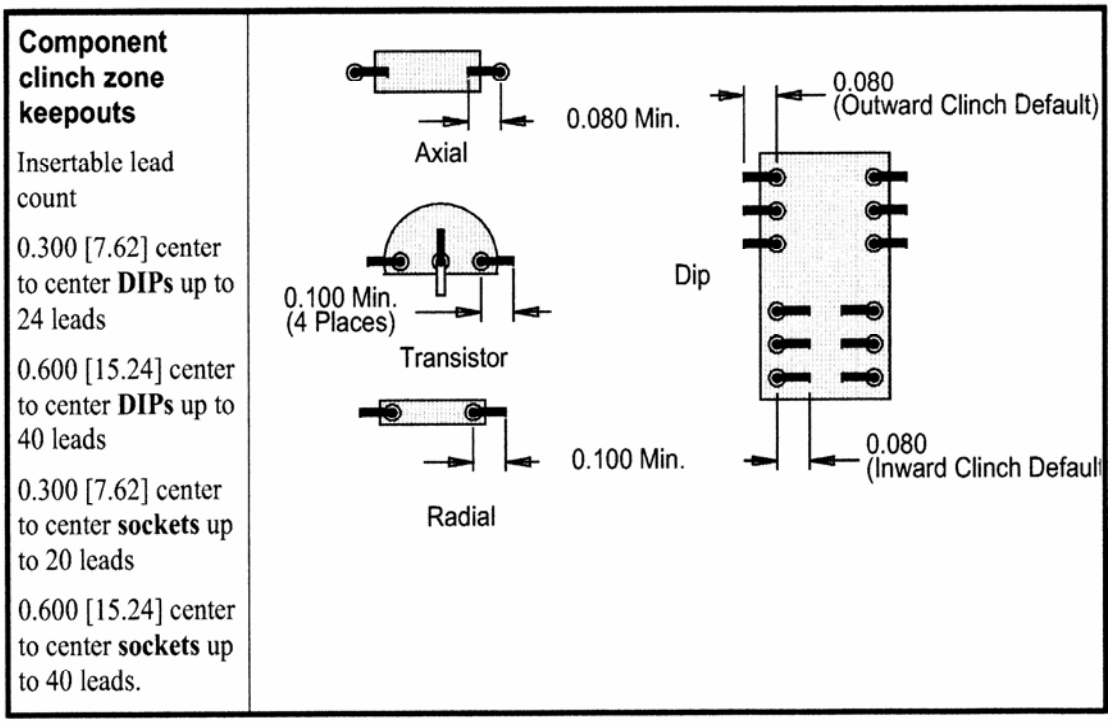
Component to tooling hole and card edge Perpendicular orientation

Spacing requirements for dip and axial insertion with tooling hole clearances.



Component to tooling hole and card edge Horizontal orientation





3.2 表面貼裝元件 Surface Mount Component

3.2.1 簡介 Introduction

Soletron 表面貼裝技術指導原則目的是減少制程中的缺陷，確保長期焊接頭的可靠性和適應於自動化裝配方式，測試，產品返修。這些指導原則建立在標準的積累和 OEM 的發展基礎上的，現在所表達的指導原則的是一些在 PCS 裝配中的設計和生產的 Soletron 知識延伸和經驗的累積。

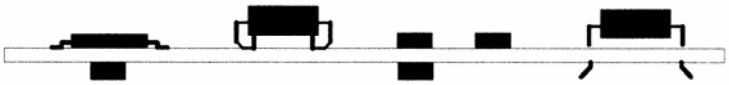
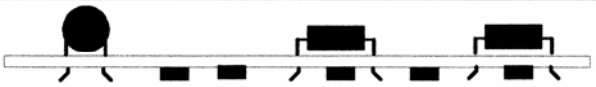
Soletron's surface mount technology guidelines aim to minimize in-process defects, ensure long term solder joint reliability and accommodate the automated assembly, test, and rework of the product. These guidelines. founded from a comprehensive accumulation of standards and OEM development, currently represent a comprehensive accumulation of Solectron's extensive knowledge and experience in the design and manufacture of PCS assemblies.

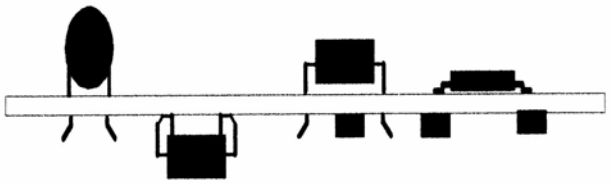
確保重複生產工藝和高質量的產品，經濟的設計是建立在一些世界範圍的加工基地基礎上的。Soletron's 目標集合這些元件的排列方式和間距導入到 PBC 設計中。這些指導原則是衡量用在 DFM 中分析和溶入針對製作、裝配、測試的自動化 FDM 工

具。

To ensure repeatable manufacturing processes and high-quality, cost-effective designs that can be built in any of our worldwide manufacturing sites, it is Solectron's goal to incorporate these component patterns and spacing guide into all PCB designs. The guidelines are the measures used in a DFM analysis, and are integrated into our automated FDM tools for fabrication, assembly and test.

3.2.2 表面貼裝類型 Type of Surface Mount Assemblies

Type I **All SMT** • Surface Mount Components (SMCs) only • Single or double sided attachment	 • **Reflow solder process**
Type II **Mixed Technology** • Pin Through Hole components on top side • SMCs on top side • May have SMCs on bottom	 • **Dual Soldering Process** Reflow solder for top side SMCs Standard wave solder process for PTH components only Dual wave solder process with SMCs on bottom side Special soldering techniques may be required: hand soldering, focused IR, hot gas, solder fountain, etc.
Type III **Mixed Components** • PTH components on top side • SMCs (Passives) on bottom Side	 • **Single Soldering Process** Dual wave soldering required

Type IV **Mixed Components** • PTH and SMCs (Actives and Passives) on top side • SMCs (Actives and Passives) on the bottom side	 • **Selective Soldering Process** Top side and bottom side reflow Bottom side wave PTH only using custom tooling; selective wave solder pallet

3.2.3 類型 IV：混合雙重迴流焊（下麵元件重量限制）

Type IV Mixed with Dual Reflow (Bottom Side Component Weight Limit)

在板底下元件在迴流焊期間重要的是放置元件不要掉下來。元件重量與錫焊區有關，這將決定是否有足夠的表面強度和重力來支持板上的元件。如果元件確定不是雙面回流焊，元件放置的那一邊將最後被迴流焊（典型處在上面）。

It is important not to place components on the bottom side of the board that will fall off during the second reflow cycle. The weight of the component in relation to its solderable area will determine whether there is enough surface tension vs. gravity to hold the component to the board. If a component is determined not to be double sided reflow， compatible place the component on the side of the board which will be reflowed last (typically to side).

注：所有應用的 SMT 配圈排列應該在 Soletron's 配圈排列內的 10%，推薦值可查閱 3.4 和 3.5。

NOTE: All SMT land patterns used should be within 10% of Soletron's land pattern recommendations found in sections 3.4 and 3.5.

元件間距排列需要對稱例如：PLCC，QFP，SOJ，SOIC，等等。非對稱排列在雙面焊時有脫落的危險，是由於表面錫焊強度不平衡。

Component lead patterns need to be symmetrical (e. g PLCC, QFP, SOJ, SOIC, etc) There is a risk of non-symmetrical parts peeling off during double sided reflow, due to "surface solder tension" imbalance.

確定是否固定元件在迴流焊過程中有能力保持不脫落，用下面的方程式：(注：一種超級計算器通過連接新產品工程在自動計算方程式方面是很有效的）

To determine if the device has the ability to stay attached during the double reflow soldering process use the following formula:(Note: an excel generator is available for calculating the formula automatically by contacting Solectron "New Products Engineering").

注：計算方程式中間距的長和寬是計算實際的錫焊面積大小，關於 BGA 計算是用近似球直徑。

WEIGHT OF COMPONENT (GRAMS) TOTAL LEAD SOLDERABLE AREA(mm^2)	Grams/mm^2

PBGA&CBGA Weight to Lead Area Ratio (Maximum Grams/mm^2)	≤0.050
PLCC&SOJ Weight to Lead Area Ration (Maximum Grams/mm^2)	≤0.350
SOIJ,SSOP,TSOP&TSSOP Weight to Lead Area Ration (Maximum Grams/mm^2)	≤0.300
QFP Weight to Lead Area Ration (Maximum Grams/mm^2)	≤0.500

NOTE: Lead length and width used in the formula is measured for both gull wing and J-Leaded as the actual soldered contact area of the lead onto the pad. The BGA measurement uses the nominal ball diameter.

3.3 選擇性錫焊工藝 Selective Soldering Process with use of pallets

3.3.1 簡介 Introduction

這種工藝要求運用回流焊接設備到帶有焊尾的元件，但是隨著在底部裝上 pallet，就可在這區域表面貼裝元件。固定點錫焊設備在一些工廠是普遍使用的，這個設備可用來每次焊一個角，這樣的設備減少了元件間的距離要求（通過聯繫部門生產工程師以瞭解確切的尺寸大小）。通過用表面貼裝或混合 pin，插孔焊接頭的數目應該減小到最小值。

This process requires the use of reflow soldering equipment for components with solder tails but with the use of pallets on the bottom side which shields surface mount components. Localized point soldering machines are available at some sites which may be used to solder one pin at a time. Such machines reduce the spacing required between device lands(contact your local manufacturing engineer for the exact dimension). The number of through hole solder joints should be kept to a minimum, by the use of surface mount packages or compliant pins.

3.3.2 選擇性錫焊指導原則 Selective soldering guidelines

在 PC 板的底面 SMD 元件的高度應該保持一個最小值，以避免帶有 pallet 的行腔高度的限制。推薦最大元件高度是 0.150(3.80) ，0.120(3.00) 值爲優先考慮。

Height of SMD components on the PCB bottom side should be kept to a minimum to avoid cavity depth issues with the pallet. Recommended maximum component height is 0.150(3.80), with 0.120(3.00) preferred.

插孔 pin 伸出範圍在 0.030(0.75) 和 0.080(2.00)之間，才能獲得良好的波焊接頭形

狀。一些 pin 在範圍值之外，就必須同生產工程部門聯繫以取得他們的同意。

Through hole pin protrusion range must be between 0.030(0.75) and 0.080(2.00) for a proper wave soldering joint. Any pins outside of this range must be agreed to by manufacturing engineering.

在通孔配圈邊和 SMD 配圈邊之間有間距的要求時，查看間距表格 3.6.5,3.6.6 和 3.6.7 。See spacing table 3.6.5,3.6.6 and 3.6.7 for the spacing required between the through hole land edge and the SMD land edge (when providing clearance for pallet use).

3.3.3. Thieving Pad 要求波焊多行間距大的元件

Thieving Pad Required for Wave Soldering Multi-leaded Devices

例如像接頭和插頭這些元件要有 Solder thieving 就要求用波焊多行間距大的通孔元件，如果地方允許，把元件旋轉到與波焊方向一致。

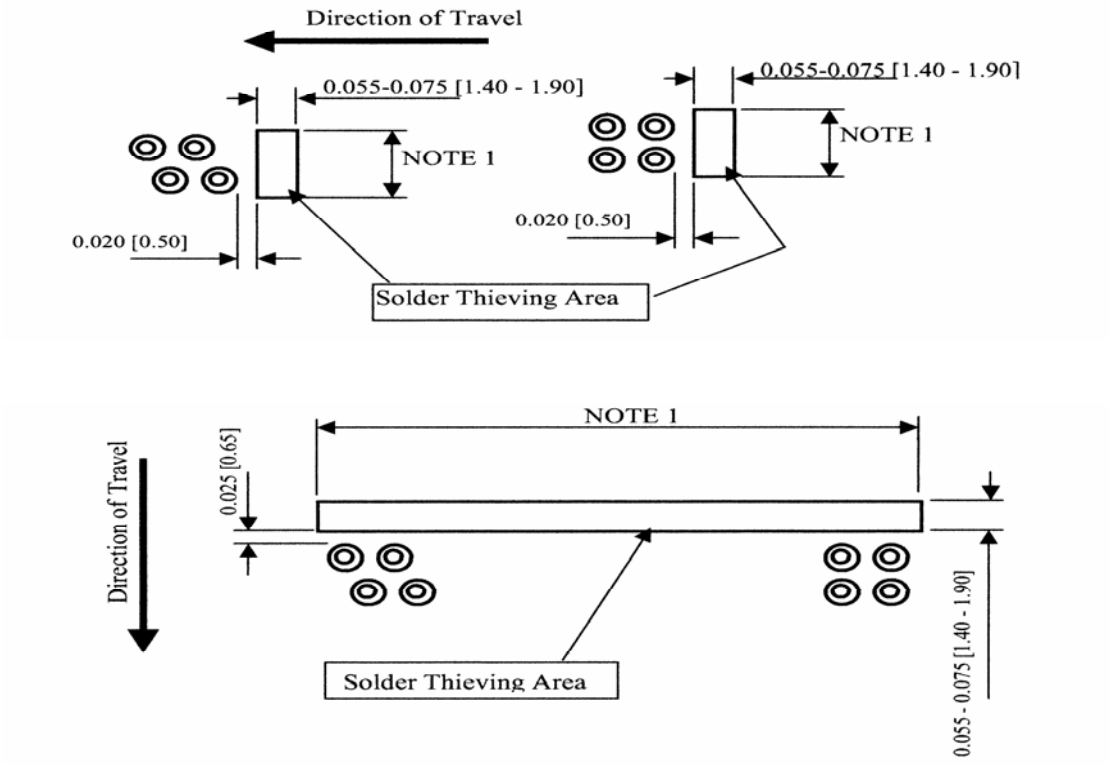
Solder thieving is required for wave soldering multi-leaded through hole devices such as connectors and plugs. Where possible, rotate the device with the longest dimension in line with the wave direction.

Thieving 可能由相同尺寸和間距的襯墊組成，下圖所示出了元件的 PIN 或每個銅 Thieving 區的要求，銅 Thieving PIN 就不會有 solder mask，用下圖能幫助定義是否在特殊元件上要求 Thieving。

Thieving may be made up of pads of the same size and spacing as the pins of the devices or per a copper thieving area shown in the chart below. The copper thieving areas are to be free of soldermask. Use the chart below to help determine if thieving is required for a particular device.

Pin Pitch	Stick-Thru	Solder Thieving Area
0.100[2.54]	Up to 0.080[2.03]	Not Required
0.100[2.54] intersatitial	Up to 0.050[1.27]	Not Required
0.100[2.54] intersatitial	0.051[1.30] to 0.080[2.03]	Required
0.025[0.64] or 0.050[1.27]	Up to 0.020[0.51]	Not Required
0.025[0.64] or 0.050[1.27]	0.021[.53] to 0.080[2.03]	Required

NOTE 1 - Adjust width to be beyond the device hole and pad pattern.



3.4 SMT 配圈排列方式　　SMT Land Patterns

配圈排列方式包括了所有的普通 SMT 元件封裝和 BGA、CSP 封裝。 配圈排列尺寸由墊片的長和寬，墊片間距和頭對頭的間距給定的。預計的跟和頭的相切值是在假設元件大小基礎上的，這些數值作爲焊接頭質量的參考。

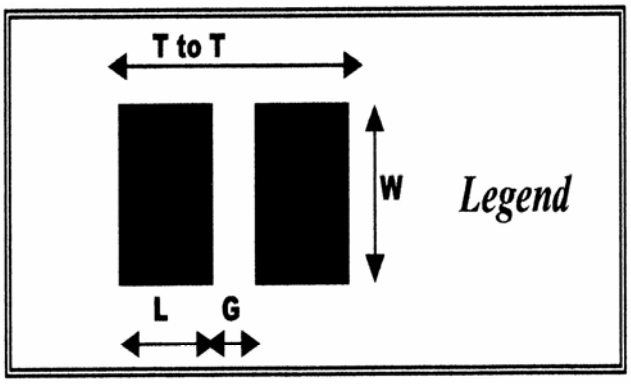
The land patterns cover all generic SMT component packages and include BGA and CSP component package. The land pattern dimensions are given for pad length and width, pad gap, and the resulting toe-to-toe spacing. The expected heel and toe fillet based on nominal component dimensions is provided as a reference to the quality of the solder joint.

3.4.1 被動晶片 Passive Chips

3.4.1. Passive Chips

Chips (Reflow)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
0201 [0603]	12 [0.32]	15 [0.38]	9 [0.24]	39 [1.0]	7.5 [0.2]	3.5 [0.09]	No traces, planes, solder mask or marking permitted in the gap. Wide trace connections need to be placed on both ends or sides of the pad
0402 [1005]	20 [0.50]	21 [0.53]	12 [0.30]	54 [1.36]	6.5 [0.16]	5 [0.13]	No traces, planes, solder mask or marking permitted in the gap. Wide trace connections need to be placed on both ends or sides of the pad.
0603 [1608]	30 [0.75]	30 [0.75]	28 [0.70]	88 [2.20]	12.5 [0.30]	3.5 [0.09]	Avoid traces, planes or marking in the gap. Wide trace connections need to be placed on both ends or sides of the pad.
0805 [2012]	50 [1.25]	45 [1.15]	30 [0.75]	120 [3.05]	20.5 [0.52]	3.5 [0.09]	
1206 [3216]	60 [1.50]	50 [1.25]	70 [1.75]	170 [4.25]	22 [0.52]	3 [0.09]	
1210 [3225]	100 [2.50]	55 [1.40]	70 [1.75]	180 [4.55]	27 [0.67]	3 [0.09]	
1808 [4520]	80 [2.00]	55 [1.40]	120 [3.10]	230 [5.90]	26.5 [0.70]	5 [0.13]	
1812 [4532]	125 [3.20]	65 [1.65]	105 [2.60]	235 [5.90]	29 [0.74]	4 [0.14]	
1825 [4564]	250 [6.35]	70 [1.75]	105 [2.60]	245 [6.10]	34 [0.80]	4 [0.14]	
2010 [5025]	100 [2.50]	60 [1.50]	130 [3.30]	250 [6.30]	26.5 [0.65]	4.5 [0.12]	
2225 [5564]	250 [6.35]	70 [1.75]	140 [3.55]	280 [7.05]	30 [0.73]	5 [0.13]	
2512 [6332]	125 [3.20]	65 [1.65]	180 [4.55]	310 [7.85]	31 [0.78]	5 [0.14]	

Chips (Wave Solder)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
0603 [1608]	30 [0.75]	40 [1.00]	30 [0.75]	110 [2.75]	23.5 [0.57]	2.5 [0.07]	Not recommended
0805 [2012]	50 [1.25]	50 [1.25]	35 [0.90]	135 [3.40]	28 [0.70]	1 [0.02]	
1206 [3216]	60 [1.50]	60 [1.50]	70 [1.75]	190 [4.75]	32 [0.77]	3 [0.09]	
1210 [3225]	100 [2.50]	65 [1.65]	70 [1.75]	200 [5.05]	37 [0.92]	3 [0.09]	
1808 [4520]	80 [2.00]	65 [1.65]	120 [3.10]	250 [6.40]	35 [0.95]	5 [0.13]	
1812 [4532]	125 [3.20]	75 [1.90]	105 [2.65]	255 [6.45]	39 [0.98]	4 [0.11]	
2010 [5025]	100 [2.50]	70 [1.75]	130 [3.30]	270 [6.80]	36.5 [0.90]	4.5 [0.12]	
2512 [6332]	125 [3.20]	75 [1.90]	180 [4.60]	330 [8.40]	41 [1.05]	5 [0.11]	



3.4.2 低感應係數被動晶片　　Low Inductance Passive Chips

Low Inductance Chips (Reflow)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
0306 [0816]	60 [1.50]	14 [0.35]	14 [0.35]	42 [1.05]	5 [0.12]	2.5 [0.06]	No traces, planes or marking permitted in the gap. Wide trace connections need to be placed on both ends or sides of the pad.
0508 [1220]	80 [2.00]	25 [0.65]	20 [0.50]	70 [1.80]	10 [0.26]	2.5 [0.06]	No traces, planes or marking permitted in the gap. Wide trace connections need to be placed on both ends or sides of the pad.
0612 [1632]	125 [3.20]	30 [0.75]	30 [0.75]	90 [2.25]	13 [0.32]	5 [0.12]	No traces, planes or marking permitted in the gap. Wide trace connections need to be placed on both ends or sides of the pad.

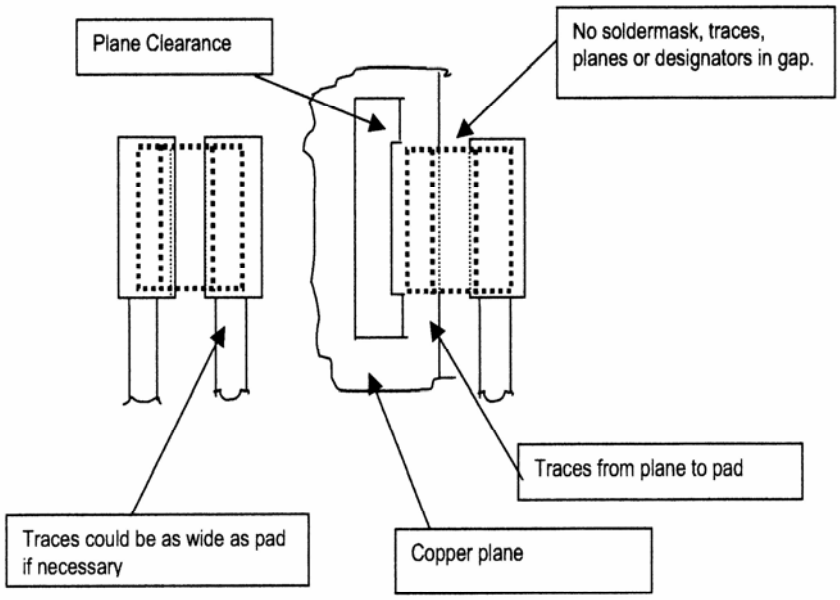
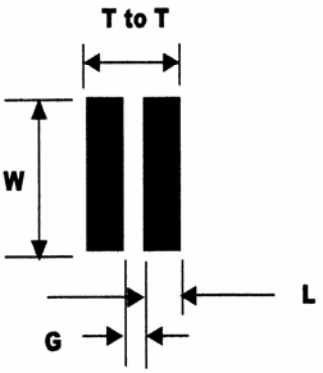


Figure 15- Legend for Low Inductive Passive Chips



3.4.3 鉭質電容　　Tantalum Capacitors

注意這有一些新尺寸電容與舊尺寸鉭質電容搭配使用，表中已列舉。不斷變化的供

應值與 a 指定者在封裝尺寸方面產生衝突,設計者必須仔細注意哪種墊片尺寸要用。

Please note that there are new sizes of tantalum capacitors that overlap with old sizes. As shown in the table, various suppliers are using conflicting alpha designators for package size. Designers must carefully note the component size to know which pad design to use.

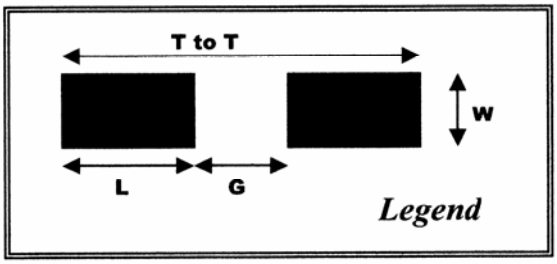
Tantalum Capacitors (Reflow)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
1206 [3216] A, A2, Y-size	50 [1.25]	60 [1.50]	40 [1.00]	160 [4.00]	17 [0.40]	12 [0.31]	
1311 [3528] B, B2, X-size	90 [2.25]	60 [1.50]	50 [1.25]	170 [4.25]	16 [0.37]	13 [0.34]	
1810 [4726] B-size	56 [1.40]	60 [1.50]	96 [2.45]	216 [5.45]	15.5 [0.38]	13 [0.35]	
2218 [5846] D, D2, V-size	100 [2.50]	84 [2.15]	100 [2.50]	286 [6.80]	20 [0.50]	13 [0.35]	
2312 [6032] C-size	90 [2.25]	84 [2.15]	110 [2.75]	278 [7.05]	21 [0.53]	13 [0.35]	
2816 [7343] D, E, N-size	100 [2.50]	84 [2.15]	160 [4.00]	328 [8.30]	21 [0.51]	14 [0.39]	
Tantalums (Wave)							
1206 [3216] A, A2, Y-size	50 [1.25]	90 [2.25]	40 [1.00]	220 [5.50]	47 [1.19]	12 [0.31]	Not recommended
1311 [3528] B, B2, X-size	90 [2.25]	100 [2.50]	50 [1.25]	250 [6.25]	56 [1.42]	13 [0.34]	Not recommended
1810 [4726] B-size	56 [1.40]	90 [2.25]	96 [2.45]	276 [6.95]	45.5 [1.15]	13 [0.35]	Not recommended
2218 [5846] D, D2, V-size	100 [2.50]	140 [3.50]	100 [2.50]	380 [9.50]	76 [1.86]	13 [0.35]	Not recommended
2312 [6032] C-size	90 [2.25]	140 [3.50]	110 [2.75]	390 [9.75]	77 [1.96]	13 [0.35]	Not recommended
2816 [7343] D, E, N-size	100 [2.50]	150 [3.75]	160 [4.00]	460 [11.50]	86.5 [2.20]	14 [0.39]	Not recommended

當以內迴圈電路測試爲目的要求劈開墊片，除了 0.008[0.20]（不適合波焊）這個尺寸從中心劈開兩部分之外，所有留下的尺寸都是相同的。

* When split pads are required for in-circuit-testing purposes all footprint dimensions are the same except for an 0.008[0.20]split opening down the center of pad width(w) for both pads.(not applicable for wave solder)

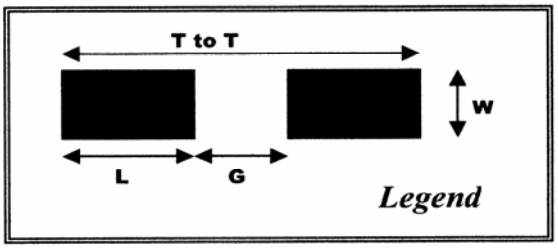
3.4.4 鋁質電解質電容　　Aluminum Electrolytic Capacitors

Alum. Electrolytic Capacitors	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils	mils	mils	mils	mils	mils	
	[mm]	[mm]	[mm]	[mm]	[mm]	[mm]	
4 mm diameter	35	105	30	240	29.5	4.5	
	[0.90]	[2.65]	[0.75]	[6.05]	[0.73]	[0.12]	
5 mm diameter	35	125	40	290	29	9.5	
	[0.90]	[3.20]	[1.00]	[7.40]	[0.75]	[0.25]	
6.3 mm diameter	35	145	50	340	32	10.5	
	[0.90]	[3.70]	[1.25]	[8.65]	[0.82]	[0.28]	
8/9 mm diameter	35	175	100	450	30	11	
	[0.90]	[4.45]	[2.50]	[11.40]	[0.75]	[0.30]	
10 mm diameter	35	175	160	510	26.5	10.5	
	[0.90]	[4.45]	[4.00]	[12.90]	[0.65]	[0.30]	
16 mm diameter	47	262	2.36	760	31	14	
	[1.20]	[6.65]	[6.00]	[19.30]	[0.80]	[0.35]	



3.4.5 MELFs

Alum. Electrolytic Capacitors	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
4 mm diameter	35 [0.90]	105 [2.65]	30 [0.75]	240 [6.05]	29.5 [0.73]	4.5 [0.12]	
5 mm diameter	35 [0.90]	125 [3.20]	40 [1.00]	290 [7.40]	29 [0.75]	9.5 [0.25]	
6.3 mm diameter	35 [0.90]	145 [3.70]	50 [1.25]	340 [8.65]	32 [0.82]	10.5 [0.28]	
8/9 mm diameter	35 [0.90]	175 [4.45]	100 [2.50]	450 [11.40]	30 [0.75]	11 [0.30]	
10 mm diameter	35 [0.90]	175 [4.45]	160 [4.00]	510 [12.90]	26.5 [0.65]	10.5 [0.30]	
16 mm diameter	47 [1.20]	262 [6.65]	2.36 [6.00]	760 [19.30]	31 [0.80]	14 [0.35]	

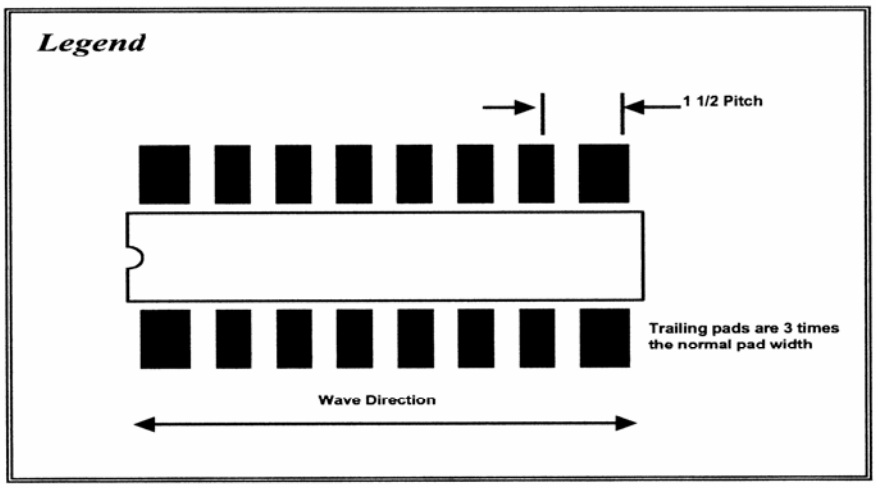


這些指導原則是假設一個四邊形排布。這個假設有利於在洄流焊期間方便確定元件中心。

These guidelines assume a rectangular pattern. The suggested cutout pad depicted above facilitates component centering during reflow.

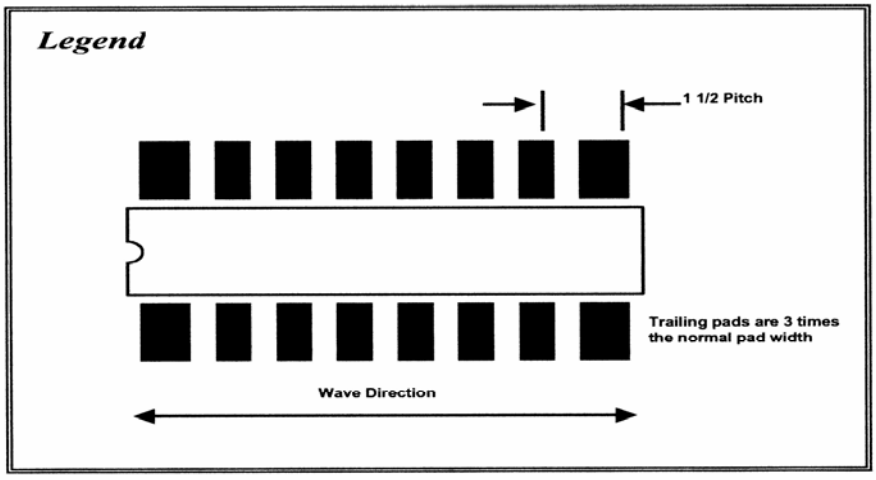
3.4.6 SOICs (reflow)

SOICs (Wave)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
SOIC-#D	24* [0.60]	70 [1.75]	150 [3.80]	290 [7.30]	27 [0.65]	2 [0.06]	* - last pad is 72; R-Packs not recommended
SOIC-#DW	24* [0.60]	70 [1.75]	320 [8.10]	460 [11.60]	27 [0.65]	0.5 [0.03]	* - last pad is 72;



3.4.7 SOIC(Wave)

SOICs (Wave)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
SOIC-#D	24* [0.60]	70 [1.75]	150 [3.80]	290 [7.30]	27 [0.65]	2 [0.06]	* - last pad is 72; R-Packs not recommended
SOIC-#DW	24* [0.60]	70 [1.75]	320 [8.10]	460 [11.60]	27 [0.65]	0.5 [0.03]	* - last pad is 72;

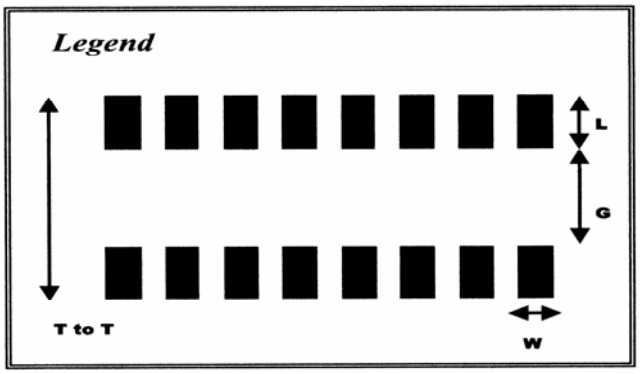


這種區域排列假設波能向兩個方向傳播，因此寬墊片在兩邊末端。

The land pattern assumes that the wave could be in either direction therefore the wide pads are on both ends.

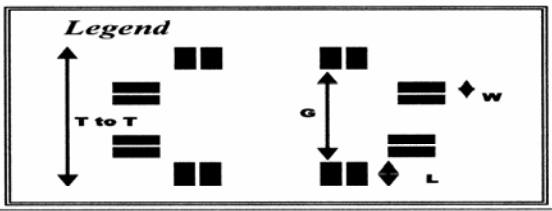
3.4.8 SOJ

SOJ	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
300 wide body	24 [0.60]	80 [2.00]	220 [5.60]	380 [9.60]	40 [1.00]	40 [1.00]	
350 wide body	24 [0.60]	80 [2.00]	270 [6.85]	430 [10.85]	40 [1.00]	40 [1.00]	
400 wide body	24 [0.60]	80 [2.00]	320 [8.10]	480 [12.10]	40 [1.00]	40 [1.00]	
450 wide body	24 [0.60]	80 [2.00]	370 [9.35]	530 [13.35]	40 [1.00]	40 [1.00]	



3.4.9 PLCC

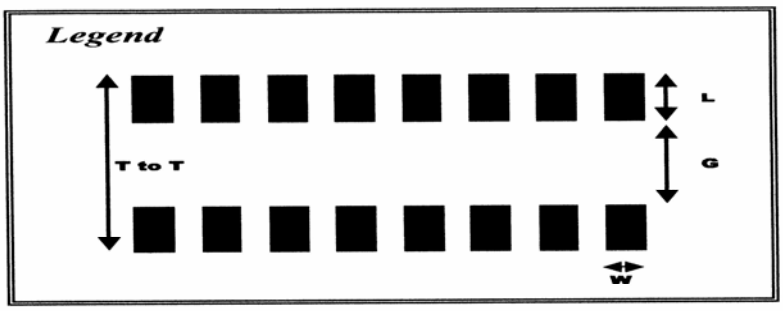
PLCC	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
18 rectangular	24 [0.60]	80 [2.00]	210 [5.35]	370 [9.35]	63 [1.60]	17 [0.43]	
			350 [8.90]	510 [12.90]	63 [1.60]	17 [0.43]	
20 square	24 [0.60]	80 [2.00]	270 [6.90]	430 [10.90]	60 [1.50]	20 [0.53]	
28 square	24 [0.60]	80 [2.00]	370 [9.40]	530 [13.40]	60 [1.50]	20 [0.53]	
28 rectangular	24 [0.60]	80 [2.00]	270 [6.90]	430 [10.90]	60 [1.50]	20 [0.53]	
			470 [11.90]	630 [15.90]	60 [1.50]	20 [0.53]	
32 rectangular	24 [0.60]	80 [2.00]	370 [9.40]	530 [13.40]	60 [1.50]	20 [0.53]	
			470 [11.90]	630 [15.90]	60 [1.50]	20 [0.53]	
44 square	24 [0.60]	80 [2.00]	570 [14.50]	730 [18.50]	60 [1.50]	20 [0.53]	
52 square	24 [0.60]	80 [2.00]	670 [17.00]	830 [21.00]	60 [1.50]	20 [0.53]	
68 square	24 [0.60]	80 [2.00]	870 [22.10]	1030 [26.10]	60 [1.50]	20 [0.53]	
84 square	24 [0.60]	80 [2.00]	1070 [27.20]	1230 [31.20]	60 [1.50]	20 [0.53]	



3.4.10 SSOP Small

SSOP Small	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
25 mil/0.635 mm*	16 [0.40]	80 [2.00]	190 [7.40]	350 [11.40]	21.5 [0.55]	21.5 [0.55]	
31 mil/0.8 mm*	20 [0.50]	80 [2.00]	345 [11.30]	505 [15.30]	22.0 [0.55]	28.0 [0.70]	

* Note: For SSOP footprints not listed in the above table refer to the optional figure pad design drawing in the next TSOP section to calculate various additional pad sizes.

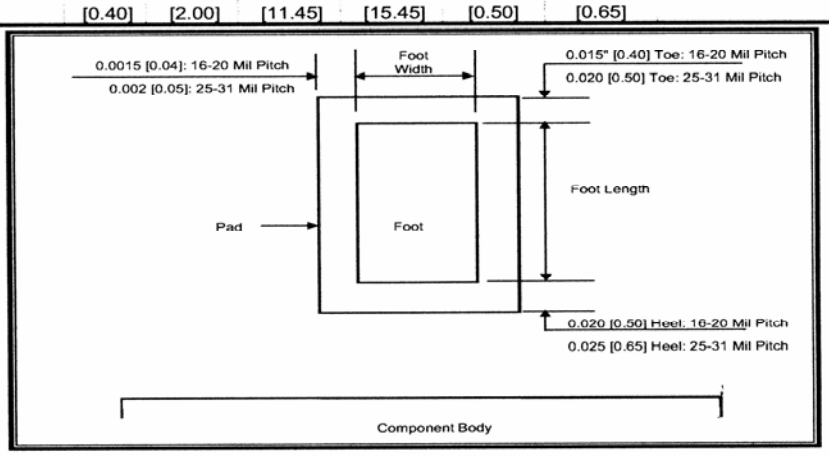


注：上圖不包含 SSOP 的值，在下個 TSOP 部分提到墊片設計圖的參照數值以計算變化增加的墊片尺寸。

Note: For SSOP footprints not listed in the above table refer to the optional figure pad design drawing in the next TSOP section to calculate various additional pad sizes.

3.4.11 TSOP

TSOP	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
16 mil/0.4 mm	10 [0.25]	70 [1.75]	620* [15.75]	760* [19.25]	15 [0.40]	20 [0.50]	NO SOLDER MASK BETWEEN PADS
20 mil/0.5 mm	12 [0.30]	70 [1.75]	700* [17.75]	840* [21.25]	15 [0.40]	20 [0.50]	NO SOLDER MASK BETWEEN PADS
26 mil/0.65 mm	16 [0.40]	80 [2.00]	450* [11.45]	610* [15.45]	20 [0.50]	25 [0.65]	



Optional Figure 16 maybe used to calculate the footprint pad size for any TSOP. * Use diagram to determine exact pad positioning.

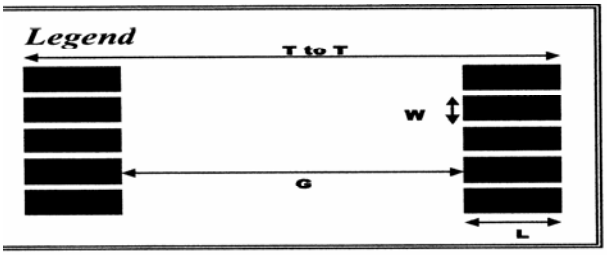
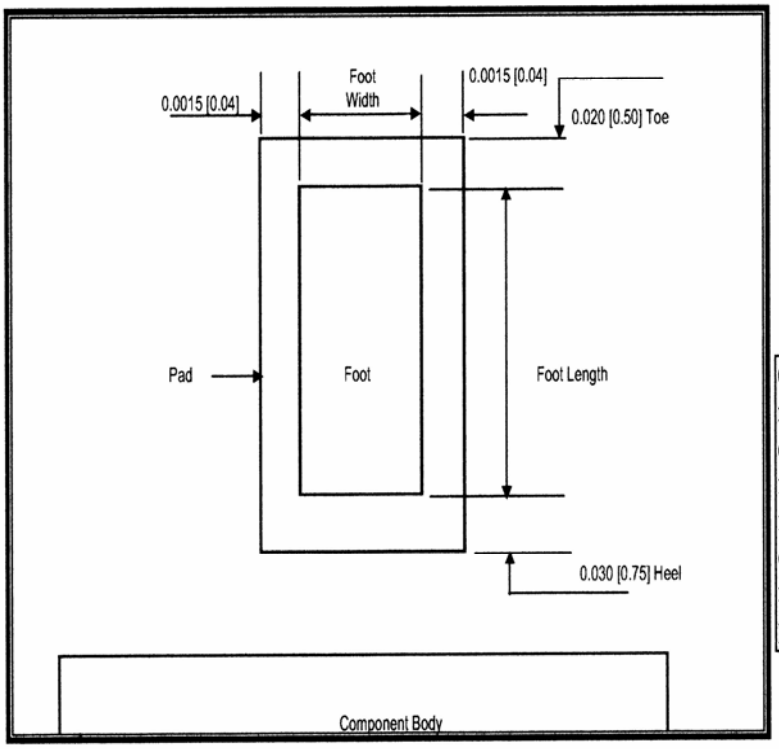


Figure 16- TSOP Pad Design

1. Pad **length** = toe + foot length + heel
2. Pad **width** = foot width + 2X side dimension
3. Pad **toe to toe** = component lead toe to toe + 2X pad toe
4. Pad **gap** = Pad toe to toe - 2X pad length
5. Pad **pitch** = component lead pitch
6. **Space between pads** = pitch - pad width

3.4.12 QFP

QFP	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
16 mil/0.4 mm (ex. 128 pin)	10 [0.25]	70 [1.75]	550* [14.00]	690* [17.50]	20 [0.50]	30 [0.75]	NO SOLDER MASK BETWEEN PADS
20 mil/0.5 mm (ex. 208 pin)	12 [0.30]	70 [1.75]	1080* [27.45]	1220* [30.95]	20 [0.50]	30 [0.75]	NO SOLDER MASK BETWEEN PADS
25 mil/0.635 mm (ex. 132 pin)	16 [0.40]	80 [2.00]	960* [24.40]	1120* [28.40]	20 [0.50]	30 [0.75]	
31 mil/0.8 mm (ex. 64 pin)	20 [0.50]	80 [2.00]	525* [13.40]	685* [17.40]	20 [0.50]	30 [0.75]	



Optional Figure 17 may be used to calculate the footprint pad size for any QFP. * Use diagram to determine exact pad positioning.

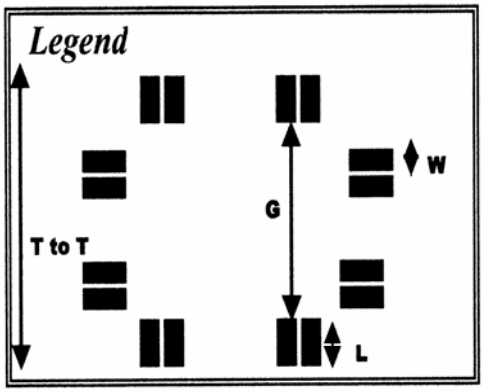


Figure 17- QFP Pad Design

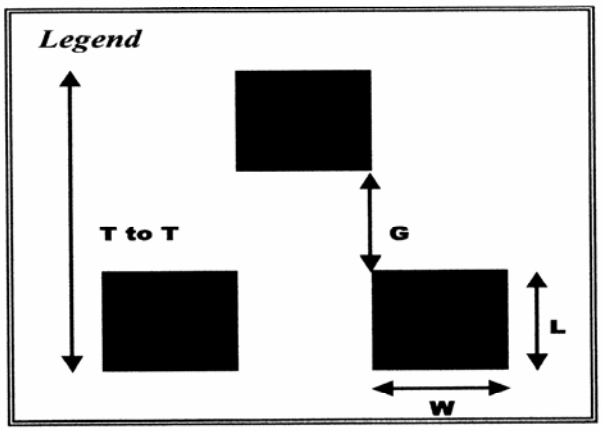
1. Pad **length** = 0.020 [0.50] + foot length + 0.30 [0.75]
2. Pad **width** = foot width + 0.003 [0.08] (0.0015 [0.04] per side)
3. Pad **toe to toe** = component lead toe to toe +0.040 [1.00]
4. Pad **gap** = Pad toe to toe - 2X pad length
5. Pad **pitch** = component lead pitch
6. **Space between pads** = pitch - pad width

Document Number CORSDC-10-100059 Revision: K Page: 54 of 95

3.4.13 SOT-23

3.4.13. SOT-23

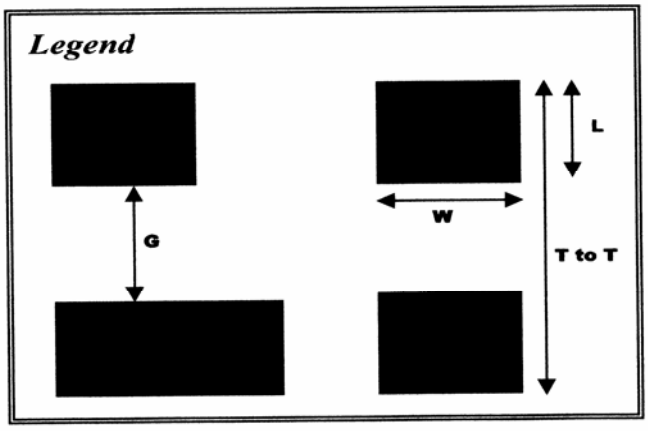
SOT-23		Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Component Type		mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
SOT-23 (Reflow)	Dual pads	40 [1.00]	50 [1.25]	35 [0.90]				Gap is between pads
	Single pad	40 [1.00]	50 [1.25]	40 [1.00]	140 [3.50]	22 [0.55]	5.5 [0.15]	Gap is between single and dual pads
SOT-23 (Wave)	Dual pads	40 [1.00]	70 [1.75]	35 [0.90]				Gap is between pads
	Single pad	40 [1.00]	70 [1.75]	45 [1.15]	185 [4.65]	44.5 [1.15]	3.0 [0.08]	Gap is between single and dual pads



3.4.14 SOT-143

3.4.14. SOT-143

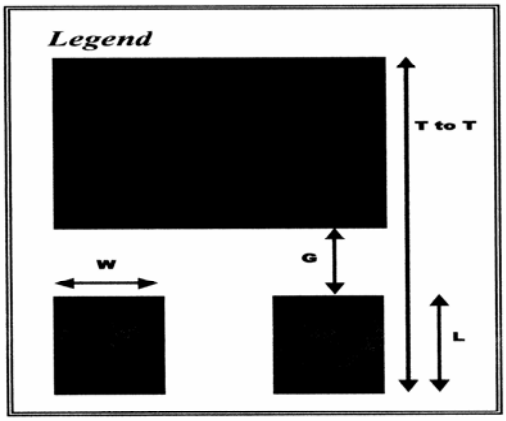
SOT-143	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	mils [mm]	
	40 [1.00]	40 [1.00]	40 [1.00]	120 [3.00]	17.5 [0.42]	6.5 [0.19]	Large pad is 50x40



3.4.15 D-PAK(TO 252/369)

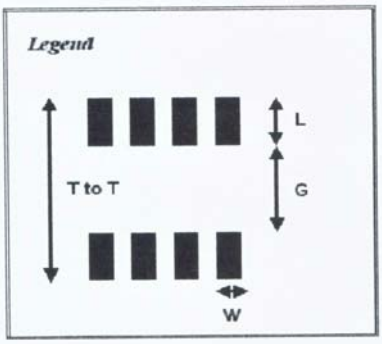
3.4.15. D-PAK (TO 252/369)

D-PAK (TO 252/369)	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
Small pads	63 [1.60]	118 [3.00]	118 [3.00]				Gap is between pads
Large pad	236 [6.00]	236 [6.00]	76 [1.90]	430 [10.90]	21 [0.53]	71 [1.80]	Gap is between large pad and small pads



3.4.16 晶片電阻/電容封裝 Chip Resistor / Capacitor Packs

Chip Resistor / Capacitor Packs	Pad Width W	Pad Length L	Pad Gap G	Toe-to-Toe TtoT	Toe Fillet (REF)	Heel Fillet (REF)	Comments
0302 [0806] Panasonic 14V, 4 terminals	14 [0.35]	16 [0.40]	12 [0.30]	44 [1.10]	10 [0.25]	0 [0.0]	Lower yielding part
0404 [1010] Panasonic 24V, 4 terminals	20 [0.50]	20 [0.50]	20 [0.50]	60 [1.50]	10 [0.25]	0 [0.0]	
0606 [1616] concave Panasonic V4V, 4 terminals	16 [0.40]	28 [0.70]	30 [0.75]	86 [2.15]	19 [0.48]	9.0 [0.23]	Fillets measured from bottom of dimple.
0606 [1616] convex Panasonic 34V, 4 terminals	16 [0.40]	28 [0.70]	40 [1.00]	96 [2.40]	16 [0.40]	0 [0.0]	
0804 [2010] Panasonic 28V, 8 terminals	12 [0.30]	20 [0.50]	20 [0.50]	60 [1.50]	10 [0.25]	0 [0.0]	End pads are 16 [0.40] wide Ensure pad pitch is correct
1206 [3216] concave Panasonic V8V, 8 terminals	16 [0.40]	28 [0.70]	30 [0.75]	86 [2.15]	19 [0.48]	9.0 [0.23]	Fillets measured from bottom of dimple.
1206 [3216] convex Panasonic 38V, 8 terminals	16 [0.40]	28 [0.70]	40 [1.00]	96 [2.40]	16 [0.40]	0 (0.0)	
1506 [3816] Panasonic 2HV, 16 terminals	12 [0.30]	28 [0.70]	31 [0.80]	87 [2.20]	12 [0.30]	4.0 [0.10]	
2010 [5022] concave Panasonic S8V, 8 terminals	28 [0.70]	50 [1.25]	40 [1.00]	140 [3.50]	26 [0.65]	2.0 [0.05]	



3.5 BGA 配圈排列方式 BGA Land Patterns

3.5.1 BGA 封裝描述 BGA Packaging Descriptions

PBGA	Plastic Ball Gird Array
TBGA	Tape Ball Grid Array
CBGA	Ceramic Ball Grid Array
CCGA	Ceramic (Wire) Column Grid Array
	Cast Column Grid Array
	Clasp Column Grid Array
CSP	Chip Scale Packaging

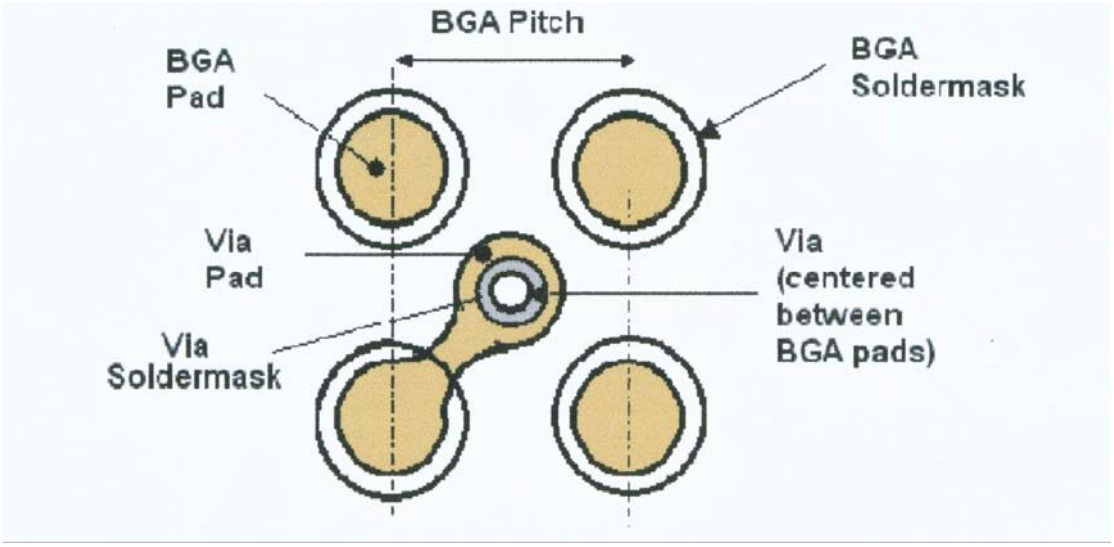
3.5.2 球狀材料描述 Ball Material Descriptions

PBGA	Eutectic(63Sn/37Pb)
TBGA	Eutectic(63Sn/37Pb) Single Metal Tape
	High Temp(90Sn/37Pb) Dual Metal Tape(IBM)
CBGA	High Temp(90Pb/10Sn)
CCGA	Column(90Pb/10Sn)
CSP	Eutectic(63Sn/37Pb)

注:關於錫焊球的組成和直徑,檢查 BGA/CSP 元件資料表和供應商,這些可能影響 PCB 的設計。下面的墊片尺寸可定義銅片的尺寸。

NOTE: Check with the BGA /CSP component datasheet and supplier concerning the composition and diameter of the solder ball as it may influence the PCB design. The below pad geometries provide for copper defined pads.

3.5.3 BGA 墊片/Via Dogbone 幾何學 BGA Pad/Via Dogbone Geometry



3.5.4 PBGA(50mil/1.27mm pitch)

Land Shape: Dogbone Ball Diameter: 25-30mils

PAD Geometry		VIA Geometry		
Land	Soldermask	Finished Hole	Pad Diameter	Top/Bot.side

Diameter	Diameter			Soldermask Diameter
25[0.64]	29[0.74]	12[0.30]	25[0.64]	18[0.45]

3.5.5 PBGA (39mil/1.00 mm pitch)

Land Shape: Dogbone Ball Diameter: 20-25mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
20[0.50]	24[0.60]	10[0.25]	22[0.55]	16[0.35]

3.5.6 Eutectic Ball TBGA (50mil/1.27mm pitch)

Land Shape: Dogbone Ball Diameter: 25-30mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
25[0.64]	29[0.74]	12[0.30]	25[0.64]	18[0.45]

3.5.7 High Temp Ball TBGA (50 mil/1.27 mm pitch)

Land Shape: Dogbone Ball Diameter: 25mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
28.5[0.72]	32.5[0.83]	12[0.30]	25[0.64]	18[0.45]

3.5.8 CBGA (50 mil/1.27 mm pitch)

Land Shape: Dogbone Ball Diameter: 35mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
28.5[0.72]	32.5[0.83]	12[0.30]	25[0.64]	18[0.45]

3.5.9 CCGA (50 mil/1.27 mm pitch)

Land Shape: Dogbone Ball Diameter: 22.5mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
28.5[0.72]	32.5[0.83]	12[0.30]	25[0.64]	18[0.45]

3.5.10 CCGA (39 mil/1.00 mm pitch)

Land Shape: Dogbone Ball Diameter: 22.5mils

PAD Geometry	VIA Geometry

Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
27[0.70]	31[0.80]	8[0.20]	18[0.46]	12[0.30s]

3.5.11 CBGA (39 mil/1.00 mm pitch)

Land Shape: Dogbone Ball Diameter: 27.5mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
27[0.70]	31[0.80]	8[0.20]	18[0.46]	12[0.30]

3.5.12 CSP/microBGA (31.5 mil/0.8 pitch)

Land Shape: Dogbone Ball Diameter: 14-20mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
16[0.40]	20[0.50]	8[0.20]	18[0.46]	12[0.30]

3.5.13 CSP/microBGA (30 mil/0.75 mm pitch)

Land Shape: Dogbone Ball Diameter: 14mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
14[0.35]	18[0.45]	8[0.20]	18[0.46]	12[0.30]

3.5.14 CSP (25.6 mil/0.65 mm pitch)

Land Shape: Dogbone Ball Diameter: 8-12mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
12[0.30]	16[0.40]	Microvia or surface wiring only See detail in section 3.5.16 for microvia options		

3.5.15 CSP (19.7 mil/0.50 mm pitch)

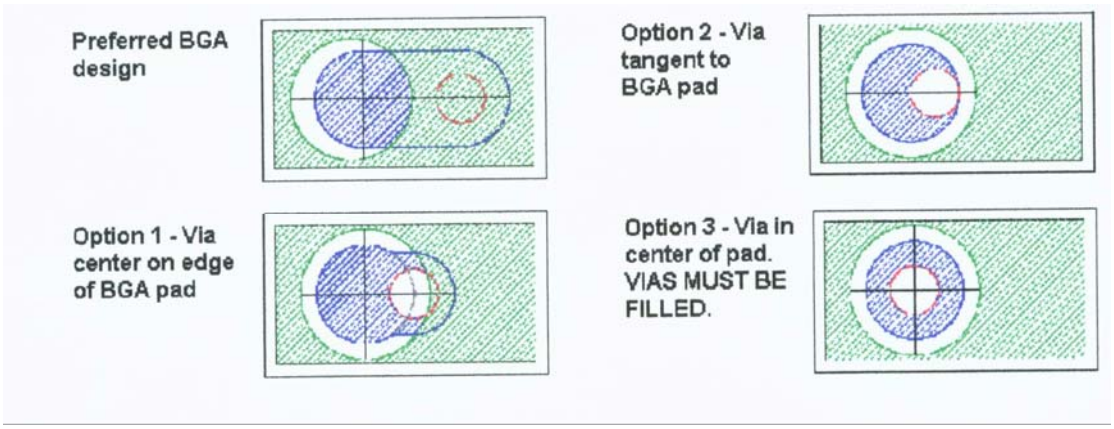
Land Shape: Dogbone Ball Diameter: 8-12mils

PAD Geometry		VIA Geometry		
Land Diameter	Soldermask Diameter	Finished Hole	Pad Diameter	Top/Bot.side Soldermask Diameter
11[0.28]	15[0.38]	Microvia or surface wiring only See detail in section 3.5.16 for microvia options		

3.5.16 BGA 微型通孔選擇 BGA Microvia Options

如果標準通孔不與要求的密度相符，就可選擇下面的微型通孔。這些選項是爲優先選擇，都是建立在經驗的基礎上發展起來的，以定義 BGA 焊接頭空焊的存在，想更詳細地瞭解參照 4.3.11 部分。對於 2，3，選項，最重要的是聯繫你的 DFM 瞭解更多的關於結構說明和買方的選擇這些有代表性的資訊。

The microvia options below can be used if standard through hole vias are not compatible with the required density. These options, shown in order of preference, were developed based on experiments that determined the presence of voids in the BGA solder joints. See section 4.3.11 for further details. For options 2 and 3, it is very important to contact your DFM representative for further information regarding the fabrication specification and vendor selection.



3.6 SMT 間距規則　　SMT Spacing Rules

3.6.1 簡介　　Introduction

PCB 裝配完後，有無數個元件的尺寸和形狀，他們也伴隨著一系列功能和性能的局限來獲得期望的終端產品。SMT 間距規則爲高質量，可機加產品提供最小的尺寸，這種產品如果需要能重做，同時這個規則爲設計者提供最大的可行性以迎合產品的功能和性能要求。

PCB assemblies come in numerous sizes and shapes, with few or many components. They also come with a variety of functional and performance constraints to achieve the desired end product. The SMT spacing rules provide the minimum dimensions for a good-quality, machine-producible product that can be reworked if required. At the same time, the rules offer the designer maximum flexibility to meet the product's functional and performance objectives.

接下來 SMT 間距規則是推薦 SMT 與 SMT 和 SMT 與 PTH 元件之間最小間距。間

距大小是基於鍍金屬區的寬度或是元件體中最大的。

The following SMT spacing rules are minimum recommended spacings between SMT to SMT and SMT to PTH components. Spacing dimensions are based on the width of the land metallization or the component body, whichever is greatest.

3.6.2 洄流焊 BGA 到（同側）晶片間距 Reflow BGA to (Same Side) Chip Spacing

因爲用有罩的噴嘴，這樣就需要定期地重做 BGA，要求優先保持晶片體到 BGA 體之間間距是每一間距的 0.125(3.18)參照圖 1，然而有些時候當需要退耦和其他晶片移 BGA 體更近的時候，來獲得更好的電子設計功能。必要時，移晶片更近至 BCA 體的反面板的逃逸通道。如果電子元件不允許信號穿過這個通道，最後的選擇方式是在 BGA 同側移近晶片。這些晶片必須放在 BGA 周圍的最小 0.020(0.50)到最大 0.080(2.00)範圍之內，這有利於返修工藝，在重做進程中，這樣晶片將放在噴嘴的裏面，允許噴嘴平放在板上，應該注意的是在返修後，可能需要花額外的人力去修正晶片。

Because it is necessary to rework the BGA periodically using a hooded nozzle, it is strongly preferred to keep the “chip body to BGA body” spacing at 0.125(3.18) per spacing chart (part 1). However, there are times when decoupling caps and other chip parts need to be moved closer to the BGA lead/ball to obtain better electrical design functionality. When necessary, move the chips closer to the breakout vias on the opposite side of the board from the BGA body. As a last resort, if electrical requirements will not permit the signal transfer through the vias, the chips may be moved closer to the BGA on the same side of the board. These chips must be lay in an AREA defined by a distance of 0.020(0.50) minimum to 0.080(2.00) maximum surrounding the BGA body. This benefits the repair process in that the chips will lie inside the nozzle allowing the nozzle to rest flat on the board, during the reworking process. It should be noted that an additional production cost may be required to manually touch up the chips after the repair process.

3.6.3 映射 BGA Mirror Imaged BGAs

必須小心,當 BGA 映射而保持板不變形和在接頭處強度提高。盡可能保持 BGA 的尺寸小於 1.00(25.4)平方英寸（BGA 越大，返修的可能性就越大），可能的話，提高板子的厚度來幫助減小在元件的重量下的變形和提高焊接頭的可靠性。

Care must be taken when BGAs are “mirror imaged” to keep the board free from warpage

and increased strain at the solder joint. Where possible, keep the BGA size to less than 1.00(25.4) square. (The larger the BGA size the greater the possibility of rework.)Where possible, increase the board thickness to help reduce the warpage under the devices and increase the solder joint reliability.

3..6.4 背對背放置 BGA 或 CSP BGA or CSP Placed Back-to-Back

地方允許的話，推薦類似背對背的 BGA 和 CSP，元件被彼此偏移最小值.200(5.00)

來阻止板變形，一些 dogbone 在兩個元件之間共用通孔，這樣易於產生焊接頭應

變，相同周長的 BGA 放成背對背形式是優先整體放置 BGA，由於 BGA 球被放置

超過了元件沖模的參數範圍。

It is recommended that, where possible, similar back-to-back BGAs and CSPs be offset from each other a minimum of 0.200(5.00) to prevent board warpage under the devices. Any dogbone shared vias between the two devices are susceptible to solder joint strain. Similar perimeter BGAs placed back-to back are preferred over fully arrayed BGAs since the BGA balls are located beyond the parameters of the device die.

3.6.5 SMT 被動對被動式封裝-回流焊與波焊工藝制定

SMT Passive to Passive packages-Reflow and Wave Processing

		201 End	201 Side	402 End	402 Side	603 End	603 Side	805 End	805 Side	1206 End	1206 Side	1210 End	1210 Side	Tant A-D/Large Cer. End	Tant A-D/Large Cer. Side	PIH/SMT (5)	Press Fit Pins/body
201 End	Reflow (2)	10	12	10	15	10	20	10	25	10	30	10	30	10	40	150	200/150
	Wave (1)																
201 Side	Reflow (2)		12	12	15	12	20	12	25	12	30	12	30	12	40	150	200/150
	Wave (1)																
402 End	Reflow (2)			12	15	12	20	12	25	12	30	12	30	12	40	150	200/150
	Wave (1)																
402 Side	Reflow (2)				15	15	20	15	25	15	30	15	30	15	40	150	200/150
	Wave (1)																
603 End	Reflow (2) (6)					12	20	12	25	12	30	12	35	12	40	150	200/150
	Wave (1)(3)					40	35	45	40	60	50	60	70	200	200		
603 Side	Reflow (2) (6)						20	20	25	20	30	20	35	20	40	150	200/150
	Wave (1)(3)						40	40	45	45	50	50	70	200	200		
805 End	Reflow (6)							12	25	12	30	12	35	12	35	150	200/150
	Wave (3)							45	40	65	50	70	80	200	200		
805 Side	Reflow (6)								25	30	30	30	40	30	40	150	200/150
	Wave (3)								45	50	65	70	80	200	200		
1206 End	Reflow (6)									12	30	12	40	12	40	150	200/150
	Wave (3)									65	50	100	90	200	200		
1206 Side	Reflow (6)										30	40	40	35	40	150	200/150
	Wave (3)										65	90	100	200	200		
1210 End	Reflow											12	40	12	40	150	200/150
	Wave (3)											100	90	200	200		
1210 Side	Reflow												40	40	40	150	200/150
	Wave (3)												100	200	200		
Tant/Lg Cer End	Reflow													12	40	300	200/150
	Wave (3)(4)													200	200		
Tant/Lg Cer Side	Reflow													40	40	375	300/150
	Wave (3)(4)													200	200		

Note (1) - Wave solder of 0201and 0402's not allowed and not recommended for 0603's.
Note (2) - Multi-leaded networks require the same spacing as associated chip spacings shown.
Note (3) - Spacings assume proper component orientation and alignment (Section 3.1.3)
Note (4) - Wave solder of tantalum caps and large ceramics not recommended
Note (5) - Spacing measured from through hole land edge to SMD land edge for selective soldering applications.
Note (6) - Use equivalent size for low inductance capacitors (0306, 0508, 0612). "End" indicates the position of the terminals.

METRIC EQUIVALENTS

mil	mm	mil	mm	mil	mm
10	0.25	40	1.00	90	2.30
12	0.30	45	1.15	100	2.50
15	0.38	50	1.25	125	3.20
20	0.50	60	1.50	150	3.80
25	0.64	65	1.65	200	5.00
30	0.75	70	1.75	300	7.60
35	0.90	80	2.00	375	9.50

3.6.6 首選回流焊元件間距(part1)　　Preferred Reflow Component spacing(part1)

		201 End	201 Side	402 End	402 Side	603 End	603 Side	805 End	805 Side	1206 End	1206 Side	1210 End	1210 Side	Tant A-D/Large Car. End	Tant A-D/Large Car. Side	PIH/SM (5)	Press Fit Pins/body
201 End	Reflow (2)	10	12	10	15	10	20	10	25	10	30	10	30	10	40	150	200/150
	Wave (1)																
201 Side	Reflow (2)		12	12	15	12	20	12	25	12	30	12	30	12	40	150	200/150
	Wave (1)																
402 End	Reflow (2)			12	15	12	20	12	25	12	30	12	30	12	40	150	200/150
	Wave (1)																
402 Side	Reflow (2)				15	15	20	15	25	15	30	15	30	15	40	150	200/150
	Wave (1)																
603 End	Reflow (2) (6)					12	20	12	25	12	30	12	35	12	40	150	200/150
	Wave (1)(3)					40	35	45	40	60	50	60	70	200	200		
603 Side	Reflow (2) (6)						20	20	25	20	30	20	35	20	40	150	200/150
	Wave (1)(3)						40	40	45	45	50	50	70	200	200		
805 End	Reflow (6)							12	25	12	30	12	35	12	35	150	200/150
	Wave (3)							45	40	65	50	70	80	200	200		
805 Side	Reflow (6)								25	30	30	30	40	30	40	150	200/150
	Wave (3)								45	50	65	70	80	200	200		
1206 End	Reflow (6)									12	30	12	40	12	40	150	200/150
	Wave (3)									65	50	100	90	200	200		
1206 Side	Reflow (6)										30	40	40	35	40	150	200/150
	Wave (3)										65	90	100	200	200		
1210 End	Reflow											12	40	12	40	150	200/150
	Wave (3)											100	90	200	200		
1210 Side	Reflow												40	40	40	150	200/150
	Wave (3)												100	200	200		
Tant/Lg Cer End	Reflow													12	40	300	200/150
	Wave (3)(4)													200	200		
Tant/Lg Cer Side	Reflow													40	40	375	300/150
	Wave (3)(4)													200	200		

Note (1) - Wave solder of 0201and 0402's not allowed and not recommended for 0603's.
Note (2) - Multi-leaded networks require the same spacing as associated chip spacings shown.
Note (3) - Spacings assume proper component orientation and alignment (Section 3.1.3)
Note (4) - Wave solder of tantalum caps and large ceramics not recommended
Note (5) - Spacing measured from through hole land edge to SMD land edge for selective soldering applications.
Note (6) - Use equivalent size for low inductance capacitors (0306, 0508, 0612). "End" indicates the position of the terminals.

METRIC EQUIVALENTS

mil	mm	mil	mm	mil	mm
10	0.25	40	1.00	90	2.30
12	0.30	45	1.15	100	2.50
15	0.38	50	1.25	125	3.20
20	0.50	60	1.50	150	3.80
25	0.64	65	1.65	200	5.00
30	0.75	70	1.75	300	7.60
35	0.90	80	2.00	375	9.50

3.6.7 首選回流焊接元件間距 （part2）

Preferred Reflow Component Spacing (part 2)

Note: Dimensions in mils

DEVICE Type	CHIP narrow	CHIP wide	SOT narrow	SOT wide	SOIC narrow	SOIC wide	PLCC narrow	SOJ narrow	SOJ wide	QSOP wide	QSOP narrow	BGA body
CHIP wide	See passive spacing matrix in section 3.6.5		25	25	30	30	50	50	30	50	50	125
CHIP narrow			25	25	30	30	50	50	30	50	50	125
SOT wide			30	30	25	25	40	50	30	50	50	125
SOT narrow			30	30	25	25	40	50	30	50	30	125
SOIC narrow					30	30	30	50	70	50	50	125
SOIC wide					30	30	30	50	70	50	50	125
PLCC narrow							70	50	50	70	70	125
SOJ narrow								50	50	70	70	125
SOJ II wide								50	50	70	70	125
QSOP wide										70	70	125
QSOP narrow										70	70	125
BGA												125
PGA												
QFP 16 mil												
QFP 20/25												
CONN narrow												
CONN wide												
Prs Fit Leads												
PIH/SMD												
AXIAL narrow												
AXIAL wide												
DIP narrow												
DIP wide												

METRIC EQUIVALENTS

mil	mm	mil	mm	mil	mm
10	0.25	40	1.00	90	2.30
12	0.30	45	1.15	100	2.50
15	0.38	50	1.25	125	3.20
20	0.50	60	1.50	150	3.80
25	0.64	65	1.65	200	5.00
30	0.75	70	1.75	300	7.60
35	0.90	80	2.00	375	9.50

3.6.8 貼裝孔範圍區　　Mounting Hole Clearance Zone

爲阻止元件通常指設置在載波插入平衡插滑區的小晶片在滑動運行期間掉下來，下面建立的指導原則設計者應該嚴格遵守。

To prevent parts, usually small chips, located in the “carrier standoff insertion slide zone” from being knocked off the board during the sliding operation, the following guideline found in (Figure 18) should be adhere to by the designer.

3.6.9 貼標籤零件的間距範圍要求　　Device To Label Spacing Clearance Required

fine pitch 元件（低於 0.025[0.065]）和其他貼標籤例如：0402，電阻器，BGA，CSP 最小值爲 0.75[19.05]。

Labels are to be placed a minimum of 0.75[19.05] from all fine pitch device (with 0.025[0.065] pitch and below) and other devices such as 0402s, resistors network, BGAs and CSPs.

4.0 印刷板製作的指導原則　　Fabrication Guideline for Printed Boards

4.1 簡介 Introduction

這部分“製作設計”包含了資料通常被從事於印刷電路板設計的設計者所用。印電路板面是嚴格類型，利用兩個通孔和 SMT， 電鍍和/或蝕刻工藝加工。這篇檔用於連接 IPC-2220 系列檔和 Solectron PCB 結構規格程式 MTL-10-004019，這些檔將給設計帶來效益，便於加工，測試和可修印刷電路提供有用的資訊。

This section of “Design for Fabrication” contains general information necessary for use by the circuit board designer engaged in the design of printed circuit boards(PCB). The printed circuit boards covered are the rigid type, utilizing both through-hole and surface mount devices(SMT), manufactured by the electroplating and/or etch process. This document, used in conjunction with IPC-2220 series documents and Solectron PCB Fabrication Specification Procedure MTL-10-004019, will provide the information necessary for designing cost effective, manufacturable, testable and repairable printed circuit boards.

注：生產可行性設計部分 2.0 是作爲附加的要求，這將影響製作設計進程。

Note: See : “Design for Manufacturability” section 2.0 for additional requirements that will affect the “Design for Fabrication” process.

4.2 選擇恰當的工藝 Choosing The Proper Technology

爲一些給定設計，選擇正確的工藝是設計出經濟的和適合加工的完美 PCB 板裝配的成功基礎。決定所用的技術類型，應該考慮所用的錫焊工藝，板的密度，元件的封裝類型。大部分設計可用標準工藝，但有些特殊的較小通孔尺寸，線路寬度和間距尺寸，就需要用超高密度的微型通路和 HDI（高密度相互連接）技術。爲這些設計的特殊要求，參考 Solectron’s 高密度設計原則，通常的佈線規則將提供最經濟的高密度互相連接。

Choosing the proper technology for any given design is critical to the success of a cost effective and manufacturable finished PCB assembly. To determine the type of technology to use one should consider the soldering processes used, the board density, and the device size/package types. Most designs can be done with standard technologies but some must be done using ultra high density micro-vias and HDI (High Density Interconnect) technologies with reduced via sizes, trace widths and spacings. Reference Solectron’s High Density Design Guidelines for specific requirements for these designs. As a general rule of thumb the following trace-offs will provide the most cost effective higher interconnect density.

- 加層前，用較小的線寬，孔和線距

- 研究板怎樣能合理的拼接產品 以確保最大限度材料使用
- 設計埋入式通孔前，先用盲孔通孔
- 對於小數量層如果沒有阻抗和電源的約束，就可用電源和接地層劃分
- 在用於提高整體密度以允許有更大的貼裝空間，用埋入式電容

爲一個給定板，密度確定正確的技術，可看下面：

IPC-2221, 3.6 部分, 佈局(用於 HDI 密度)

IPC-2315, 5 部分, 佈局 (用於 HDI 密度)

對於一個總的標準技術和超高微觀通路技術看下表（對特別的尺寸，聯繫當地板買方。

- Use smaller line/width, smaller holes and trace spaces before adding layers.
- Investigate how boards will fit into a production paned to ensure that maximum material utilization occurs.
- Use blind vias before designing buried vias to the design.
- Use a power and ground mesh if the design is free of impedance requirements and electrical constraints for smaller layer counts.
- Use buried capacitance where applicable to increase the overall density allowing more room for mounting additional actives.
  To determine the proper technology for a given Board Density see the calculators found in:
  IPC-2221, Section 3.6, Layout Evaluation(use for HDI densities)
  IPC-2315, Section 5, Layout Evaluation (use for HDI densities)
  For an overview of standard technologies and ultra high micro-via technologies see the table below.(Contact the local board vendor for specific dimensions)

4.2.1 優先標準和 HDI 密度技術規格

The Preferred Standard and HDI Density Technology Roadmaps

DHD=Drilled Hole Diameter. -The finished nominal hole size plus the plating manufacturing compensation A/R-annular ring-distance Between the drilled hole and edge of pad	Stand Technology -Though vias -10 mil diameter min. -Volume Production	HDI Technology -Blind/microvias -6mil diameter -Volume Production	Advanced Technology -Blind/buried/micro vias -4 mil diameter -Limited capability -Cost adder
Inner Layer Specifications:			
Inner Layer-Min.1 oz Trace width/spacing	0.004[0.10]/0.004[0.10]	0.004[0.10]/0.004[0.10]	0.0035[0.09]/0.004[0.10]

Inner Layer-Min.1/2 oz Trace width/spacing	0.003[0.08]/0.004[0.10]	0.004[0.10]/0.003[0.08]	0.002[0.05]/0.003[0.08]
Min. Pad diameter to obtain hole with an annular ring requirement	0.012[0.30]+DHD+2x min.A/R	0.010[0.25]+DHD+2X min. A/R	
Min. pad diameter to obtain hole Tangency:	Add 0.012[0.30] to DHD	0.010[0.25]+DHD	
Power plane clearance	DHD+0.024[0.60]	DHD+0024[0.60]	
Outer Layer Specification			
1/2 oz .Min. Trace width/spacing	0.004[0.10]/0.005[0.13]	0.004[0.10]/0.004[0.10]	0.003[0.08]/0.003[0.08]
Min. Pad diameter to obtain hole Tangency	Add 0.010[0.25] to DHD	Add 0.010[0.25] to DHD	
Min. Pad diameter to obtain a hole with an annular ring requirement	0.010[0.25]+DHD+2X min. A/R	0.010[0.25]+DHD+2X min. A/R	
NPTH-to-copper for primary drill	0.015[0.38]	0.015[0.38]	0.010[0.25]
Outer Layer-Trace/SMT Pad Spacing	0.006[0.15]	0.006[0.15]	0.004[0.10]
Outer Layer-Trace/PH Pad Spacing	0.006[0.15]	0.006[0.15]	0.004[0.10]
Outer Layer-Trace/Via Pad Spacing	0.006[0.15]	0.006[0.15]	0.004[0.10]
General overall requirements			
Min. PCB Edge-to-Conductor	0.025[0.65]	0.025[0.65]	
Min. NPTH-to-trace	0.015[0.38]	0.015[0.38]	
Layer-to-Layer Registration	0.005[0.13]Front to Back	0.005[0.13]Front to Back	0.003[0.08]Front to Back
Hole Location tolerance	+/-.002[0.05]	+/-.002[0.05]	+/-.001[0.025]
Board Dimensions-overall tolerance	+/-.005[0.13]	+/-.005[0.13]	+/-.005[0.13]
Fabrication Radius	0.031[0.80]Min	0.031[0.80]Min	0.015[0.38]Min
Max. NO. Layers(based on impedance & via size	18 0.093[2.40]thick board	14 0.080[2.00]thick board	12 0.062[1.60]thick board
Hole Specification			
Minimum mechanical drilled hole diameter	0.010[0.25]	0.010[0.25]	0.008[0.20]
Minimum laser drilled hole diameter	0.006[0.15]micro-via 0.012[0.30] blind	0.006[0.15]micro-via 0.012[0.30] blind	0.004[0.10]micro-via 0.010[0.25] blind

	core via	core via	core via
Maximum drilled hole diameter	0.250[6.35]	0.250[6.35]	
Maximum aspect ratio	10:1	10:1	12:1-18:1
Plated hole diameter tolerance	+/-0.003[0.08]	+/-0.003[0.08]	+/-0.002[0.05(OSP/ NiAu)
Drilled hole diameter tolerance	+/-0.0015[0.038]	+/-0.0015[0.038]	+/-0.001[0.025]
Hole-to-hole location accuracy	+/-0.003[0.08](0.0085[0.21]DTP)	+/-0.003[0.08](0.0085[0.21]DTP	
Pad-to-Hole Requirements			
Min. Plated Hole Size(FHS)for via	0.008[0.20]TH	0.006[0.15](Blind micro via)	0.004[0.10](blind micro via)
Min. Outer/Inner Layer NPTH Hole-to -Trace	0.015[0.38]	0.015[0.38]	
Min. Annular Ring(TH Comp)	0.0095[0.24]	0.0095[0.24]	
Power plane minimum anti-pad clearance	Drilled Hole+0.024[0.60]	Drilled Hole+0.024[0.60]	
Via Requirements			
Via land size	0.019[0.48] for 0.008 [0.20]FHS	0.016[0.40] for 0.006 [0.15]laser FHS	0.014[0.35] for 0.004 [0.10]laser FHS
Via inner Layer anti-pad diameter for a 0.008[0.20]FHS	0.032[0.81]	0.032[0.81]	
Via/Via barrel spacing min.	0.021[0.53]	0.021[0.53]	
Via min. annular Ring	0.0055[0.14]	0.004[0.10]	
Via-to-SMD pad end spacing	0.010[0.25]	0.010[0.25]	
Board Material			
Laminate type available:	FR-4(Tg=/>135Cmulti-functional)	FR-4(Tg=/>135C multi-functional)	FR-4 or BT High(Tg>170C multi-functional)
Foil weight:(inner layer)	1/2,1 ounce	1/2,1 ounce	2,3 ounce
Foil weight:(outer layer)	1/2 ounce	1/4 ounce	1/4ounce,1 ounce,2 ounce
Dielectric & PCB thickness:			
Minimum overall board thickness	0.012[0.31]	0.012[0.31]	0.008[0.20]
Maximum overall board thickness	0.280[7.11]	0.480[12.19]	0.250[6.35]
Thickness tolerance	+/-10%	+/-10%	+/-8%

Warp and Twist	1.0%	1.0%	0.7%,0.5%
Minimum dielectric spacing:	Cores:0.004[0.10] Prepreg:0.0035[0.089]	Cores:0.004[0.10] Prepreg:0.0035[0.089]	Cores:0.004[0.10] Prepreg:0.0035[0.089]
LPI Soldermask Specifications:			
Min. average thickness over trace	0.0005[0.013]	0.0005[0.013]	
Registration tolerance	+/-0.003[0.08]	+/-0.002[0.05]	+/-0.002[0.05]
Spacing (for mask between pads)	0.009[0.23]	0.009[0.23]	0.007[0.18]
Available colors	Green	Green	clear
Surface Finishes Available:	(see section 2.5)		
Hot air Solder Level thickness	50-1500u in	50-1500u in	
OSP	solderable	solderable	
Electroless Ni/Immersion Au	100u in Ni/2-8u Au	100u in Ni/2-8u Au	
Edge plated fingers	100-150u in Ni/20-50u in Au	100-150u in Ni/20-50u in Au	
Fused Tin Lead			0.0003[0.008]min (as plated)
Immersion Tin	25.6 u in	25.6 u in	
Immersion Silver	3.2-6.4u in	3.2-6.4u in	
Legend Specifications			
colors	White, Yellow	White, Yellow	Orange, Black
Min. smallest line width	0.008[0.20]	0.008[0.20]	0.006[0.15]
Location accuracy	+/-0.008[0.20]	+/-0.008[0.20]	+/-0.006[0.15]
Minimum character height	0.045[1.14]	0.045[1.14]	0.030[0.76]
Board Outline Routing			
Edge-to-edge tolerance	+/-0.010[0.25]	+/-0.010[0.25]	+/-0.003[0.08]
Edge-to-datum hole tolerance	+/-0.005[0.13]	+/-0.005[0.13]	+/-0.003[0.08]
Minimum internal radius	0.047[1.20]	0.047[1.20]	0.016[0.41]
Minimum External radius	None	None	None
Max. routed hole diameter and tolerance	1.250[31.75]+/-0.010 [0.25]	1.250[31.75]+/-0.010 [0.25]	1.250[31.75]+/-0.005 [0.13]
Min. routed hole diameter and tolerance	0.250[6.35]+/-0.005 [0.13]	0.250[6.35]+/-0.005 [0.13]	0.250[6.35]+/-0.003 [0.08]
Preferred router bits	0.093[2.40]	0.093[2.40]	0.031[0.79],0.047[1.20] 0.062[1.60].0.125[3.18]
Board Outline Scoring			

Minimum web thickness	0.012[0.30]	0.012[0.30]	0.004[0.10]
Available Scoring angles	30 degrees	30 degrees	45 or 60 degrees
Web thickness tolerance	+/-0.003[0.08]	+/-0.003[0.08]	+/-0.002[0.05]
Location Tolerance	+/-0.005[0.13]	+/-0.005[0.13]	
Jump score capability	Yes	Yes	
Edge beveling			
Available angles	30 degrees	30 degrees	20,45,70 degrees
Angle tolerance	+/-5 degrees	+/-5 degrees	
Available depths	0.015[0.38]to 0.075[1.90]	0.015[0.38]to 0.075[1.90]	0.010[0.25]-0.080[2.03]
Depth Tolerance	+/-0.010[0.25]	+/-0.010[0.25]	+/-0.007[0.18]
Electrical Characteristics:			
Impedance Tolerance	+/-10%	+/-10%	
Etch Factors			
Inner Layer 2 oz.	0.002[0.05]	0.0025[0.063]	N/A
Inner Layer 1 or oz.	0.001[0.25]	0.00125[0.032]	N/A
Inner Layer 1/2 oz.	0.0005[0.012]	0.00063[0.016]	N/A
Inner Layer 1/4 oz.	0.00025[0.006]	0.00036[0.009]	N/A
Inner Layer 1/8oz.	0.00012[0.003]	0.00018[0.004]	N/A
Inner Layer 2 oz.	+.001[0.025]/-.003[0.08]	0.003[0.08]	N/A

4.3 微型通孔技術，分層結構和 DFM 要求

Micro-via technology, stackup structures and DFM Requirements

在當今市場中，至少有 12 種以上 HDI 類型，最通常的特徵是在 HDI 板上盲式微型通孔（類型 I ）傳統的銑床加工工藝通常要求一些小型盲式通孔，特別是直徑爲(0.006[0.15])或更小盲孔，埋入式通孔很普及地用於連接微型通孔以推進佈線密度到一個較高水準。

There are more than a dozen type of high density interconnect (HDI) solutions being offered in the market today. The most common feature in an HDI board is blind microvias (type I, blind microvias). Processes other than traditional mechanical drilling are usually require to form these small blind vias, typically (0.006[0.15]) in diameter or less. Buried vias are also gaining popularity in combination with the microvias to boost the routing density to an even higher level.

這個部分所定義的要求是爲了發展新 PCB 技術質量給 Solectron 產品，這些要求超越了標準技術和工藝說明的定義範圍，這部分的目的是捕獲變化基本技術的設計傾向，新的基本技術說明被用到下面領域：

- 盲孔微型通孔由鐳射切除和電鍍組成

- microvia-in-pad 爲 BGA 或 CSP 和其他元件讓位，注意：看題目“在 BGA 或 CSP 下的墊片優先提供微型通孔”
- 埋入中心通孔或通孔通路連接所有埋入層
- 專用基板材料到微型通孔技術

This section defines the requirements for new PCB technology qualification being developed for use in Solectron products, which are beyond the definition of the standard technologies documented and procurement specifications. The intent of this section is to capture the design intent for various substrate technologies. The specific new substrate technologies being used are in the following areas:

- Blind microvia holes formed by laser ablation and plating.
- Blind microvia-in-pad for BGA/CSP and other device escapes. CAUTION: See section entitled”Micro-in-Pad under a BGA or CSP” for the preferred method of providing microvias under BGAs and CSPs.
- Buried Core Vias or through hole vias connecting to all inter-layers
- The use of specific laminate material dedicated to micro-via technology.

4.3.1 分層要求 Layer Stackup Requirements

根據機械和電子要求確定分層，分層資料將通常在 PCB 結構或專門的特徵圖中詳細列出。

分層應該列出的是：

* 整個 PCB 的厚度和公差

* 信號、電源和地電位設置

* 每個信號層的阻抗要求

* 臨界層到層的間距

* 盡可能，只在核心厚度上通過分層

Layer stackups are determined by mechanical and electrical requirements. Stackup information would usually be detailed on the PCB fabrication or specific feature drawing.
The Stackup would show:
*Overall PCB thickness and tolerance(i.e.,reduce layer count or reduce board size)
* Placement of signal, power and ground planes.
* Impedance requirements for each signal layer.
* Critical lay-to-layer spacing (and tolerance)

* Where possible, only on core thickness should be used throughout the stackup.

4.3.2 HDI 分層選用 RCC 和 FR-4 材料考慮的因素

Material Considerations using RCC and FR-4 For a HDI Stackups

層 1 和層 2 與層 N 和 N-1 之間的電介質的厚度可以是非固定的環氧樹脂（例塑膠包覆銅片像 RCC）或玻纖環氧樹脂（FR-4）。用非固定環氧樹脂的一個好處是加快鐳射鑽孔的速度，孔臂光滑和除去 CAF 增長，生產能力比玻纖基板會高 3 倍。

The dielectric thickness between Layers 1/Layers 2 and Layers n/Layer n-1. can be of un-reinforced epoxy (e.g., resin coated copper foil, such as RCC) or glass-reinforced epoxy (FR-4). The one advantage of using un-reinforced epoxy is the faster speed in laser drilling, smoother hole wall and elimination of CAF growth. The throughput can be as much as 3 times higher than that which can be achieved in glass-reinforced laminates.

然而，帶有一些通孔的大板，是否選用 RCC 或玻纖環氧樹脂，在壓板之前，最好選擇用純環氧樹脂（TAITO HDI 2000 或 SAN-EI PHP 900）填充通孔，典型的壓縮電介質厚度依靠內層銅的厚度和形式是：0.0010[0.025]-0.0025[0.063]

However, on large boards with many vias, whether using RCC or glass reinforced epoxy, it is a good choice to fill the vias with pure epoxy resin (TAITO HDI 2000 or SAN-EI PHP 900) before pressing the board. The typical pressed dielectric thickness is 0.0010[0.025]-0.0025[0.063], depending on inner-layer copper weight and type.

4.3.3 類型 I，HDI 結構的典型分層　Typical Stackup for a Type I HDI Structure

在板的一邊或兩邊，分層有一個單一微型通孔和通孔通路連接外層。

This stackup has a single microvia on either one or both sides of the board and through hole vias connecting the outer layers.

4.3.4 類型 II，HDI 結構的典型分層　Typical Stackup for a type II HDI Structure

這個分層與類型 I 有同樣的結構，不同的是在板內增加了埋入式通孔結構。

This stackup has the same construction as Type I with the addition of buried vias in the board substrate.

*具有一個 0.006[0.15]的微型通路類型 II HDI 的典型結構可以在 0.062[1.60]厚的板(在銅上）上有 14 或略小的銅層。(圖 19 顯示了橫截面的詳細結構)。一個 0.012[0.30]厚的埋入式核心通孔通常的從 2 延伸 13 層，這工藝可提供板兩邊被動與主動的放置，因爲板埋入式核心有類似通孔的通路但在外層沒有集中孔。

*A typical Type II HDI Structure with a 0.006[0.15] microvia might have fourteen copper layers or less in a 0.062[1.60] thick board (over copper). (Figure 19 shows the cross section details of the construction). A 0.012[0.30] buried core via would normally extend from layer 2 through layer 13. The technology provides for the placement of both actives and passives on both sides of the board with the buried core breakout vias functioning much like through hole vias but without the vias penetration onto the outer layers.

4.3.5 典型類型 II 微型通孔標示特徵

A Typical Type II Micro-Via Roadmap Feature

Design Feature	attribute	Limits
Track Width	(0.004[0.10])nominal	(0.0035[0.09])Min
Track Gap	(0.004[0.10])nominal	
Track Gap	(0.006[0.15]at surface before plating	(0.004[0.10]at surface before plating
Buried Core Via Hole Size	(0.012[0.30]	IPC HDI Type II
Blind Via Land Size	0.006[0.15]	
Blind Via Land Size	0.016[0.40]L1,L4 0.016[0.40]L2,L3	(+0''/-0.001[0.025])finish
Buried Core Via Land Size	(0.022[0.56]	IPC HDI Type II
PCB Thickness	(0.062[1.60]+/-.007[0.18] measured over glass	

4.3.6 14 層微型通孔板典型 PCB 製作工藝

A Typical PCB Fabrication Process for a 14 layer microvia Board

典型的 PCB 結構如下描述

- 獨立地映射和刻蝕兩邊的內部核心
- 所有核心從 L3/4 到 L11/12 和薄片 L2&L13 一起連接金箔
- 從(L2/L3)鑽埋入式核心通孔
- 電鍍 L2/L3 核心通孔
- 映射和刻蝕 L2/L3
- 選擇的通孔填充
- 連續地 L1/L14 外部覆蓋金屬薄片
- 鐳射或機加鑽盲式通孔 L1/2 和 L14/13（有些僅鑽 L1/14 通孔）

- 鐳射電鍍通孔（有些通孔 via）
- 映射和刻蝕外層
- 運用錫焊和表面拋光

The typical PCB fabrication is as described by the following flow:
*Image and etch two-sided inner cores independently.
*Laminate of all cores L3/4 to L11/12 inclusive and L2&L13 capping foils together
*Drill buried "core" via hole from (L2/L3)
*Plate L2/L13 core vias
*Image and etch L2/L13
*Optional Via filling
*Sequentially laminate L1/L14 outer foils
*Laser or mechanically drill blind vias L1/2 and L14/13 (and drill any L1/14 through vias if there are any)
*Plate laser vias (and through hole vias if there are any)
*Image and etch outer layers
*Apply solder resist and surface finish

4.3.7 類型 III HDI 結構的通常微型通路間距和尺寸

General Micro-via spacing and dimensions for Type III HDI structure

類型 III 與類型 II 不同是在 PBC 基至少一面允許最少兩個微型通孔層（看圖 20） Type III differs from Type II by allowing at least two microvia layers on at least one side of a PBC substrate.(see figure 20)

4.3.8 埋入式核心通孔的 PCB 佈局特點 PCB Layout Features for Buried Core Vias:

埋入式核心通孔可能被標準的環氧樹脂填充，用 FR-4 填充之前，來防止樹脂材料脫離 FR-4 和掉到核心通孔內。任何核心通孔填充必須是 COMPLETE 和在真空壓力之下填充，至少 70%的埋入式通孔填充環氧樹脂或樹脂，不允許有化學親和

Buried Core vias may be filled with a standard acceptable epoxy before applying the FR-4, to protect the resin material from leaving the FR-4 and being lost down into the core via holes. Any via filling must be COMPLETE and under vacuum pressure filling at least 70% of the buried vias with epoxy or resin and allowing for NO chemical entrapment.

4.3.9 通孔電鍍要求 Via Plating Requirements

在多層 PCB 上埋入式核心通孔的 MCP

絕對最小值：13 微米

平均最小值：15 微米

* Minimum Copper Plate of Buried Core Vias on the multilayer PCB is:
Absolute Minimu: 13 microns
Average Minimum: 15microns

微型通孔最小銅板的厚度應該迎合下面的要求：

絕對最小值：15 微米

平均最小值：17 微米

*The minimum copper plate thickness of microvias shall meet the requirements of the following:
Absolute Minimum:15microns
Average Minimum: 17microns

4.3.10 帶有相切環孔的微型通孔的允許

Micro-Via with Tangency annular ring is permitted

鐳射通孔相切條件

* 相切條件是這樣定義的，當電鍍孔外邊與銅配圈的外邊方向一致時，銅孔的外部銅片牆是可接受的。

Tangency Condition of Laser Vias

- The tangency condition is defined such that the outside copper plated wall of the blind via is acceptable when the outer edge of the plated hole is in line with the outer edge of the copper land.

4.3.11 BGA 或 CSP 下“墊片中的微型通孔”

“Microvia-in-Pad ” under a BGA or CSP

- 參照 3.5.16 部分可得到更多的資料
- 初步研究表明，當微型通孔的中心處在 BGA 球下焊接頭的空焊機率被提高，空焊引起的原因是回流焊接過程中來至微型通孔內部釋放的空氣和焊劑，而進入 BGA 球中。一種方式是沿著 BGA 墊片周圍設定通孔中心，下圖 1 所示，第二種選擇是相切於 BGA 墊片的邊設定通孔的邊，下圖 2 所示。間隙不會隨著技術增加而減少，它也是在小間距(0.65 和 0.5mm)BGA 上無效的。如果通孔設在墊片中心，電鍍後則必須定義爲鐳射

鑽孔和鍍後填充，注：並不是所有的供應商都有這個能力，對所有的 BGA 首選的方法是在任何間距和錫球尺寸獨立的 dogbone 墊片邊界設置微型通孔。

- 微型通孔直徑定義在 0.004[0.10]-0.006[0.15]，對於大量的買方，微型通孔的墊片尺寸等於鐳射孔的直徑加 0.0085[0.22]或相切的 0.0042[0.11]環形圓。

*Refer to section 3.5.16 for further information

*Preliminary studies indicate that solder joint voids are increased when the center of a micro-via is directly under the BGA ball. The void is caused by the release of air and flux from inside the micro-via, up and into the BGA ball during the reflow soldering operation. One alternative is to place the center of the via along the circumference of the BGA pad. This is shown in option 1 below. A second alternative is to place the edge of the via tangent to the BGA pad. This is shown option 2 below. Voids are not reduced as much with this technique. It is also least effective on small pitch (0.65 and 0.5mm) BGAs. If vias are placed in the center of the pad, they must be defined as laser drilled, and fill after plating. Note: Not all fab suppliers have this capability. The preferred approached for all BGAs is to place the micro-via within the boundaries of its own individual dogbone pad at any pitch and ball size.

*Micro-vias should be defined as 0.004[0.10]-0.006[0.15] diameter. The micro-via capture pad size, for most board vendors, is equal to the laser hole diameters plus 0.0085[0.22] or an annular ring of 0.0042[0.11] for tangency.

4.4 PCB 電路設計考慮（爲 HDI 和較低技術）

PCB Electrical Design Considerations (For HDI and lower technologies)

4.4.1 功能要求 Functional Requirements

功能要求包括：阻抗、信號速度、延遲傳播、Cross-talk、信號完整、EMI（電子磁干擾），ESD 和 RF 設計。（注：對功能的補充資訊看 IPC02221，6.0 部分電學考慮和 IPC-D-317 高速設計推薦。）

Functional requirements include: Impedance,、Signal speed、Propagation delay、Cross-talk、Signal integrity、EMI(Electro-magnetic interference)、ESD(Electrostatic Discharge) and RF (Radio Frequency) Designs.
(Note: For supplement information on functional requirements see IPC-2221section 6.0 Electrical considerations and IPC-D-317 high speed design recommendations.)

4.4.2 板材原則 Board Material Guidelines

盡可能設計應該用 FR-4 的材料，因它的完好確定的性能和廣泛的加工範圍。FR-4 被

用 50 歐姆的阻抗可達到千兆赫茲，不同性能的另種材料應該在對 FR-4（最大 1G 赫茲）有限制的設計條件下被考慮，新材料所必要的是工藝公差和適用領域，如果沒有加工硬化出現元件變形，推薦用 FR-4 Tg>170 degrees C 和板厚大於 0.080[2.00]以阻止板變形。

Where possible, design should use FR-4 with its well established properties and wide manufacturing experience base. FR-4 can be used for 50 ohm impedance lines up to gigahertz frequencies. Alternative materials with different properties should only be considered when the design limits of FR-4 are reached (1Ghz max.). It is then essential with the new material, process tolerances and probable yields. If fine pitch devices are present with no mechanical stiffening, it is recommended to use FR-4 with a Tg>170 degrees C and a board thickness greater than 0.080[2.00] to prevent board warpage.

4.4.2.1 可用基本裸板材料　　Available basic bare board materials:

	Tg(C)	Degradation Temperature(C)
FR4	140multi-funtional	235
FR4/FR5	160-175 muti-functional	235
BT	180-200	265

4.4.3 導體間距要求　　Conductor Clearance Requirements

電路波峰運行電壓可能影響高電壓導體和在 PCB 板上的臨近導體之間的間距，這些電壓和相關的間距在 IPC-2221　6.0 部分顯示，導線之間的最小間距給定工作電壓看說明 IEC950。

The peak operating voltage of a circuit may influence the clearance between the high voltage conductor and adjacent conductors on the PCB. These voltages and associated clearances are shown in IPC-2221 section 6.0. For minimum clearances between traces at a given working voltage see specification IEC 950.

4.5 裸板/面板指導原則和麵板資料

Bare Board/Panel Guidelines and Panel Documentation

4.5.1 正確定出尺寸以確定檔

Dimensioning From a Datum for Proper Documentation

在板輪廓線內部選非電鍍孔作爲參考面，所有的尺寸應該參照這個面，面板也該參照這

個面。用這個面定位特徵，定義工具孔，結合鑽孔排列方式用到其他尺寸特徵，定義圖案位置和大小和裸板外廓尺寸。

Select a non-plated hole inside the board outline as a datum. All dimensions should reference this datum. The same datum should be used on all boards within the panel. Use the datum for locating features, defining tooling holes, tying drill patterns to other dimensional features, defining location and size of cut-outs and dimensioning the bare board outline.

4.5.2 面板層對稱分層 Panel Layer Stackup Symmetry

4.5.2.1 電介質間距 Dielectric spacing

優先說明銅重量相同地穿過分層，平衡電介質間距爲了在 Z 軸方向對稱，這有利於減小變形的可能性（對 HDI 設計，盲式外層微型通孔的電介質設計爲最小 0.002[0.05]厚）

It is preferred to specify the layer copper weight identically throughout the stackup. Balance the dielectric spacing so that it is symmetrical in the Z axis. This helps reduce the possibility of warpage.(For HDI designs the dielectric will be 0.002[0.05]thick minimum for the blind outer layer micro-vias.)

4.5.2.2 銅重 Copper weights:

銅重的工業標準是在內層上 1/2 oz 或 1 oz，外層是 1/2oz。然而對 0.006[0.13] 線路和 0.004[0.10]寬線路一些買方寧願在內層 1/2 oz 銅，因在保持線寬內刻蝕困難，除了買方有其要求，否則保持銅重一致的通過分層（例如：對內部信號層 1 oz 銅隱入電源層和 1 oz 銅接地層），（HDI 外層銅重應是 1/4 oz 爲鐳射鑽孔）。對於板路徑攜帶電流的能力是基於路徑的寬和厚度看 IPC-2221 專門說明 6.2 部分。

The industrial standard for copper weight is 1/2 oz or 1 oz. on the inner layers and 1/2 oz. for the outer layers. However, for 0.006[0.13] traces and 0.004[0.10] wide traces some board vendors prefer 1/2 oz. copper on the inner layers because of the etching difficulties in holding the trace width. Unless instructed by the board vendor to do otherwise, keep the copper weights the same thoughtout the stackup (i.e., 1 oz. buried power and ground with 1 oz. copper for inner signal layers). (HDI outer layer copper weights will be 1/4 oz. copper for lazer drilling.) For current carrying capacity of board tracks based on track width and thickness see IPC-2221 specifications section 6.2.

Ounces per sq.ft	um
1/8	5
1/4	9
1/2	18

1	

Figure22-Copper Foil Thickness Conversion Table

4.5.3 板設計相關因素 Board design Considerations

除了每條線攜帶電流的能力和電子性能被考慮之外，控制電特性要求較低元件公差，板材料，路徑設置和控制板阻抗的板結構的混合。

Besides the current carrying capacity of each track, the electrical characteristic of each track must be considered. Controlling electrical characteristics require a blending of lower component tolerances, board material, track placement and board construction to control the board's impedance.

4.5.4 說明每片板或面板受控阻抗

Specifying Controlled impedance on each board or panel

當設計受控阻抗板時，指定板整體光面厚度，材料，公差，分層和在每層板的要求阻值資料，不要求指定最終路徑寬度和電介質厚度因爲製造者在每塊板上將做 TDR 測試以確保符合要求。

When designing controlled impedance boards, specify the board overall finished thickness, material, tolerance, the layer stackup, and the impedance value required in ohms for each layer in the board's documents. It is not required to specify finished trace widths and dielectric thickness because the fabricator will do the TDR tests on each board to ensure compliance.

4.5.4.1 受控阻抗阻礙 Controlled impedance containment

帶有高速信號、EMI 的設計根據常規的阻礙手段是很難控制的，三明治式 BC 材料勝於標準的基板材料，在通過板電源與接地層之間提供充足的實際退耦。

Designs with high speed signals、emissions (EMI) are difficult to control by conventional containment methods. Sandwiching buried capacitance(BC) material, rather than the standard laminate, between ground and power layers will provide much more substantial decoupling between both power and ground layers throughout the board.

4.5.4.2 埋入式電容的技術可行性 Buried Capacitance Technology Feasibility

埋入式電容通過傳遞和其他功能也能很有效的用於代替大量離散的低值陶瓷晶片來退耦。從經濟價值可行性考慮至少 40%的電容需要被代替，移去第二面的表面貼裝電容將爲板提供附加的空間，減少通孔和提供從雙面裝配到單面回流焊裝配可能性轉換。

BC 基板通常 0.002[0.05] 厚，花費和要求感應係數減小這將決定植入電容的類型材料，

埋入式電容材料內部容量範圍從 0.5 to 50pf/square inch ，聯繫當地的埋入式電容材料

“3M, Hadco (now Sanmina), and Dupont”買方以獲得更多的資料。

“Buried Capacitance’ can also be used very effectively to replace large numbers of discrete low value ceramic chip capacitors used to decoupling, by-pass and other functions. At least 40% of these capacitors need to be replaced to make the technology economically feasible. Removal of secondary side surface mount capacitors will provide additional board space, eliminate vias and provide the possible conversion from a double-sided assembly to a single sided reflow assembly. BC laminate is usually 0.002[0.05] thick. Cost and required inductance reduction will determine the type of embedded capacitance to use. Buried Capacitance material has an internal capacitance ranging from 0.5 to 50pf/square inch. Contact your local vendor of buried capacitance material “3M, Hadco (now Sanmina), and Dupont” for further information.

注：對其他的面板結構資料看機加指導原則部分 2.3 面板結構設計和 IPC-221, IPC-2141

and IPC-D-317，這些定義了受控電阻的基本理論。

Note: “For additional Panel fabrication information see the manufacturability Guideline section 2.3 design for panel fabrication” and IPC-221, IPC-2141 and IPC-D-317 which defines the basic theory of controlled impedance.

4.6 孔與槽 Hole and Slot

4.6.1 簡介 Introduction

裸板要求安裝通孔元件、其他元件機械連接板和附加支架、印刷電路支架和測試點固定

的孔和槽，這部分提供電鍍/非電鍍孔和槽類型的考慮，指導和公差，這些對設計者是

很有效的。

Bare boards require holes and slots for the installation of the though hole components, bracket attachments, mechanical connections to the board for other components, installation of the print circuit board to its housing, and test points. This section provides considerations, guidance and tolerances for the various types of plated/non-plated holes and slots available to the designer.

4.6.2 板厚所對應之縱橫比率 Aspect Ratio vs. Board Thickness

默認孔的縱橫比率是：PCB 厚度被最小名義孔尺寸相除，典型的是 7-8:1。一些供應商

能達到 10：1 的縱橫比率，12-18 到 1 的縱橫比率或較大要求就要與製造者討論和增加

額外的費用。

The default hole aspect ratio, which is the PCB thickness divided by the minimum nominal hole size, is typically 7-8:1. A hole aspect ratio of 10:1 is achievable by some suppliers. Aspect ratio of 12-18 to 1 or greater require review with the fabricator and an expectation of additional costs.

4.6.3 層數所對應之板厚 Board Thickness vs. Layers

PCB 厚度有時被一些公司在光基板上測量，或其他的在板上測量兩者都是公差±10% 。

在標準 PCB 技術，最小電介質間距的設計是 0.004[0.10]，受控電阻的需要，在給定厚度的情況下，會降低達到的最大層數，這是由於特定的電介質間距的需要，可參照下表。

PCB thickness is measured over bare laminate by some companies or over the board finish by others, both with ±10% tolerance. Minimum design dielectric spacing is 0.004[0.10] on standard PCB technologies. Controlled impedance requirements may reduce the maximum layer count achievable within a given thickness, due to specific dielectric spacing requirements. For approximate achievable layer within a given thickness reference table below:

Board thickness vs.layers			
Aspect ratio	Min.FHS	Max.Bd.Thk	Max.layers
8:1	0.008[0.20]	0.065[1.65]	12
7:1	0.013[0.33]	0.097[2.45]	18
7:1	0.018[0.45]	0.130[3.30]	24
7:1	0.025[0.65]	0.170[4.30]	30

4.6.4 電鍍孔 Plated Holes

銑孔直徑的大小範圍是 0.002-0.003[0.05-0.08] 0.002-0.003[0.05-0.08]，比名義上的孔尺寸大，爲了允許在電鍍期間孔尺寸要變小。

公差作爲標準闡述例如：

- +/-0.003[0.08]是標準鑽孔位置公差
- +0.003[0.08]/-0.002f[0.05]最小直徑公差

Holes are typically drilled 0.002-0.003[0.05-0.08] larger than the nominal hole size to allow for hole size reduction during plating process.

Tolerances should be specified as standard, whenever possible. Examples:

- +/-0.003[0.08] is the standard drill location tolerance
- +0.003[0.08]/-0.002f[0.05] minimum diameter tolerance

不要把電鍍或非電鍍孔邊設在比 0.015[0.38]近的刻蝕特徵，電鍍不良和銅的移入易引起短路。

Do not locate hole edges, plated or non-plated, closer than 0.015[0.38] to etched features. Mis-registration, poor plating solutions and copper migration can cause shorts.

4.6.5 通用孔的鑽孔和檔指導原則 General Hole Drilling and documentation Guidelines

* 在製造工藝圖上，計算和編輯所有孔和孔的尺寸和指明是否一些能隨意電鍍
* 參照基準孔定所有孔的尺寸
* 在通孔上，檢查和刪除雙倍採樣數
* 在鑽孔圖內，直徑大小 0.002[0.05] 內合併孔
* 在通孔〈0.018[0.45]不要闡述孔尺寸大小，而是選擇下面的：
    * 闡述鑽孔尺寸
    * 沒有最小孔尺寸允許闡述最大孔尺寸
    * 允許板買方選擇鑽孔尺寸以迎合內環要求。看這段中縱橫比率部分
    * 在熱空氣平行運行期間，允許焊劑塞入孔

* Count and document all holes and hole sizes on the fabrication drawing and indicate if any can be optionally plated.
*Reference all dimensioned holes to the primary datum hole.
*Check and remove double hits on vias
*Combine hole sizes that are within 0.002[0.05] diameter from each other in the drill graphics
*Do not specify hole size on vias<0.018[0.45]. Rather, choose one of the following:
    *Specify the drilled hole size
    *Specify maximum hole size allowed with no minimum hole size.
    *Permit the board vendor to select drill size to meet annular ring requirement. See Aspect Ratio section in this section.
    *Permit plugging of hole with solder during hot air level operation.

4.6.6 電鍍與非電鍍槽 Plated and Non-plated slots

電鍍槽是典型的額外花費，鑽孔工藝和數控機床能生產槽。

- 尺寸公差：長和寬保持在+/-0.005[0.13]
- 位置公差：保持在+/-0.005[0.13]

- 槽長應該是最小兩倍槽寬+0.001[0.025]

Plated Slots will typically be at a premium cost. At drilling sequence or numerically controlled machining can produce them.

- Size tolerance: Length and Width maintains+/-0.005[0.13]
- Position tolerance :Maintains+/-0.005[0.13]
- Slot length should be a minimum of twice the slot width+0.001[0.025]

4.6.7 非電鍍通孔 Non-Plated Through Holes

大於 0.25[6.35]直徑非電鍍孔在側面加工過程中產生，尺寸公差和位置公差是：

- 鑽頭尺寸公差：+/-0.005[0.13]
- 位置公差：+/-0.005[0.13]

Non-Plated holes>0.25[6.35] diameter are produced during the profile routing sequence. The size tolerance and position tolerance is:

- Drill size tolerance:+/-0.005[0.13]
- Position tolerance: +/-0.005[0.13]

保持所有刻蝕特徵 0.015[0.38]遠離所有的鑽孔，提高 0.025[0.65]給孔邊來導電以確保孔固定或壓力適中。

Keep all etched features 0.015[0.38] away from all NPTH drilled holes. Increase to 0.025[0.65] for edge of hole to conductor for holes securing riveted or press-fitting hardware.

4.7 內外層設計要求 Inner and Outer Layer Design Requirements

4.7.1 簡介 Introduction

這部分闡述間距，最小預留量，外形，尺寸和特徵爲內層和外層印刷電路考慮的問題。

This section addresses spacing, clearances, shapes, dimensions and attribute considerations for the inner and outer layers of a printed circuit board.

4.7.2 內層的通用規則 General rules for both inner and outer layers

* 所有內外信號層都應該平衡銅或 thieving 分配，知道所用的銅墊片直徑大小 0.056[1.4] 在 0.100[2.5] pitch 上 和 0.050[1.25] pitch 在 0.030[0.75]平方英寸墊片上。每 1.0 平方英寸中 1/10 平方英寸開路從下部出來到 x-ray 鐳射在表面側壓期間能撞擊板。在 SMD 晶片下或電子敏感元件和標籤區是不允許 Thieving。

* 每個平面的分隔層和信號層在板分層中描述和層號位置清晰地被標示。

* 通常，墊片到線連接應該被分開以提高相互連接的可行性，推薦如下：當墊片直徑減掉鑽頭尺寸的值小於 0.015[0.38]，線路應該保持分開。

* 間隔所有內部銅迴圈線路不少於 0.025[0.65]。

* All inner and outer signal layers shall have balanced copper or thieving distribution. Known copper pad sizes used is 0.056[1.4] in diameter on a 0.100[2.5] pitch and 0.030[0.75] square pad on a 0.050[1.25] pitch. A 1/10 square inch opening every 1.0 square inch out from under parts to the x-ray laser can strike the board during surface profiling. Thieving is not permitted under SMD chips or electrically sensitive devices and in areas for labels
* The artwork layer for each plane and signal layer be clearly labeled as to its description and layer number position in the board stackup.
* In general, a pad to trace connection should be tear-dropped to increase the interconnect reliability. It is recommended that when the pad diameter minus the drilled hole size is less than 0.015[0.38], the trace should contain a teardrop.
* Space all internal copper from route paths by at least 0.025[0.65].

4.7.2.1 電源塊的電源/接地連接 pad （電流不小於 20 安培）

Power/Ground Connection pad for power bricks (for less than 20 amps)

* 注：電源連接器不要超過 4 個平面應用高溫連接，兩個靠近板底部和兩個靠近板的上部分層。如果可能在通常墊片中用多角 pin 分流進入合適的平面。

* Note: Power connectors must not have more than 4 planes connected using thermals. Two near the bottom and two near the top of the board stackup. When possible use multiple pins in a common pad with current distribution vias into the appropriate plane.

* 外層表面墊片設計

    * 用 0.025[0.63]最小值環孔，外層墊片直接連接到 pin 孔。

* 內層熱墊片設計

    * 熱墊片應該被加入焊劑 PTH 元件連接到電源和地平面，最多四個平面能被連接到任何一個錫焊 pin，在板的上部兩個和兩個靠近錫焊邊，連接墊片到地和電源面被一個內部和外部直徑所指定。

        * 內部直徑是鑽頭加 0.022[0.55]

        * 如果孔直徑小於 0.100[2.50]，內部直徑要比外部直徑大 0.020[0.50]

        * 如果孔直徑是或大於 0.100[2.50]，外部直徑比內部直徑大 0.030[0.80]

* 對於元件禁止上面的熱傳到板上例如 DC/DC 轉換和連接器，每個錫焊 pin 要求最多四個平面必須有最小 0.012[0.30]給孔直徑允許間距和外部墊片容易產生熱傳到孔壁，不用固體平面連接，在大的表面墊片內用電流分流連接通孔和提供反墊片允許間隙大於四個平面。

*Surface pad design on outer layers:

*Outer pads are directly connected to the pin hole with a 0.025[0.63] minimum annular ring.

* Thermal pad design on inner layers

* Thermal pads should be added to all soldered PTH device connections to the power and ground planes. A maximum of four planes can be connected to any one soldered pin. Two at the top of the board and two near the solder side. Connection pads to ground and power planes are specified by an inner and outer diameter.
    * The inner diameter is the drill size plus 0.022[0.55]
    * The outside diameter is 0.020[0.50] larger than inside diameter if the hole is less than 0.100[2.50] in diameter..
    * The outside diameter is 0.030[0.80] larger than the inside diameter if the hole is 0.100[2.50] in diameter or greater.

* For devices prohibiting topside heat onto the board such as DC/DC converters and connectors, a maximum of four internal planes per soldered pin is required. There must be a minimum of 0.012[0.30] lead to hole diameter clearance and large external pads to facilitate heat transferring up the hole's barrel. Do not use solid plane connections. Use current distribution direct connect vias in the large surface pads and provide anti-pad clearances to more than four planes.

* 當每個 pin 電流超過 4 安培，電源 pin 連接僅一個平面，推薦用分流墊片和通孔。

*For power pins connecting to only 1 plane, current distribution pads and vias are recommended when current exceeds 4 amps per pin.

4.7.2.2 電源塊的電源/接地連接 pad（超過 20 安培）

Power/Ground Connection pad for power bricks (for more than 20 amps)

* 外層表面墊片設計

* 表面銅墊片

* Surface pad design on outer layers:

在板上面和下面的表面銅墊片應該保持足夠大均勻的間距 0.023[0.58] FHSvias ，通孔在 soldermask 內有最小 0.010[0.25]開放圓環。通孔直接地連接

兩個外層加所有分別的內層連接，就必要有足夠的分流通孔來攜帶傳輸電流塊，每個通孔傳輸假設 3 安培電流和每個表面分流墊片傳輸 10 安培電流，當分流超過了表面墊片的限制就 要增加額外的表面型墊片，被一些面所隔離，熱能被加到內層和連接到孔壁，像下面的闡述，內部分流墊片攜帶電流能力減小，由於熱連接到 pin 孔壁，像表面墊片攜帶同樣的電流需要兩倍數量的內部墊片（看下圖）

The surface copper pads on both the top and bottom of the board should be large enough to contain evenly spaced0.023[0.58] FHSvias. These vias are to have a 0.010[0.25] minimum annular ring opening in the soldermask. The vias are to be directly connected to both of the outer layers plus all respective internal plane connections. There needs to be enough distribution vias to carry all the current the brick will deliver. Assume 3 amps per distribution via and 10 amps per surface distribution pad. When the current distribution exceeds the surface pad limits additional surface type pads, isolated from any planes, can be added to the inner layers and connected to the hole barrel with thermals, as described below. The internal distribution pad current carrying capacity is reduced due to the thermal connection to the pin hole wall. Use twice as many internal distribution pads to carry the same current as the surface pads.(see below)

* 內層熱墊片設計 Thermal pad design on inside layers

* 墊片內部直徑是鑽孔直徑加 0.050[1.27]

* 如果孔的直徑是或大於 0.100[2.50]，外孔直徑比內孔直徑大 0.030[0.76] 就可產生熱量突變。

  * 以 90 度分開四段

  * 孔的每段寬度-0.020[0.50]要小於 0.100[2.50]（20 安培）

    * 孔的每段寬度-0.030[0.76]要等於或大於 0.100[2.50](>30 到 60 安培)

    * 每段角度-45

    * 最多四個內部平面優先連接板下部的兩個和上部兩個分層，所有其他的平面應該有反向墊片和不連接到平面

* The pad inner diameter is the drill diameter of the hole plus 0.050[1.27].

* The outside diameter creating the thermal break is 0.030[0.76] larger in diameter than the inside diameter if the hole is 0.100[2.50] in diameter or greater.
* Number of spokes-4 at 90degrees apart
* Width of spokes-0.020[0.50] for holes less than 0.100[2.50] (20amps)
* Width of spokes-0.030[0.76] for holes equal or greater than 0.100[2.50](>30 to 60 amps)
* Angle of the spokes -45
* A maximum of 4 internal planes can be connected. Preferably two at the bottom and 2 at the top of the board stackup. All other planes should have anti-pads and not connected to the planes.

與熱連接的平面，最多連接四個平面，優先考慮板下面的兩個平面和上面的 2 個平面分層，所有其他平面應該有反向的墊片和不連接到平面

Plane connections with thermals， Max of 4 planes can be connected. Preferably two at the bottom and 2 at the top of the board stackup. All other planes should have anti-pads and not connected to the planes.

- 電源連接器和電壓符合高電流連接設計

Power connector and Voltage regulator high current connection design.

* 墊片的內部直徑是鑽頭直徑加 0.050[1.27]，電流連接應該被包含在同一個墊片內，分流通路應該設置在 pin 區域周圍和直接連接到同個網路的內部平面，這些分流通路應該盡可能同樣大,在錫焊區內有一個圓環以利於錫填充。連接器應該有它的 pin 連接於 0.015[0.38]寬的四段熱和一個內部，外部熱間斷直徑適合於 pin pitch，儘量僅 2 個內部平面被連接到板的錫焊邊附近。
* The pad inner diameter is the drill diameter of the hole plus 0.050[1.27] current connection should all be contained in the same pad. Current distribution vias should be placed in the areas around the pins and directly connected to the internal planes of the same net. These current distribution vias should be as large as possible and have a 0.010[0.25] annular ring in the soldermask to facilitate solder fill. The connector should have its pins connected with 4 spokes thermals 0.015[0.38] wide and an internal and external thermal break diameter appropriate to the pin pitch. It is preferred that only 2 internal planes be connected near the solder side of the board.

4.7.3 內層通則 General rules for Inner Layers

* 在所有面上，地和電源面圍繞非電鍍通孔的 FHS 的允許間距應是 0.015[0.38]
* 在內層上線路圍繞鍵槽和 NPT 孔的允許間距應定位，從一些樣圖或爲硬體貼裝非電

鍍通孔邊或機加孔邊大於 0.025[0.65]。壓緊應該有 0.100[2.54]或更多的特徵餘量來避免與內部工件短路。

*圍繞光板的周界的線路在所有信號層.地層或電源層上允許間距必須等於或大於 0.025[0.65。]

* 最小直徑墊片應比鑽孔尺寸大 0.014[0.35]或比光名義孔大 0.019[0.48]。

* 所有內層 Gerber data 必須有正極

* 小於 0.008[0.20]的特徵是不被允許的

*The ground and power plane clearance around the FHS of non-plated through holes shall be 0.015[0.38] on all layers.
* Routing clearance on inner layers around keyslots and NPT holes shall be located no closer than 0.025[0.65] from the edge of any cut-out or keyslot or the edge of a non-plated –through-hole used for hardware mounting or manufacturing hole. Press in fasteners should have 0.100[2.54] or more feature clearance to avoid shorting to internal features.
* Routing clearance around the perimeter of finished board must be equal to or greater than0.025[0.65] on all internal signal layers, ground layers and power layers.
* Minimum diameter pad should be 0.014[0.35] larger than drilled hole size or 0.019[0.48] larger than finished nominal hole size.
*Gerber data for inner layers must have a positive polarity.
*No feature smaller than 0.008[0.20] square is allowed.

除非製造商要求通孔壁支持，可隨意移去所有非功能墊片（通常在高層數板上），如果通常的墊片不被移去，確保保持所有反向墊片允許間距。

Optional-Remove all non-functional pads unless the fabricator requires via barrel support (usually on high layer count boards). Insure all antipad clearance are maintained if the unused pads are not removed.

4.7.4 外層通則 General Rules For Outer Layers

* 用不同的尺寸墊片給通孔和測試點，這增加了外觀和板的視覺上的辨別力

* 外層 Gerber data 必須是正極

* 從板邊保持平面和線路 0.025[0.635]的最小值

* 保持至少 0.015[0.38]的來至鑽頭的刻蝕

* 圍繞通孔元件件 pin，獲得 0.001[0.025]最小值圓環，墊片必須比鑽孔尺寸大 0.014[0.35] 或比光的名義孔尺寸大 0.019[0.48]

* 盡可能使用圓形墊片

* 爲平衡電鍍，保持銅上和下 10%平方英寸內變動，以避免在外層上的不平衡設計因爲獨立的線路或孔不能按說明來電鍍

* 避免外層上設地平面，除了電路要求外

*盡力避免在外層設置最複雜的線路，fine 線路和稠密的電路用內層或信號層

* 保持墊片邊超過金手指邊最少 0.050[1.25]，或允許在手指寬度上面的 soldermask 值是 0.050[1.25]，以阻止 PCB 佈線期間翹起

* 金邊連接器和逃逸標號之間的最小距離是 0.025[0.65]，從指到通孔保持值 0.050[1.25]

* 在 PBC 的原始面上外部連接器不能設在導體的下面（例晶振，感測器等），除了 PCB 表面元件被提高最小值 0.010[0.25]，或電介質。

* Use different sized pads for vias and test points. This enhances visual discrimination of artwork and board.
* Outer layer Gerber data must have a positive polarity.
* Keep planes and traces a minimum of 0.025[0.635] from the edge of the board.
* Keep all etched features at least 0.015[0.38] from all drilled holes.
* To achieve a 0.001[0.025] annular ring minimum around through hole device pins, pads must be 0.014[0.35] larger than the drilled hole size or 0.019[0.48] larger than finished nominal hole size.
* Use round pads wherever possible.
* For balanced plating distribution, keep the top and bottom square inches of copper within 10 percent of each other. Avoid unbalanced design on the outer layers because solitary traces and holes may not plate to specification.
*Avoid ground planes on outer layers, unless required for electrical performance purposes.
* Strive to keep the most complex circuit routing off the outer layer, use the inner layer signal layers for fine-line and dense routing.
* Keep all pad edges at least 0.050[1.25] above the gold fingers, or allow for soldermask on the top of the finger width is 0.009[0.23] to prevent lifting during PCB edge routing.
* Minimum space between gold edge connector and breakaway tab is 0.025[0.65]. Maintain 0.050[1.25] from fingers to vias.
* External conductors should not be placed under conductive body components (e.g., crystal, transformer) on the primary side of the PCB, unless the component (including

non-insulated straps) is elevated from the surface of the PCB by a minimum of 0.010[0.25] or unless insulted washed are used.

* 爲一個 PTH 孔外部區域周圍一些電子連接器件尺寸大小是器件直徑 +0.120[3.00]

* 留一個開放區域給買方貼日期代碼，ID 和 UL 圖示，建議尺寸大小是 0.200[5.00]x0.400[10.00]

* External land size for a PTH hole around an electrically connected hardware is the hardware diameter+0.120[3.00].

* Leave an open area for vendor date code, ID and UL logo. Suggested size is 0.200[5.00]x0.400[10.00].

4.8 經孔與墊片電鍍 Plated via Hole and Pads

4.8.1 簡介 Introduction

通孔用來相互連接配圈墊片到其他層和測試點。

Vias are used for interconnection of land pads to other layers and test nodes.

4.8.2 測試節點通路 Vias for test nodes

測試點尺寸和間距看測試 2.6 部分

See testing section 2.6 for acceptable test point size and spacing.

4.8.3 通孔佈置原則 Via Placement Guidelines

* 通孔在 SMT 回流焊配圈墊片中是不允許有的，通孔必須與配圈墊片分開用線連接。

盲式微型通孔在間距大或均勻的回流焊墊片中可使用，它們不能直接地放在大間距或 BGA 球下，看 3.5.15 部分 BGA 墊片中微型通孔。

* Through hole vias are not permitted in the SMT reflow land pad. Vias must be separated from the pad and connected by a trace. Blind micro-vias are permitted in leaded or discreet reflow pads. They must not be placed directly under leads or BGA balls. See 3.5.15 for microvias in BGA pads.

* 通孔與晶片墊片之間銅與銅最小間距是基於兩個連接和暴露錫焊表面之間的 0.005[0.13]環內，不管通孔和墊片尺寸，這個間距必須計算得值符合最小錫焊環要求。

一種方法是允許通孔移近晶片墊片是通過侵蝕錫焊邊界，這樣的侵蝕使 soldermask 覆蓋超過了通孔但保持通孔內清潔。最小的通孔允許間距是 0.004[0.10]和優先選擇的直徑是 0.006[0.15]，比通孔 FHS 大。下面是舉例用優先選擇 FHS 直徑 0.006[0.15]開路

連同晶片墊片 0.003[0.08]soldermask 開路，產生通孔侵蝕。“銅到銅最小間距”顯示在下面圖表中，通孔墊片和晶片提供了最小 0.005[0.13]或大些的 soldermask 壩。注意間距在晶片邊上比直接在末端大，這是因爲在設置和回流焊工藝期間，晶片在墊片上的移動，所有通孔要求最小 0.0055[0.14]圓環或一個 0.011[0.28]銅墊片比 FHS 通孔大。

* The smallest copper to copper spacing allowed between a via and chip pad is based on a 0.005[0.13] solder web between the two connected and exposed solder surfaces. Regardless of the via hole and pad size the spacing must be calculated to adhere to the minimum solder web requirement. One way to allow the via to move closer to the chip pad is to encroach the via with soldermask. The encroachment provides soldermask coverage over the via pad but keeps the via hole clear. The minimum via hole clearance is a 0.004[0.10] and the preferred is 0.006[0.15] diameter, greater than the via FHS. The chart below is an example of providing via encroachment using the preferred 0.006[0.15] diameter opening around the FHS along with a 0.003[0.08] soldermask opening around the chip pad. The “copper to copper minimum spacing” shown in the chart below between the via pad and chip pad provides for a minimum soldermask dam of 0.005[0.13] or greater.

Unconnected and Connected encroached Via to Chip Pad Copper Spacing (Reflow process)

Chip package	Spacing Y minimum	Spacing Y Preferred	Spacing X minimum	Spacing X Preferred
04020-0603	0.010[0.25]	0.015[0.38]	0.006[0.15]	0.009[0.23]
All others	0.015[0.38]	0.020[0.50]	0.006[0.15]	0.009[0.23]

Note that the spacing is greater on the sides of the chip than directly on the ends. This is to allow for possible movement of the chip on the pads during the placement and refllow process. All vias require an annular ring minimum of 0.0055[0.14] or a copper pad 0.011[0.28] greater in diameter than the via FHS.

* 通路空不允許設在分立元件下（晶片阻抗，晶片電容，鉭質電容，震盪器，開關等），或直接貼裝元件（開關，金屬盒零件等）

* Vias are not allowed under discrete components(chip resistors, chip capacitors, tantalum capacitors, oscillators, switches, etc.), or flush mounted components (switches, metal can devices, etc)

* 應用一些通路孔和小於推薦值的墊片前檢查 PCB 生產能力

* Check the PCB manufacture’s capability before using any via holes and pads smaller than those recommended.

*直接設在 BGA 下同一面所有非測試墊片逃逸通孔，應有 soldermask 侵蝕但不是進入通路孔，soldermask 比完成孔的直徑大 0.006[0.15]，但能改變要依靠板拋光和板買方的

能力

* All non-test pad breakout vias located on the same side directly under a BGA should have solder mask encroachment up to but NOT entering the via hole. The mask opening should be 0.006[0.15] larger than the finished via hole diameter but could change depending on the board finish and the board vendor's capability.

* 一些通孔被用作測試點就必須在測試點能接觸到的表面有 soldermask

* Any vias that are to be used as test points must have open solder mask on the test point access surface.

4.9 電鍍相關因素 Plating Considerations

* 板上佈線方式主要影響面板電鍍的方式，線路應在元件和錫焊面平滑地分配（在 10% 內）

* The layout of the circuitry on the board has a major influence on the way the panel actually plates. Circuitry should be distributed on the component and solder sides evenly (within 10%).

* 電鍍分配影響孔的尺寸，分離孔將被超出電鍍和可能導致拋光孔的尺寸低於規格

* Plating distribution affects hole sizes. Isolated holes will be overplated and may result in finished hole size below specifications.

*分離線需要被"robbed" 或 "thieved"以達到電鍍分配，用 0.030[0.80] 方形在中心 0.050[1.25]或 0.056[1.40]圓形在圓 0.100[2.50]留下 1/10 平方英寸/每平方英寸作爲清除餘量。

*Isolate traces need to be "robbed" or "thieved" to level out plating distribution. Use 0.030[0.80] squares on 0.050[1.25] centers or 0.056[1.40] round on 0.100[2.50] centers leaving 1/10 square inches clear every square inch.

* 典型的銅電鍍規格要求最小平均值 0.001[0.025]，單面不小於 0.0008[0.02]

* Typical copper plating specifications call out a 0.001[0.025] minimum average with no single reading less than 0.0008[0.02].

* 對於 SMOBC、HASL、所有 SMT 墊片和孔厚度將從 50-1500 微米範圍內變化

* For SMOBC, HASL solder thickness for all SMT pads and holes will range between 50-1500 microns.

4.10 絲網印刷圖例 Silkscreen Legend

4.10.1 簡介 Introduction

絲網印刷圖案通常用來確定下面：

- 元件類型
- 元件位置
- 元件方位

Silkscreen artwork should generally be used to identify:

- Component type
- Component location
- Component orientation

4.10.2 絲網印刷原則 Silkscreen Guidelines

* 絲網印刷商標用來確認指定者和板上所有元件的正確方位，如果圖案清晰和包有soldermask，也可用銅來確認這些特點

* Silkscreen legend should be used to identify the reference designator and correct orientation of all devices on the board. An alternative is to use copper to identify these same issues is acceptable if legible and covered with solder mask.

* 所有元件的參照指定者應盡可能靠近元件設置，如果板的空間不允許這樣放就要從元件附近引出一箭頭線來標。

* The reference designator of all components should be placed as close as possible to the component. If board space is not available near the device run a lead line from the text to the device.

* 參照制定者應在板的正面定位（盡可能）

* The reference designators should be oriented (whenever possible) reading right side up.

* 絲網印刷不要靠近超過任何墊片，通孔或測試點 0.006[0.15]

* The silkscreen shall no closer than 0.006[0.15] to any pads, vias or test points.

* 對 fine pitch（0.020[0.50] 和更小）和 BGA/CSP （0.031 [0.80] 和更小），絲網印刷應從零元件墊片放最小值 0.020[0.5]，這包括名稱，方位標記，pin 號碼標記。確保臨近元件標記不侵犯這個允許間距，如果太靠近這些墊片，絲網印刷的厚度能影響錫焊質量。

* For fine pitch devices (0.020[0.50] and less) and BGA /CSPs （0.031 [0.80] pitch and

less）， silkscreen should be placed a minimum of 0.020[0.5] from a device pad. This includes names, orientation marks, and pin number marks. Ensure markings for adjacent components do not encroach on this clearance. The thickness of the silkscreen can affect the solder screening process quality if it is placed too close to the pads.

* 圖示的標準特徵高爲 0.045[1.15] 在 0.005[0.13] 厚，最小特徵間距值和最小線寬應 0.008[0.20 以保持可辯性（參照下表可得相關的文字高和寬）

* The standard character height for legend is 0.045[1.15] at 0.005[0.13] thick Minimum character spacing and minimum line width should be 0.008[0.20] to maintain legibility. (Reference chart below for text height to width relationship).

* 表面貼裝板用一個底部絲網印刷來顯示下面元件略圖的指定者，底部絲網印刷應放在能讀到的地方。

Height	Width
100	11
90	10
80	9
70	8
60	7
50	6

* A bottom silkscreen will be used for surface mount boards showing the outline of the bottom side parts with their reference designators. The bottom silk-screen should be orientated to be right reading.

* 絲網印刷圖案不允許在表面貼裝配圈上，它將在製作過程中掉下來，特別指出不許把指定者和定位圖示放在銅墊片上

* Silkscreen legend is not allowed on surface mount lands. It will be removed during the fabrication process. Specifically ensure reference designators and orientation marks are not on copper pads.

*只要提供完整的資料，絲網印刷應被減到最小值，例如，它不必提供一個完整的 IC 包裝外廓或晶片圖，壓縮雙線標號每個客戶要求的密度板上允許指明極性，元件值和方位

* Silkscreen usage should be minimized as long as complete information is provided. For example, it is not necessary to provide a complete outline of an IC package or a chip. Abbreviated double line marking is permitted to indicate polarity, device value and orientation on very dense boards per customer requirements.

*應該用連續 pin 標號，不要在元件實體下放標號

* A consistent pin mark should be used. The preferred mark is placed. Do not place marking

under the component body.

* 在第二面，對於大元件的 pin 號碼或局部標示可以幫助糾錯

*Pin numbers or tic marks for large devices on the secondary side may be added to aid in debug.

* 爲所有 BGA 要求有行和列設計

* Row and column designation required for all BGAs.

4.10.3. 分立元件指定者 Discrete component designators

分立元件標號應該開始於 PCB 板的左上角

Discrete components should be numbered sequentially starting the upper left corner of the PCB

The following prefixes are typically used for discretes

COMPONENT	DESIGNATOR
Capacitor	C
Resister	R
Resister Network	RN
Diode	CR
Inductor	L
LED	DS
Transistor	Q
Jumper	JP
Connector(Male)	P
Connector(Female)	J

4.10.4. 測試點辨認 Test Point Identification

在絲網印刷上測試點不需要被標號或顯示

Test points do not need to be numbered or shown on the silk screen..

4.10.5 Pin 1 指定者 Pin 1 Designator

* Pin 1 通孔元件在所有層和絲網印刷上顯示一個方形

*所有活動的 SMT 元件 Pin 1 將在絲網印刷上設計

*Pin 1 for through-hole components will be shown with a square pad on all layers and on the silk screen.

* Pin 1 for all active SMT components will be designated on the silk screen.

4.10.6 極性元件 Polarized Components

*所有極性元件的正極是 Pin 1，正極在絲網印刷上設計成+標號

* The positive lead of all polarized components will be pin 1. The positive lead will be designated with a + sign on the silk-screen.

* 在絲網印刷上二極體的方位將顯示二極體的特徵或陽極/陰極標示

* The orientation of diodes will be shown with a diodes symbol or anode/cathode marking on the silk-screen.

* 所有相似裝配的元件像電容應該有相同的極性方位

* All similar looking hand assembled components like electrolytic caps should have the same polarity orientation.

4.10.7 板面確認 Board Identification

在元件邊標示出每片板，下麵是優先標示

Each board will be marked on the component side, preferably in the silk screen with the following:

- 裝配板零件數和版本
- 在板的不用區，錫焊刻蝕層應顯示板的商標，UL 代碼和周代碼
- 板的零件數和版本號應在刻蝕層的底部顯示
- Board assembly part number and revision
- The solder etch layer shall display the logo of the board shop, UL code and a weekly date code in an unused area of the board.
- The board part number and revision shall be displayed on the bottom side etch layer

4.10.8 佈線圖確認 Artwork Identification

每層佈線圖都將標示板的零件號，版本號和層號，這個標示也該在板的工作區外

Each layer of the artwork will be marked with the board part number, revision and layer # of the artwork. The marking shall be outside the board working area.

4.11 加工圖 Fabrication Drawing

4.11.1 尺寸標注 Dimensions

對於完成板的結構圖應該有公差的尺寸標注

The fabrication drawing shall show a dimensioned drawing with required tolerances for the finished board.

- 外廓的標準公差在技術要求中指出看 4.2.1 部分
- 靠最近的 0，0 參考面的尺寸應該參照 0，0 爲參考工具孔，所有其他邊分成兩邊來標

注，所有外部工具孔應以 0，0 參考工具孔來標注

- 板上的每個孔用獨特的特徵或字母標明孔的尺寸，圖例應該包含孔直徑和相關公差的特徵，也指明是否孔爲電鍍或非電鍍，要有圖案和鍵槽的位置與尺寸
- 結構圖應沿著整個板厚度顯示所要求的分層
- The standard tolerance for the outline is shown in the technology roadmap section 4.2.1
- The dimensions to the edges nearest the 0,0 Datum shall be referenced to the 0,0 Datum tooling hole. All of the other edges shall be dimensioned from those two edges. All of the other tooling holes shall be dimensioned to the 0,0 Datum tooling hole.
- Each hole on the board shall be indicated with a unique symbol or letter for each hole size. Legend should coordinate each symbol with the hole diameter and associated tolerance. Also indicate if the hole is plated or non-plated. Location and size of cutouts and keyslots are required.
- The fabrication drawing shall show the required layer stackup along with the overall board thickness.

4.12 綠漆 Solder Mask

4.12.1 簡介 Introduction

對於表面貼裝板，soldermask 必要的是：

波焊期間將橋減到最小

焊料洄流期間將球的橋減到最小

焊後清除

保護板免於氧化

Solder Mask is necessary for surface mount boards to:

- Minimize bridging during wave soldering
- Minimize bridging from solder balls during solder paste reflow
- Ease of cleaning the assembly after soldering
- Shield board from oxidation

4.12.2soldermask 材料 Solder Mask Material

在 SMT 或混合 PTH 和 SMT 裝配上使用乾燥薄膜 soldermask 在某種場合禁止被使用，一種最好的選擇是液體 photoimagable 保護來提高附著力，這個粘結力在第一次經過 SMT 裝配工藝期間減小化學親和力。

The use of dry film solder mask on SMT or mixed PTH and SMT assemblies strongly discouraged and in some cases forbidden. A better choice is a liquid photoimagable mask offering improved adhesion. This adhesion eliminates chemical entrapment during the first pass SMT assembly process.

Liquid photoimagable (Recommended of all board screening but not for hole plugging which could cause chemical entrapment).

- 在配圈墊片和連接器之間允許較小間距
- 當做屏保時不要濺殘餘物到墊片上
- 當熱產生環氧樹脂屏保時不要滲出殘餘物或沉積到配圈墊片上
- It allows for smaller spaces between land pads and conductors
- Does not splatter residue onto pads as do screened masks
- Does not bleed residue or slump on to land pads as do thermally cured epoxy-screened masks

液體 photoimagable（推薦所有板映射但不是爲孔塞能產生化學親合力）

Liquid photoimagable (Recommended of all board screening but not for hole plugging which could cause chemical entrapment)

- 標準 soldermask
- 連接器抛光-SMOBC（裸銅上 soldermask）
- 關於保護腐蝕 BGA 逃逸通孔，看“通孔設置指導原則”部分
- 除非墊片被生產工程師定義爲 SMDP，SMT 墊片上的 soldermask 是不允許存在的
- Standard solder mask
- Conductor finish-SMOBC (solder mask over bare copper)
- For masking encroachment on BGA breakout vias, see section called “Via Placement Guidelines”
- Masking on the SMT pads is not permitted unless the pads are “solder mask defined pads”(SMDP) by the manufacturing engineer ”.

4.12.3推薦 LPI soldermask　　Recommended LPI solder masks

注：專指粗面精整　　Note: Specify matte finish

- Enthone 3421
- Taiyo4000

4.12.4soldermask 指導原則　　Solder Mask Guidelines

- soldermask 穴應該定義爲大 0.006[0.15]比相關墊片或在結構圖中標示，soldermask 必須

遠離所有 SMD 墊片

- Solder mask openings should be defined as 0.006[0.15] larger (0.004[0.10]min.) than the associated pad on or noted in the fabrication drawing that the solder mask must remain off all SMD pads.
- " Gang"穴應該被用到所有 0.020[0.50]lead pitch 或低的元件，那樣的話，就不該在元件墊片上有 soldermask。
- " Gang" openings should be used for all devices with 0.020[0.50] lead pitch or below. That is, there should not be solder mask between the pads on these devices.
- 對於 soldermask 在 BGA 逃逸通孔上高出要求看"通孔設置指導原則"。
- For solder mask encroachment requirements on BGA breakout vias see section "Vias Placement Guidelines".
- 不允許有隆起通孔，因爲：
- Tenting vias is not permitted because：
- 在 soldermask 區下，化學親和力的存在引起通孔壁內空焊
- Of the possibility of chemical entrapment under the solder mask causing voids within the via wall.
- 在"OSP"拋光板上覆蓋著 Entek 包覆層，在微波焊過程期間空氣排出在 BGA 錫焊接頭處可能產生空焊
- On "OSP" finished boards covered with an Entek coating, out gassing may occur during wave soldering process creating voids in the BGA solder joint.
- soldermask 應該超過線邊延長最小 0.003[0.08]連接到配圈墊片
- Solder Mask should extend a minimum of 0.003[0.08] beyond the edges of traces adjacent to land pads.
- 在表面貼裝墊片上不允許 soldermask 產生，soldermask 高度應該等於或低於表面貼裝區域墊片的高度。
- Solder mask is not allowed on surface mount land pads. The level of the solder mask should be lower than or equal to the level of the surface mount land pads.