The Effect of Thermal Pad Patterning on QFN Voiding

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Abstract

Voiding under QFNs is a major challenge in the electronics industry. However, voiding can be suppressed by improving venting accessibility on the thermal pad by using solder mask dividing strips. Venting accessibility is defined as the perimeter length per unit area of the metal pad. Regardless of the shape and the number of subpads, increasing venting accessibility results in a decrease in the total number of voids, the largest voids, and discontinuity. Voiding caused by peripheral vias is comparable to voids caused by hidden vias. Voiding increases with decreasing print coverage and is attributed to insufficient solder. Voiding also decreases with an increase in the number of thermal vias. This phenomenon is attributed to volatiles bleeding through the small voids around the thermal via.

Key Words: solder joint, soldering, solder paste, lead-free, SMT, QFN, reflow, void, voiding, venting accessibility, thermal pad

Introduction

The quad-flat no-leads (QFN) package design is an ideal choice for many new applications where size, weight, and electrical and thermal properties are important. However, thermal pad voiding control under the QFN is a major challenge due to the large coverage area, large number of thermal vias, and low standoff. An earlier study indicated that both design and process are important for minimizing and controlling voiding. For a divided thermal pad, the solder mask defined (SMD) system is more favorable than the non-solder mask defined (NSMD) system, with the latter experiencing more voiding due to a thinner solder joint and possibly board outgassing. In this work, thermal pads divided by solder mask strips of various patterns are studied, with the solder mask strips serving as a venting channel. The conventional partial solder paste print approach via multiple isolated deposits is used as a control. The effect of pattern shape, number of thermal vias, venting accessibility, and solder mask strips are assessed and discussed.

Experiment

QFN Test Board and Component

In this work, a dummy QFN component (A-MLF68-10mm-0.5mm-DC-Sn) was used with 68 peripheral pads, 10mm long on each side, 0.5mm pitch, daisy-chained, and with a Sn surface finish, as shown in Figure 1.

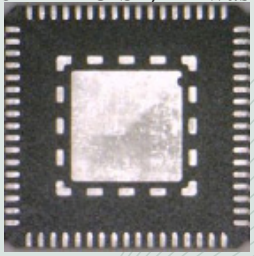

Figure 1. QFN component.

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The primary focus of this study is the effect of thermal pad design on voiding under the QFN. A photo of the QFN test board used in this study is shown in Figure 2. The board exhibits the following characteristics:

- Board thickness: 1.61mm
- Cu pad thickness: 0.05mm
- Surface finish: NiAu
- Microvia dimension: 0.1mm width, 0.1mm depth
- Solder mask: wet film, 0.05mm thickness

A test board with the QFN assembled is also shown in Figure 2.

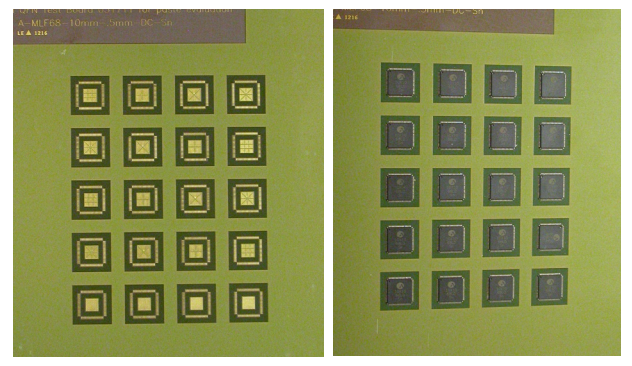

Figure 2. Photo of the QFN test boards before (left) and after (right) QFN assembly.

The primary focus for voiding control is the thermal pad design on the FR-4 test board, including (1) the number of thermal via on the thermal pad, and (2) the number and shape of solder mask divided thermal pads. The impact of the solder paste volume is regulated by the stencil aperture size. All parameters involved are shown in Table 1.

Parameter	Sub-Parameter	Layers
Thermal Pad on PCB	Thermal via number	16, 36
	Thermal subpad shape	Square, triangle
	Thermal subpad number	1, 4, 8, 9
Stencil (100 µ)	Aperture versus pad area	50%, 73%, 96%

Table 1. Parameters used in the voiding study.

Figure 3 shows more details about the thermal pad design. All subpads are divided by a solder mask.

Figure 4 shows the X-ray images of some of the QFN joints at the thermal pads with 96% paste printed. The voiding varies considerably from one design to another design, clearly demonstrating the importance of having a properly designed thermal pad.

A no-clean solder paste, SAC305 with type 4 powder and 88.5% metal load, was used for assembly of the QFN. For the test, the solder paste was printed through a stencil with 100 micron thickness onto the test board. The QFN components were then placed and sent through a BTU oven with air atmosphere. The reflow profile used is shown in Figure 5.

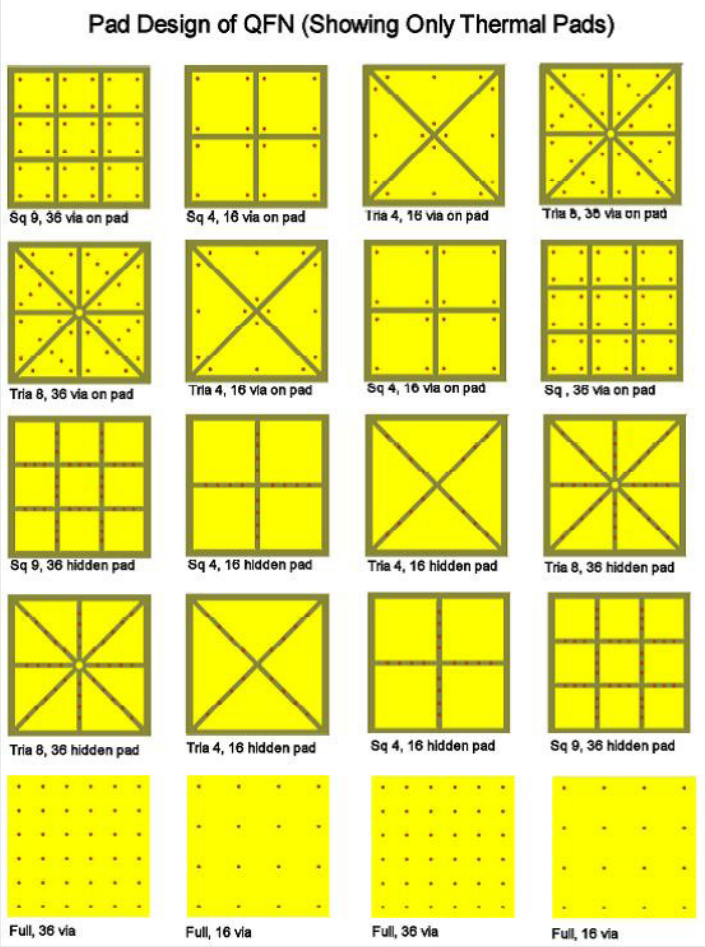

Figure 3. Pad design of the QFN test board, showing only thermal pad patterns.

Voiding Assessment

Three properties were determined, as defined in Table 2.

For some solder joints, cross-sectioning was also conducted in order to elucidate the characteristics of voiding.

Property	Definition
Discontinuity	Percentage of area under the QFN thermal pad where the continuity of the vertical metal from QFN to PCB surface is interrupted
Void Average	Average void area percentage of multiple QFNs within the metallic pad of QFN
Largest Void	The largest void measured for a category of QFN joints

Table 2. Definitions of three voiding properties.

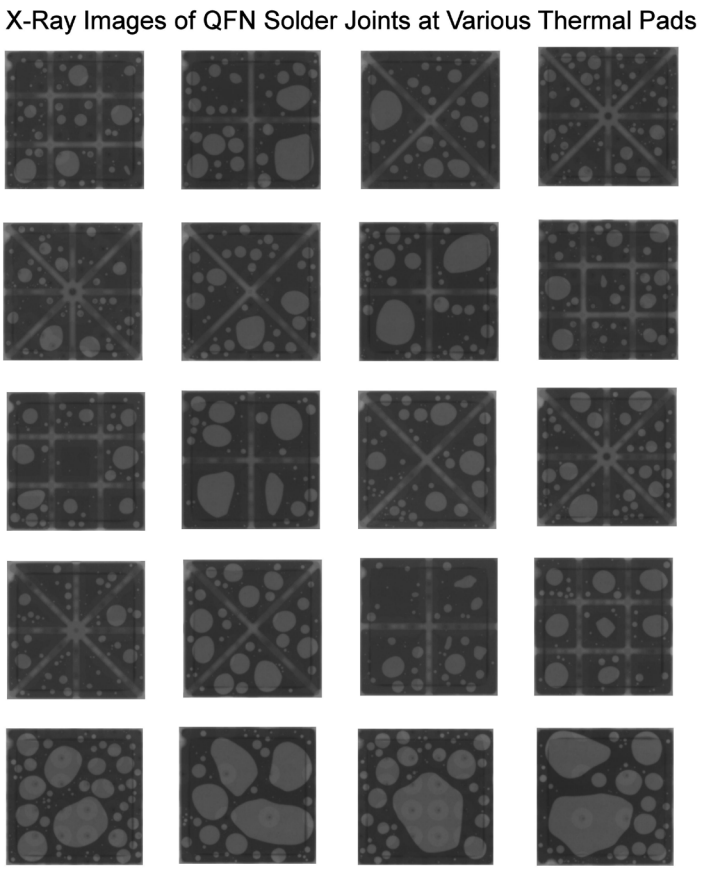

Figure 4. Examples of X-ray images of the QFN solder joints at various thermal pads with 96% paste printed .

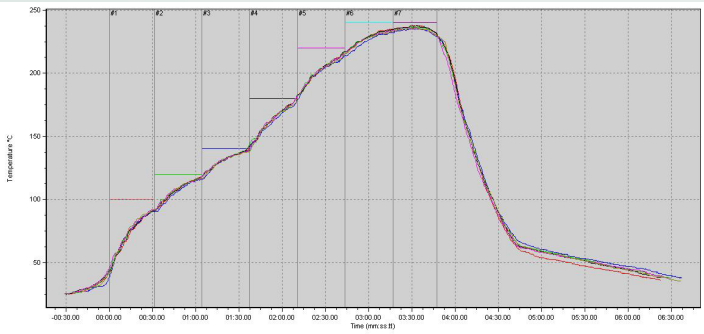

Figure 5. Reflow profile used for the QFN voiding study.

Results

The voiding results are presented in Figures 6, 7, and 8 for print coverage 50%, 73%, and 96%, respectively.

Effect of Pad Division

When plotting the total number of voids based on the pad design and print area, as shown in Figure 9, the total number of voids decreases considerably when the full thermal pad is divided into smaller subpads—the more divisions, the lower the voiding. Print coverage has a moderate effect on voiding,

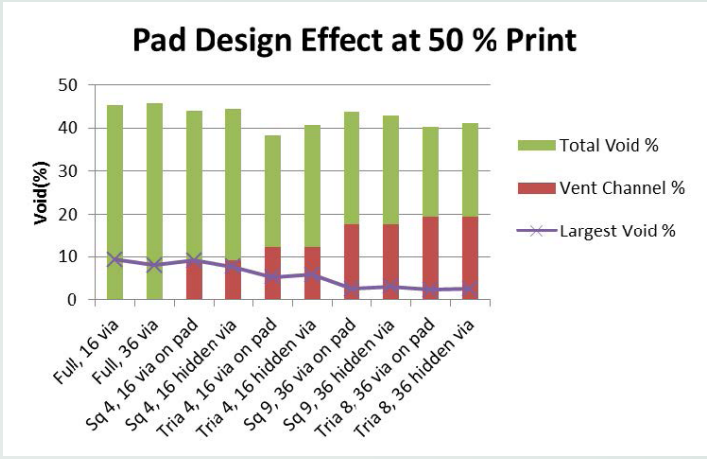

Figure 6. Voiding of a QFN with 50% print coverage.

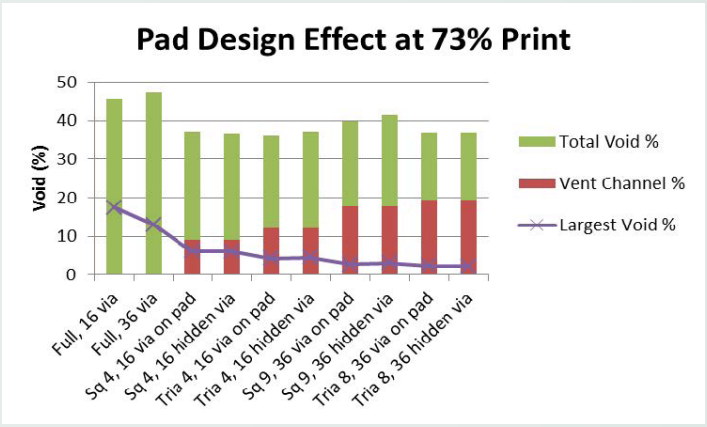

Figure 7. Voiding of a QFN with 73% print coverage.

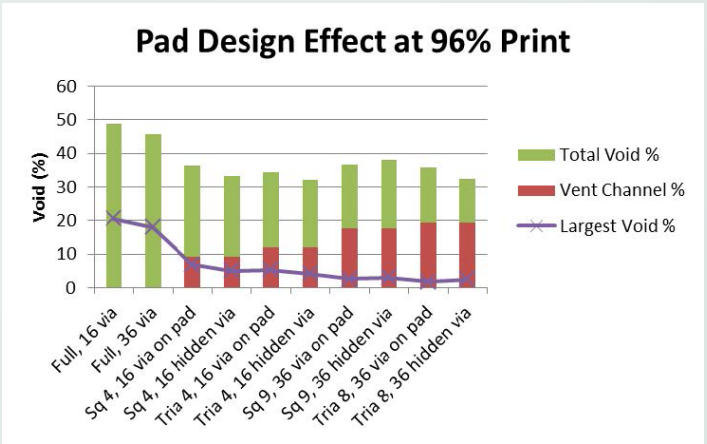

Figure 8. Voiding of the QFN with 96% print coverage.

with voiding increasing as print coverage decreases. Higher voiding associated with smaller print coverage is attributed to insufficient solder available to form joints between the QFN component and the thermal pad. Figure 10 shows examples of X-ray images of the QFN solder joints for various thermal pads with 50% paste printed. Unlike Figure 4 where some portions

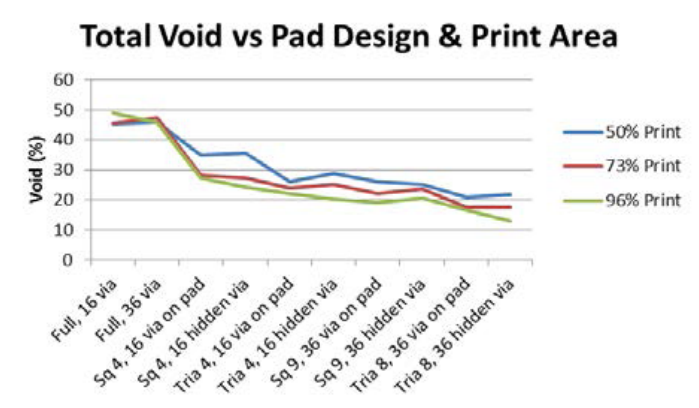

Figure 9. Relationship between the total number of voids, pad design, and print area.

of the venting channels were bridged by solder at 96% print coverage, the venting channels in Figure 10 are free of solder at 50% print coverage. This insufficiency in solder volume inevitably resulted in more voiding. The medium amount of voiding observed for 73% print coverage is attributable to the same cause.

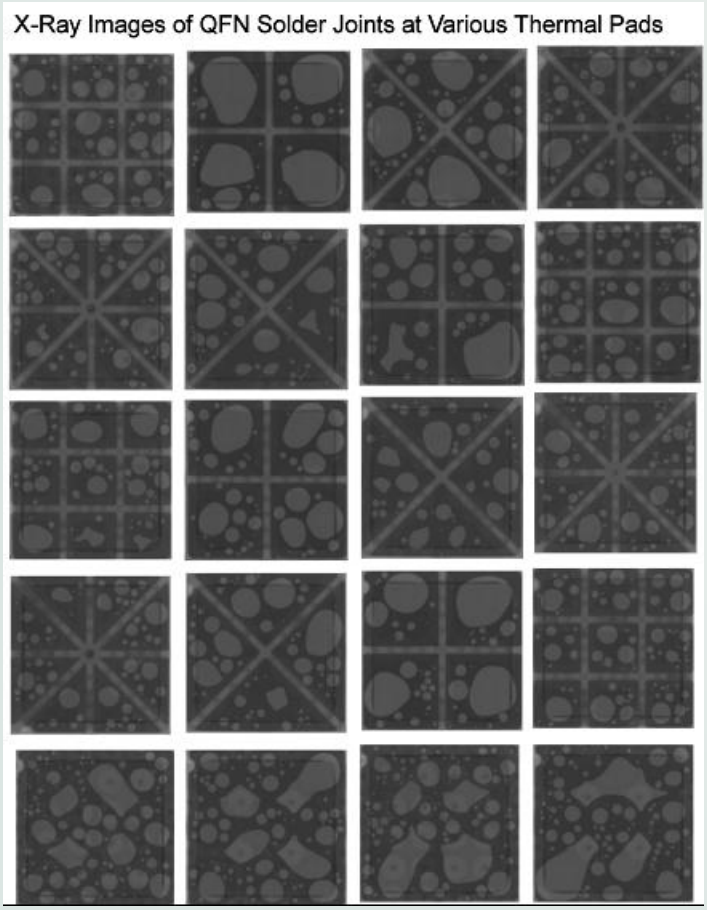

Figure 10. Examples of X-ray image of QFN solder joints at various thermal pads with 50% paste printed.

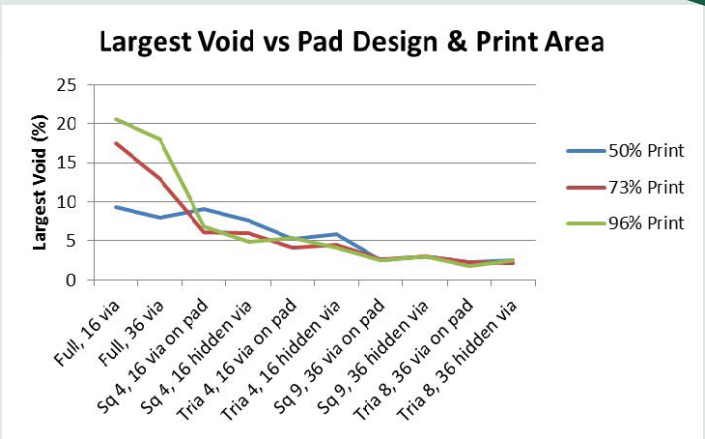

Figure 11. Relationship between the largest void, pad design, and print area.

The largest void is more sensitive to pad design, as shown in Figure 11. A drastic decrease in the largest voids occurs when the full pad is divided. The effect of print coverage is not significant, presumably due to the sporadic nature of the largest voids.

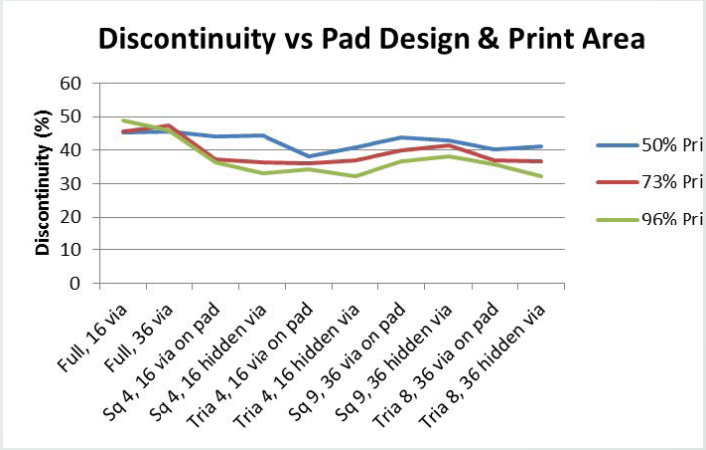

Figure 12. Relationship between the total number of voids, pad design, and print area.

Not only do the total number of voids and largest void decrease with the division of the thermal pad, but also the discontinuity reduces with pad division, as shown in Figure 12. Here the discontinuity decreases slightly with increasing pad division and increasing print coverage.

Venting Accessibility

In our previous study [1], voiding was reported to be proportional to venting accessibility. This venting accessibility is defined as the perimeter length per unit area of the metal pad. Table 3 shows the calculated venting accessibility of various thermal pad designs.

Thermal Pad Design	Venting Accessibility
Full Pad	4
Square 4	8
Triangle 4	9.66
Square 9	12
Triangle 8	13.66

Table 3. Calculated venting accessibility of thermal pad designs.

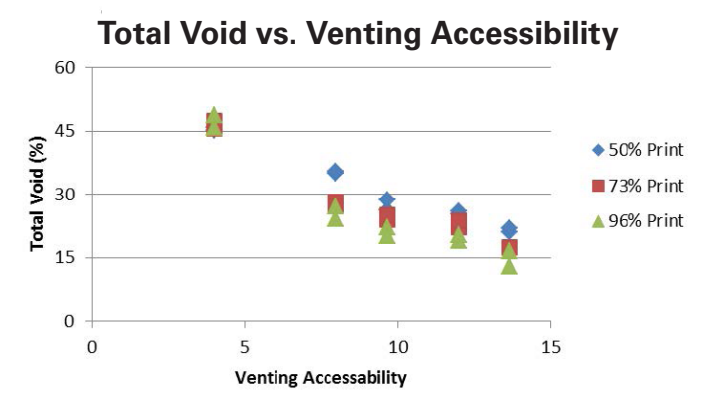

Figure 13. Relationship between the total number of voids, venting accessibility, and print area.

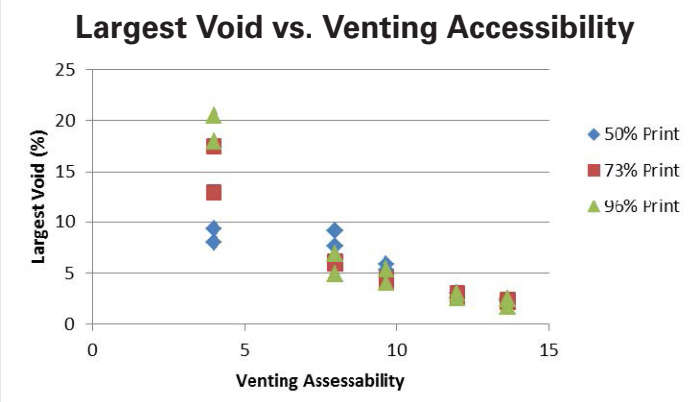

Figure 14. Relationship between the largest void, venting accessibility, and print area.

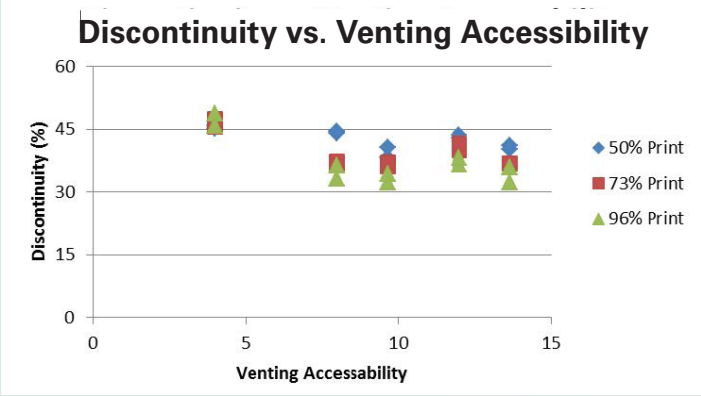

Figure 15. Relationship between the largest void, venting accessibility, and print area.

Figure 13 shows that the total number of voids decreases almost linearly with increased venting accessibility. Again, smaller print coverage results in more total voids.

The excellent correlation between the total number of voids and venting accessibility strongly support the validity of this venting accessibility model. The much higher correlation observed here over what was reported in an earlier work [1] is attributed to the reduced variables in this study. In the earlier work, the variables studied include subpad number and shape, venting channel width, SMD pad versus NSMD pad, reflow temperature, baking history, number of vias, print area, and peripheral venting. In this study, most of those variables are not included in the DOE, resulting in greater accuracy in voiding prediction.

The voiding prediction power of venting accessibility can also be observed on the largest void, as shown in Figure 14, and to a lesser extent, on the discontinuity, as shown in Figure 15.

The high accuracy of voiding prediction capability using the "venting accessibility" model allows the industry to highly accelerate the speed of thermal pad pattern design.

Via Location

As shown in Figure 3, thermal via for the divided pads were located either near the edge of the pad or hidden underneath the solder mask strips. In order to find out whether there is a difference in voiding control, the via location is plotted against the total number of voids (Figure 16) and the largest void (Figure 17), particularly for 96% print coverage case (Figures 18 and 19). Results indicate that the edge via and hidden vias have virtually no impact on voiding performance. This is understandable since a via at the edge of the pad does not contribute to voiding because the volatiles can escape so easily.

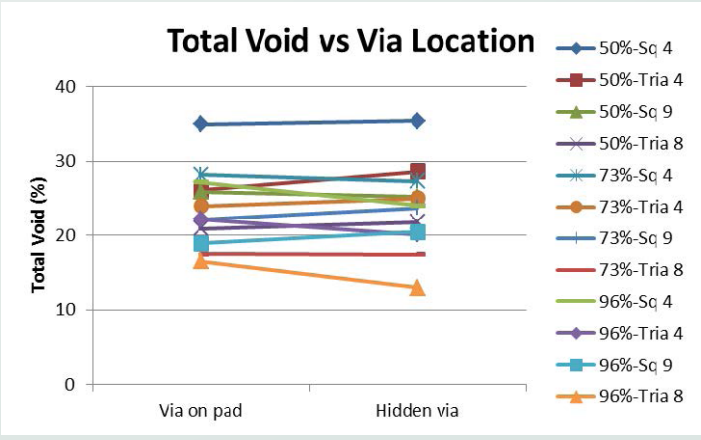

Figure 16. Relationship between the total number of voids and the via location.

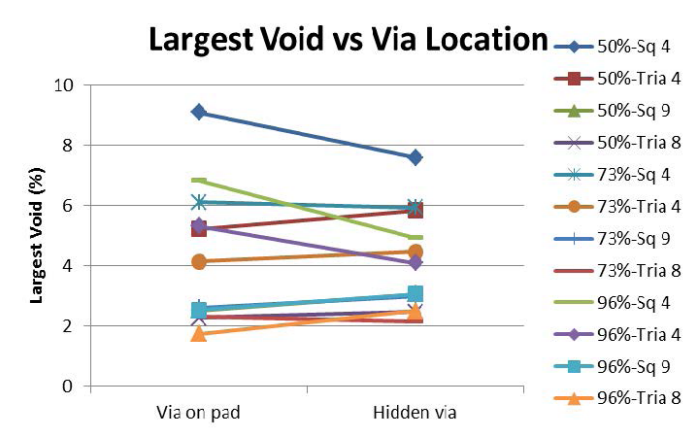

Figure 17. Relationship between the largest void and the via location.

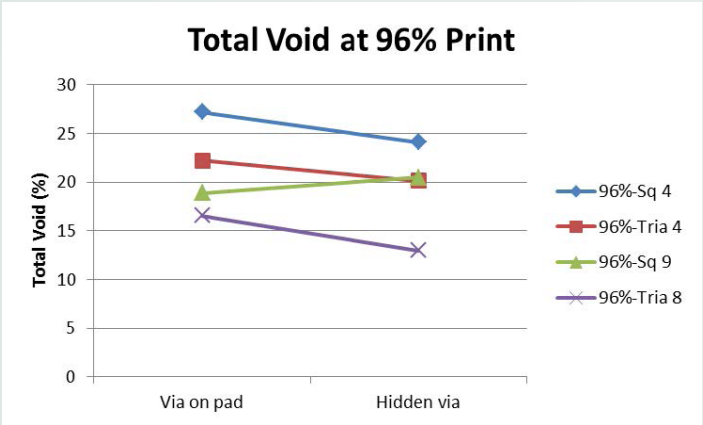

Figure 18. Relationship between the total number of voids and the via location at 96% print.

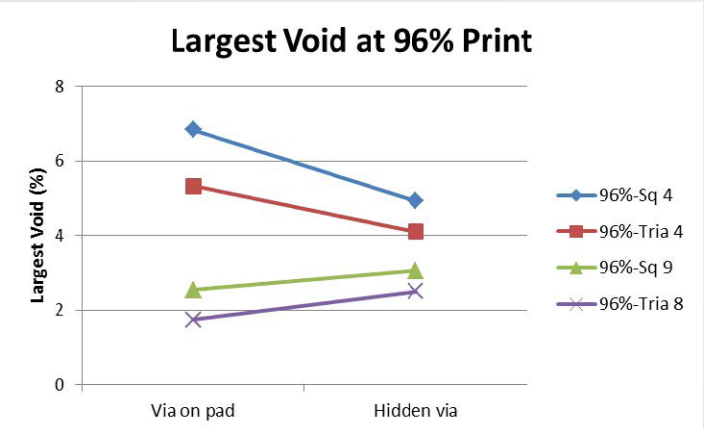

Figure 19. Relationship between the largest void and the via location at 96% print.

Via Number

When plotting via numbers against voiding, both the total number of voids (Figure 20) and the largest void (Figure 21) decrease as the number of vias increase, although no effect can be discerned on discontinuity (Figure 22). A decrease in voiding with an increase in the number of vias is unexpected, and is the opposite to what was found in a previous work [1]. This may be explained by the bleeding model, as shown in Figure 23. For peripheral vias, only small voids are apparent due to the easy access to the venting channel. However, those small voids can serve as a bleeding path for large voids entrapped in the middle of pad, and consequently, can result in lower voiding than a pad with fewer vias.

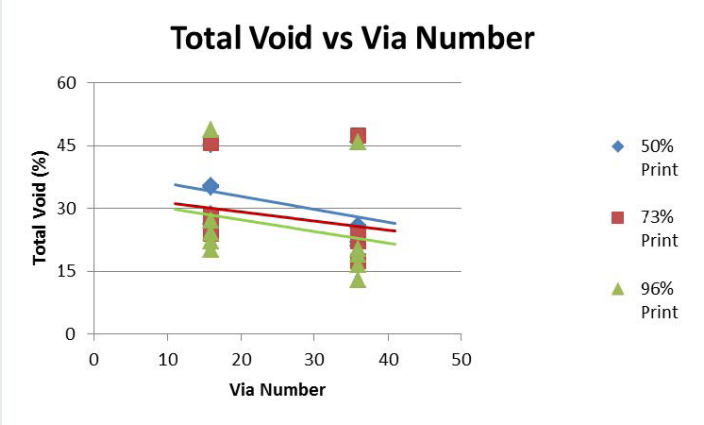

Figure 20. Relationship between the total number of voids, via location, and print coverage.

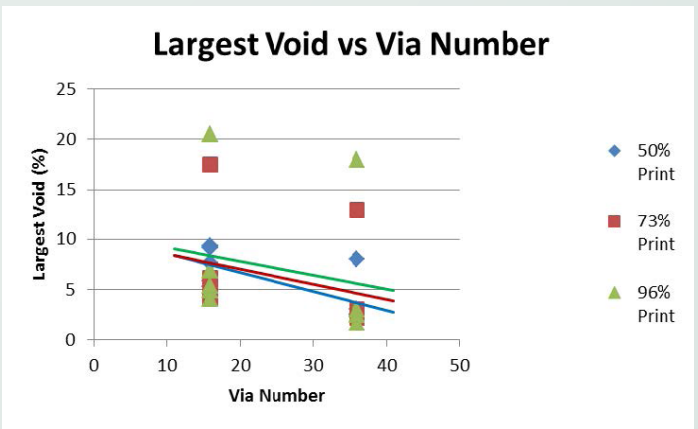

Figure 21. Relationship between the largest void, via location, and print coverage.

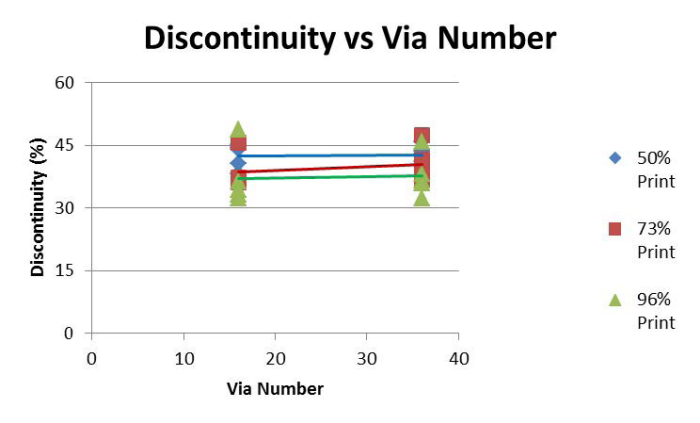

Figure 22. Relationship between discontinuity, via location, and print coverage.

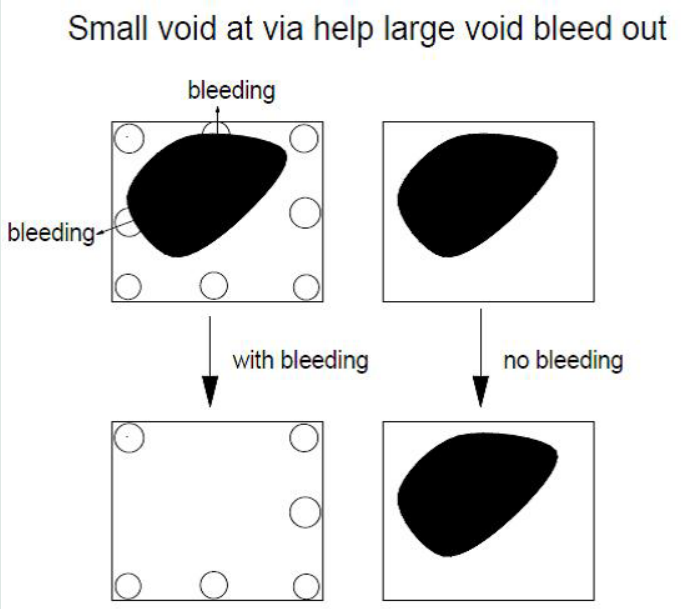

Figure 23. Small voids as the peripheral vias help large voids bleed out.

Conclusion

Voiding under the QFN can be suppressed by improving venting accessibility on thermal pad with the use of a solder mask dividing strip. Venting accessibility is defined as the perimeter length per unit area of the metal pad. Regardless of the shape and the number of subpads, an increase in venting accessibility results in a decrease in the total number of voids, the largest void, and discontinuity. Voiding caused by peripheral vias is comparable with that caused by hidden vias. Voiding increases as print coverage decreases and is attributed to insufficient solder. Voiding also decreases with an increasing number of thermal vias. This phenomenon is atributed to volatiles bleeding through small voids around the thermal via.

References

1. Derrick Herron, Yan Liu, and Ning-Cheng Lee, "Pad Design and Process for Voiding Control at QFN Assembly", APEX, San Diego, CA, Feb 28-Mar 1, 2011

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