TECHtips
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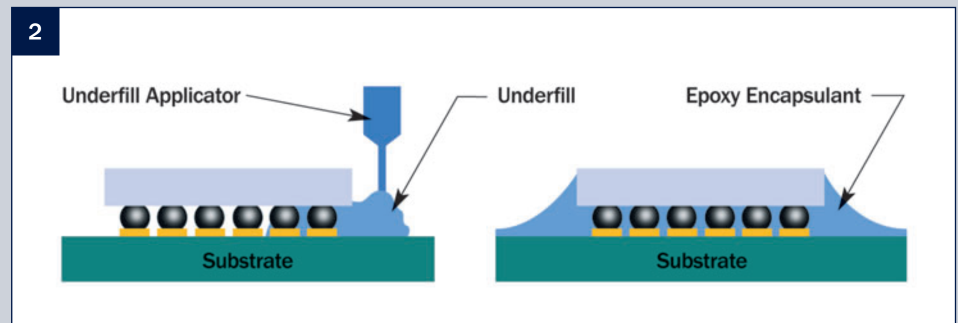
Electronics Manufacturing Insights from ACI Technologies, Inc.

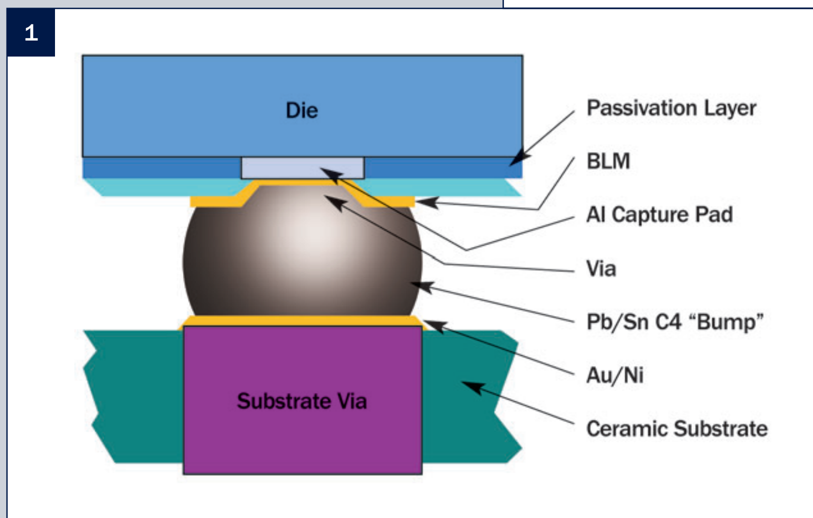
Flip Chip Attach Techniques

Last month we presented ***Flip Chip Rework***. As promised, this month we follow up with attachment techniques.

Flip chip assembly is a key technology for advanced packaging of microelectronic circuits. It allows attachment of a bare chip to a packaging substrate in a face-down configuration, with electrical connections between the chip and substrate via conducting "bumps." Flip chip technology was first invented by IBM for mainframe computer application in the early 1960s. Semiconductor devices are mounted face down and electrically and mechanically connected to a substrate (Figure 1). IBM called this manufacturing process a C4 process (controlled collapse chip connection).

Flip chip assembly offers many advantages. A key advantage is improved electrical performance. The small bumps of flip chip interconnection provide short electrical paths, which yield excellent electrical properties with low capacitance, inductance, and resistance. This results in greatly improved high frequency performance as compared to other interconnection methods such as wirebonded chip on substrate. Another important advantage of flip chip assembly is its compactness which reduces the size and weight compared to traditional wire bonded packages. The electrical connection pads on the chip and substrate surfaces can be laid out as an area array, rather than around the periphery of the chip which is a typical design for wire bond configuration. This 2D-array structure can save chip space and reduce the foot-print of the chip on the substrate. The low profile and small physical area of flip chip structures allow small electronic packages to be manufactured. Today flip chip devices can be found in electronic watches, calculators, cellular phones, electronic organizers, cameras, hand held devices, and many other products.





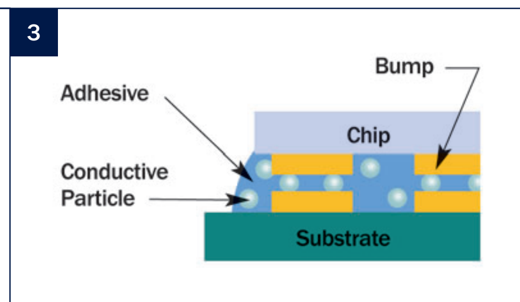


Figure 1: C4 Bumping on Si Chip [1]

Figure 2: Underfill Process [1, 2]

Figure 3: Anisotropic Conductive Adhesive [1, 2]

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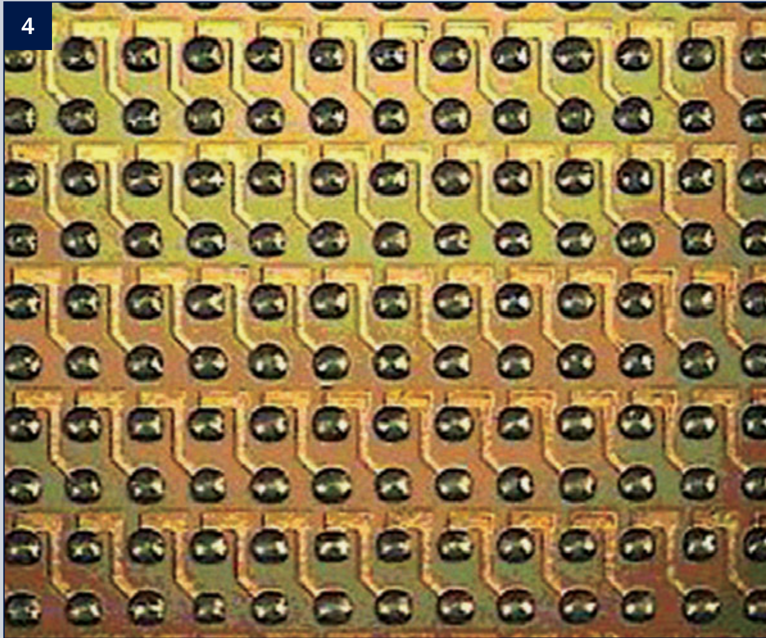
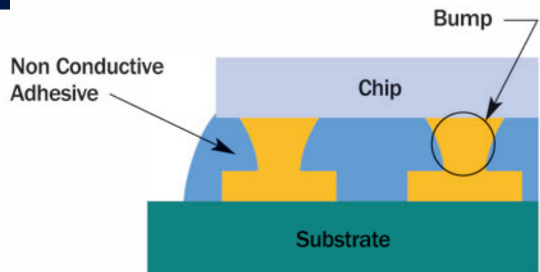
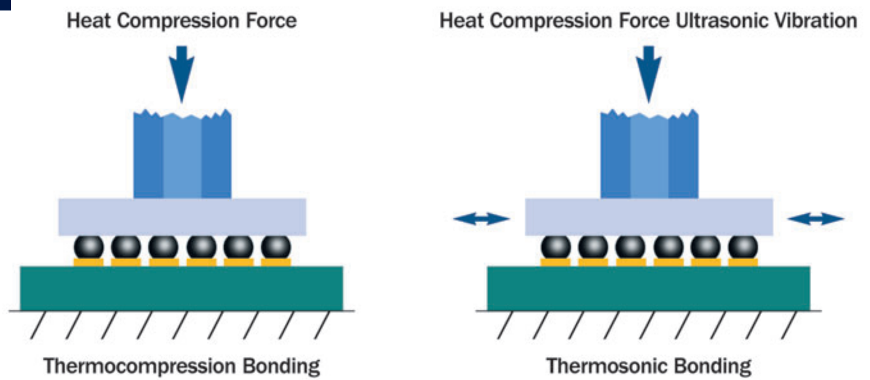


Figure 4: *Isotropic Conductive Adhesive Dispensed on Substrate (Courtesy Palomar Assembly Technologies, Inc.)*

Figure 5: *Non-Conductive Adhesive Bonding [3]*

Figure 6: *Thermocompression and Thermosonic Compression Bonding [2]*





Low-cost flip chip on boards generally use organic/laminate boards. A disadvantage of this board material is the large coefficient of thermal expansion (CTE) mismatch relative to silicon-based integrated circuit (IC) chips. If the assembly is subject to high temperatures at subsequent process steps, or undergoes temperature cycling in use as the device is powered on and off, stresses are created at the interfaces of the bump joints due to the CTE mismatch. These stresses, if sufficiently large, can lead to mechanical failure of one or more of the interconnects. This effect has been cited as the most common cause of failure in solder flip chip assemblies. To alleviate the problem of CTE mismatch, underfill encapsulant that has a CTE value between the substrate and flip chip is generally filled in the gap between the chip and organic circuit board. Underfill is dispensed along one or more edges of the chip and through capillary action flows under the chip and completely fills around the bumps (Figure 2). Upon curing, the hard underfill helps compensate for the thermal expansion difference by mechanically bonding the chip to the board and enhancing the reliability of the entire package.

The first type of flip chip (and 90% of today's market) uses standard tin/lead solder bumps. The remaining 10% of the devices use lead free metals like gold, gold/tin, indium, and adhesives to attach the chips to the substrate. Selecting the most appropriate assembly process depends on the chip bump metallurgy, substrate material (ceramic, laminate, glass), die size, and solder bump properties (bump size, pitch, and number of bumps). Some of the flip chip manufacturing processes along with their advantages and disadvantages will be discussed in this article.

Flip Chip Attach Using Adhesives

Bumping the chip is not always required in this method of attaching the chip to the substrate. Adhesive is applied to the substrate either by screen printing or selective deposition (dispensing or pin transfer) on the substrate pads. Chips are placed on the substrate with very high precision and cured at low temperature.

Adhesives used in flip chip assemblies can be broadly classified as conductive adhesives (CA) and non-conductive adhesives (NCA). Conductive adhesives are further classified

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as anisotropic conductive adhesives (ACA) and isotropic conductive adhesives (ICA). ACAs use low levels of conductive particles such as Au-coated polymer spheres, plated solid metal spheres, or low melting point solders like SnBi. Filler particles form connections when adhesive is compressed during die placement. Electrical conduction is only in the Z-axis as shown in Figure 3.

In the case of an isotropic conductive adhesive, a high concentration of conductive particles, usually Ag flakes, provide electrical conductivity in all directions. Dispensing or pin transfer of adhesive at selected regions on the substrate is performed to enable flip chip attach (Figure 4).

In the case of non-conductive adhesives, there are no conductive particles (Figure 5). Electrical connections are formed by applying pressure during chip placement. Adhesive is displaced and the chip bumps are mechanically and electrically attached to the substrate pads.

Flip chip attach using adhesives is best suited for small die which are not used in harsh environment (extreme temperature cycling, high humidity, high vibration). Since the die is already rigidly attached to the substrate, there is never a need for any underfill.

Flip Chip Attach by Reflow

For soldered bonds, the mechanical joint between the solder bump and the bonding pad (or the metal bump on pads) is formed by solder reflow at a temperature above the solder melting point. Prior to flip chip placement, flux is generally applied onto the bonding pads or solder bumps to remove any metal oxides that may prevent the solder from wetting the bonding surfaces. Flux residues, which are the reaction products of flux and metal, remain on the component and need to be cleaned off; otherwise they can cause corrosion of the microcircuit and give rise to long-term reliability problems. Even with no-clean flux systems, the flux residues can affect the performance of optoelectronic devices. Post-cleaning of the flux residues has been a big concern in solder-based flip chip bonding. Some flux residues are water soluble, while some have to be removed by aggressive solvents. For fine-pitch soldering, the residual flux may exist in the region where inspection and removal of the residue are almost impossible. Alternative fluxless soldering (e.g. plasma treatment, use of acetic acid or formic acid vapor, or halogen gases) might be applicable for some applications, but there is no single solution for the problem at present.

Flip Chip Attach by Thermocompression

Thermocompression (TC) bonding usually requires temperatures greater than 300°C. This temperature can damage some die attach plastics, packaging materials, and laminates, as well as some sensitive chips.

TC bonding has found application in gold and indium bump flip chip assemblies. The bumps are made on substrates using electrolytic plating or stud bumping methods. During the bonding process, the chip is picked up and aligned face-down to the bumps on a heated substrate. When the bonding tool presses down, the gold/indium bumps deform and make intimate contact with the bonding pads, causing pure metal-to-metal bonding to occur.

This bonding method requires gold chip-bonding pads for attachment. Aluminum pads are not very suitable due to their surface oxidation. Underfill is not generally required. The chip is typically sealed in an hermetic enclosure. TC bonding requires a flip chip bonder that is capable of producing the high bonding temperature of 300°C, a force of up to 100 cN/bump (0.22 pounds-force per bump), and a high degree of parallelism between chip and substrate. For high yield bonding, the bonding force and temperature need to be well controlled. In order to avoid damaging the semiconductor material, the bonding force must be applied with a gradient. Excessive bonding force may cause cracks in the chip passivation and sometimes bump bridging in a fine-pitch array due to over-deformation of the bumps.

Flip Chip Attach by Thermosonic Compression

Similar to thermocompression, thermosonic compression uses additional energy from ultrasonic vibration which allows a reduction in the heat and force required (Figure 6). Thermosonic flip chip technology is increasingly used in low pin count applications such as smart card, light-emitting diode (LED), and surface acoustic wave (SAW) filters in telecommunication applications.

Gold stud bump flip chip has many advantages over its ancestor, solder bump. The gold bump contacts are placed with a wire bonder and can be put onto any bond pad which can be wire bonded. They can be placed onto bond pads as small as 75 microns and on pitches as small as 125 microns. The gold bump is also more compliant than solder.

Since stud bumping can be done on a wire bonder, it does not require wafers or under-bump metallization (UBM). Single, off-the-shelf die can be bumped and flipped without pre-processing. This makes stud bump flip chip fast, efficient, and flexible for product development, prototyping, and low to medium volume production, while allowing easy scale up to high volume wafer-based production with automated equipment. Because stud bumping is a serial process, the bumping time required increases with the number of bumps. However, high speed equipment now can place as many as 12 bumps per second. Stud bump assemblies demand more precise die placement equipment and are less tolerant of placement errors than self-aligning solder

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	Anisotropic Conductive Adhesive	Isotropic Conductive Adhesive	Non Conductive Adhesive	Solder Reflow	Thermo-Compression	Thermosonic
Bumping Material	Au, In	Ni/Au bumps Indium bumps	Ni/Au, Sn/Pb, Au or Au/Sn	SnPb, AuSn	In, Au	Au or Cu stud bumps
Minimum Ball Diameter	100 µm	40 µm	30 to 75 µm	100 µm	50 to 100 µm	75 µm
Minimum Pitch	150 µm	75 µm	40 µm	150 µm	100 µm	125 µm
Contact	Mechanical	Mechanical	Mechanical	Intermetallic	Intermetallic	Intermetallic
Thermal Conductivity	Good for low heat generation application	Very good	Very good	Very good	Very good	Very good
Electrical Conductivity	Good	Very good	Good	Very good	Very good	Very good
Lead Free Application	Yes	Yes	No	Only when AuSn is used	Yes	Yes
Out Gassing	Is a concern in optical components/ hermetic application	Is a concern in hermetic packages	Is a concern in hermetic packages	No	No	No
Contamination	Contamination and bleed out may cause shorts	May create shorts	No	No	No	No
PCB Material	Laminate	Laminate	Laminate	Laminate and ceramic	Ceramic	Laminate and ceramic
Automation	Easy to automate	Yes	Yes	Yes	Yes	Yes
Self Alignment	No - need precision machine for placement	No - need precision machine for placement	No - need precision machine for placement	Yes	No	No
Curing Temperature	Low curing temperature	Low curing temperature	Low curing temperature	High reflow temperatures	150°C or less	100°C
Stress	Low stress on die	Need underfill to protect the die	No underfill required	Underfill is generally used	Underfill is generally used	Underfill required for laminates
Die Size	Good for small die with low I/O count	Good for small die with low I/O count	Small die 4 x 4 mm	4 x 4 mm through 12 x 12 mm die	3 x 3 mm through 14 x 14 mm die	5 x 5 mm
Rework	Possible	Difficult	Possible	Possible	Difficult	Possible

Table 1: Flip Chip Technology Comparison

assemblies. The thermosonic flip chip bonding process is proven to be useful for die with dimensions up to 5 x 5 mm and up to 68 I/Os.

Summary

Table 1 summarizes the variations in flip chip technology. Some advantages of flip chip packaging over traditional wire bonded packages include:

- Flip chip technology overcomes wirebond pad pitch limitations.
- Flip chip technology provides electrical designers many advantages in the design of power and ground distribution on die.
- Flip chip technology provides improved signal integrity for high speed or high frequency designs.
- I/O can be distributed in 2D array around the chip, whereas wire bond chips, pads are restricted to outer perimeter of the die.

ACI Technologies can assist with selecting the most appropriate flip chip technique for specific applications as well as help with flip chip questions or concerns. For more information, contact ACI at 610.362.1320 or via email to helpline@aciusa.org.

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