An Experimental and Computational Study of the Current Carrying Capacity of High Performance PWB Interconnections

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Abstract

Recent technology advancement has enabled enhancement in PWB electrical performance and wiring density. These innovations have taken the form of improved materials, novel PWB interconnect structures, and manufacturing technology. One such advancement is Z-axis conductive interconnect. The Z-interconnect technology involves building mini-substrates of 2 or 3 layers each, then assembling several mini-substrates together using conductive paste. Designing and manufacturing the mini-substrates separately, then assembling them together, makes it possible to reliably manufacture substrates with no via stubs, very low-loss materials, and high wiring density. The conductive paste is not quite identical to copper, the conductivity is a bit lower and structurally it's different than a plated copper barrel. This paper will examine some thermal and mechanical performance metrics to compare vias with and without conductive paste joints.

In most high performance systems (with the exception of board cooled applications such as in the avionics industry), the bulk of the power is dissipated in the chip package with the PWB playing a minor role. However, power delivery is a primary function of the PWB. Increased power requirement translates to increased electrical current flow in the board which leads to ohmic (joule) heating of the conductors. Thus, the current carrying capacity of conducting layers, joining layers, planes, and vias becomes important from both a performance and reliability standpoint. [1]

Traditional industry standard guidelines have tended to focus on generic conditions and conservative analysis. While adherence to these guidelines is sure to meet performance requirements, there are many situations where more optimized designs are needed. Consequently, an application oriented approach is better suited.

This paper deals with the current carrying capacity of Z-interconnect vias and joining layers under specific, commonly encountered conditions. Both laboratory experiments and simulations are used to perform the study. An experimental test vehicle has been used to characterize temperature rise of PWB vias under different conditions. A numerical model is developed and validated with the experiment data. The numerical model is then exercised to determine internal via temperature rise under a variety of conditions. Results obtained so far indicate that these joints are capable carrying currents in range of 3A to 5A.

Introduction

As complex circuit board assemblies get denser and higher in signal frequency, they require more and more current. For a multi-module large digital board, it is not uncommon to have 10 or 20 modules, each of which needs 200A at some core voltage near 1.0 volts. Each module also has thousands of I/O which drive designs toward massive multi-layer boards (>50 layers) and very thick boards. (>250 mils) New circuit board technology, such as Z-interconnect, is a good fit to manufacture reliable, thick, high density circuit boards. An area that needs further investigation is the high-current capacity of the conductive paste. It is a different geometry and material than copper plated vias since conductive paste is a solid cylinder of material, rather than a plated barrel, and the paste is a nano-material with conductive particles floating in a polymer matrix. It is expected that it will perform similarly to copper since the DC resistance of the paste joint is nearly identical to a copper barrel. The slightly lower conductivity of the paste is offset by the extra cross-sectional area of the solid cylinder. The thermal expansion of the paste is similar to the copper, so no extra stress is expected on the joints.

The work in this paper involved building and measuring test vehicles to generate temperature vs. current data. It included simple thermal models as well as 3D thermal simulations to correlate with the lab measurements. Construction of Z-interconnect and test vehicle design will be described. Test results will be shown. Thermal model results will be compared to test results. Finally, a few other common configurations will be modeled to emphasize the difference in results between the lab setup and a typical full assembly.

Z-interconnect construction

The methods used to build a Z-interconnect structure begin with a series of building blocks called sub-composites. These mini-circuit boards are attached together with conductive columns in a joining layer, only where needed. [2] The result is sketched below. (**Figure 1**)

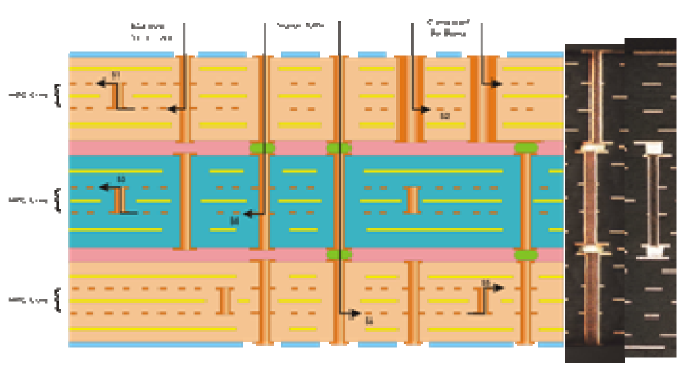


Figure 1 Z-interconnect cross-section

Sub-composites are built like any typical circuit board and can be anywhere from 2 to 40 layers. The joining core starts with an off-the-shelf laminate with 2 layers of copper attached to a dielectric sheet. Then shapes and lines are etched into the copper on both sides. A layer of dielectric and copper is stuck to both sides of the etched plane-plane core. Holes are then drilled all the way through the structure. Lastly, the hole is filled with conductive paste and the outer copper is etched away, yielding a 0S1P joining core. These steps are sketched below. (Figure 2)

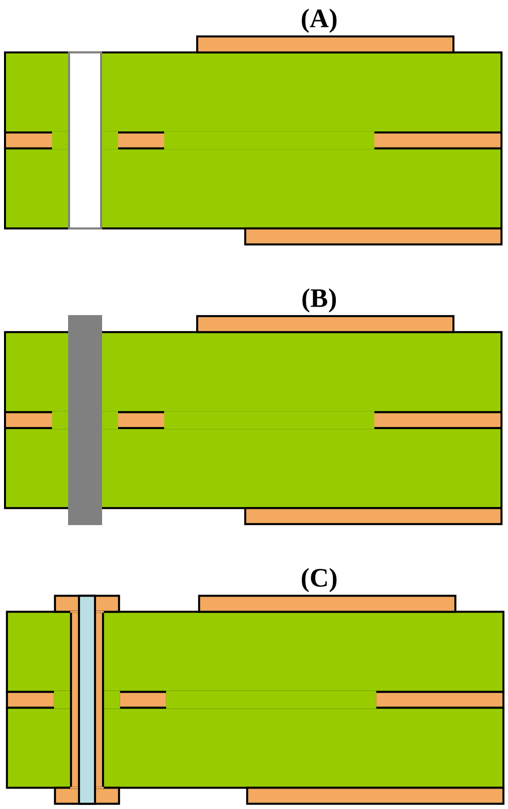


Figure 2 Fabrication of joining and signal cores (A) Drill laminated 2P core; (B) Paste fill drilled 2P core; (C) Signal sub-composite

A signal layer sub-composite process starts the same as the 0S1P core, up to attaching the dielectric and metal layers to the 1P structure. As the next step, instead of drilling, the outer copper is etched to create all the signal features. Lastly, the holes are drilled and plated to make the 2S1P core. Most boards can be made as a signal sub-composite. The 0S1P cores and signal sub-composites are combined to make a Z-interconnect stack-up. **Figure 2 and Figure 3** show simplified diagrams of Z-interconnects which include joining cores, signal sub-composites and their combined structures.[5]

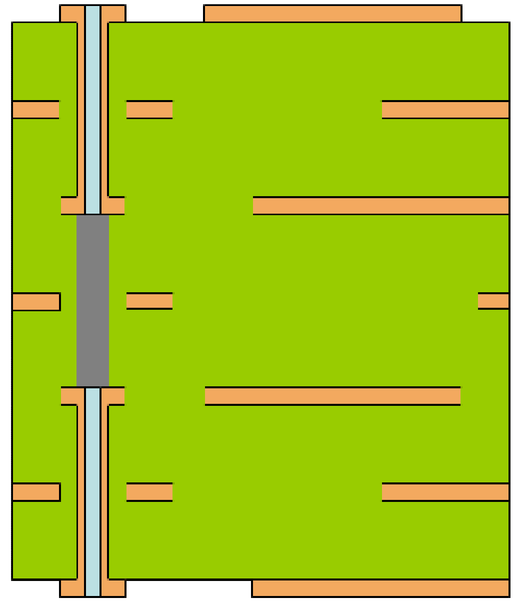
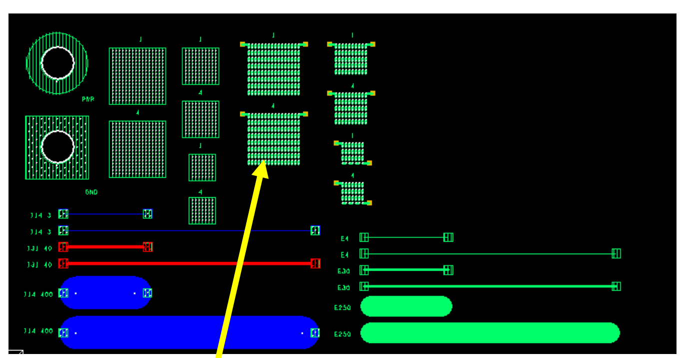


Figure 3 Z-interconnect composite stack-up

Test Vehicle Design

Test vehicles were designed to investigate vias in configurations where they carry multiple amps per via. The board stack-up had 55 metal layers divided into 4 sub-composites with 3 Z-interconnect joining structures. Via arrays were configured in daisy chain arrangements and in parallel via structures. Each via, in the test vehicle, was an 8-mil drill, plated to 6-mil finished diameter. The via-arrays were 7x7, 10x10 and 16x16. Each via array had 3 different Z-interconnect arrangements: sub-composite 1 only, no Z-interconnect joints, sub-composite 4 & 3, 1 Z-interconnect joint, and via stack through the board, all subs (1-4), 3 Z-interconnect joints. In addition, internal and external traces were designed to exercise vias in the same Z-interconnect configurations as via arrays: 0, 1 and 3 Z-interconnects. Large through holes are used to connect power supplies for testing. **Figure 4** is a snapshot of the TV design.



256-via daisy chain, passing through 4 sub-composites

Figure 4 Top view of test vehicle design

Lab Measurement Results

The measurement setup used 6032A HP power supplies connected to the daisy-chain pads, trace pads or large through holes for parallel via structures. Current was pushed through cables soldered to the pads on the board. In order to measure different structures, the cables were de-soldered, moved and soldered to the next structure. The board was clamped to allow ambient air access to both sides of the board, no fans were used. A thermo-couple was attached to the outside layer of the board roughly at the middle of the structure. Power was applied to the structure and the temperature was measured after 30 minutes. Resistance was also measured before and right after the temperature measurement. Results are shown in **Figures Figure** 5**, Figure** 6 **and Figure** 7**.**

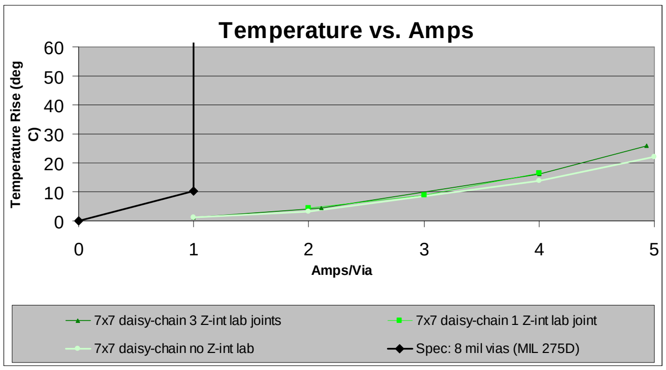


Figure 5 Measurements of 7x7 daisy-chain via array

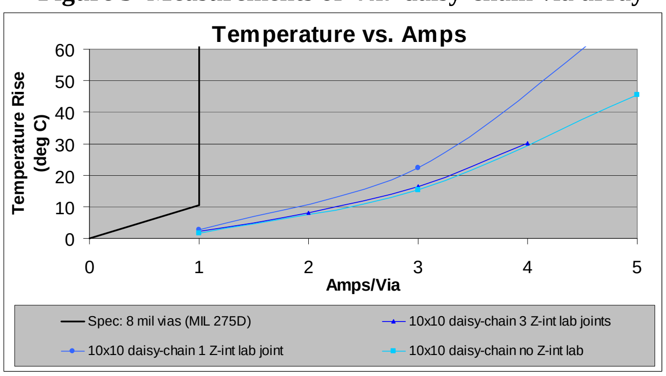


Figure 6 Measurements of 10x10 daisy-chain via array

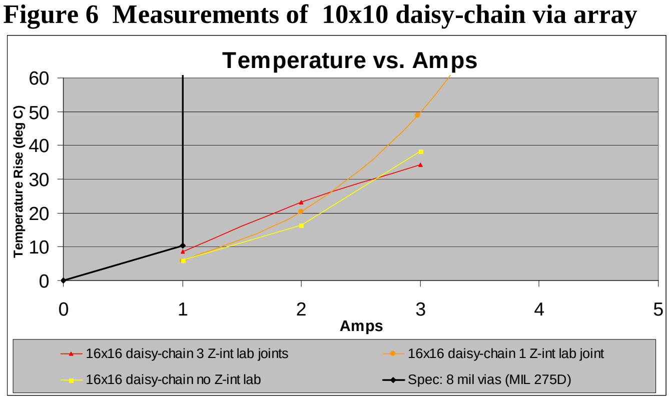


Figure 7 Measurements of 16x16 daisy-chain via array

Results showed that larger via arrays got hotter than smaller arrays. Results showed that vias halfway through the board were worse than short vias and worse than vias that went all the way through the board. The vias all the way through had a more direct path to ambient air and were closer to additional voltage/ground planes that assist in heat spreading. Vias with Z-interconnect joints easily met the MIL-275D spec.

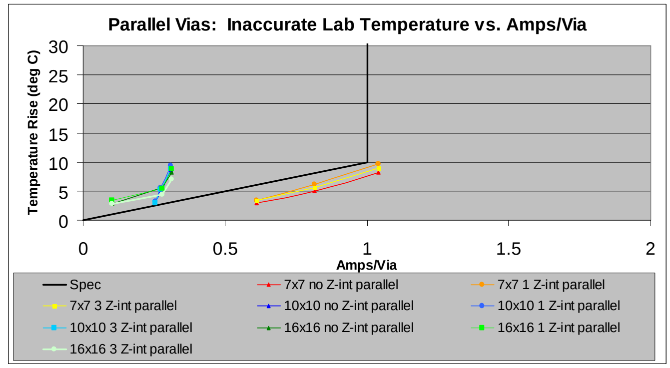


Figure 8 Measurements of parallel via arrays

Lab results from measuring parallel vias did not match what was expected. (**Figure 8**) It was discovered that it's very difficult to measure small temperature changes due to high currents and low resistances. Unwanted heat from the fixtures obscures the heat from the test structure. In the 16x16 array, vias carrying a few tenths of an amp heated up nearly 10 degrees. The same vias in a daisy chain configuration, heated up less than 3 degrees with the same low current. It was discovered that the heat that generated the 10 degree rise did not come from the via structure. The 1 meter, 8 AWG cables from the power supply to the via array were carrying up to 51 Amps and they got a little warm. The wires were about 1m in each direction, 2m roundtrip, that calculates to 40 milli-ohms of resistance. In addition, to make a controlled return path, the test vehicle had one ground plane connected at the bottom of each parallel via array, which was an inch or 2 away from the power supply ground return wire. That ground plane path added another 2 or 3 milli-ohms to the resistance. The arrays were only 10 to 200 micro-ohms total due to all the parallel vias. Therefore 51 Amps through 40 milli-ohm cable and 3 milli-ohm ground plane completely overshadowed the 100 micro-ohm parallel via structure.

Results from measuring wires showed that internal traces were a lower temperature than external traces, which is different from the MIL-275D spec. This may be due to the many layers of copper planes in the test vehicle. [3] The copper quickly conducts heat to the edge of the board, spreading the heat from an internal trace so it can radiate from the entire surface of the board. The external trace is further away all those copper planes. **Figure 9** and **Figure 10** and **Figure 11** show lab results from measuring temperature on various board traces.

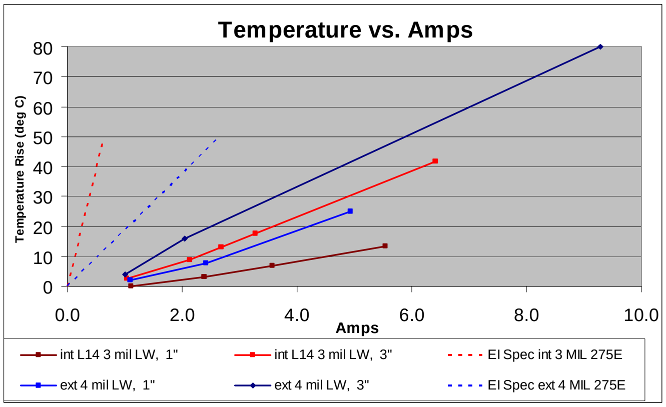


Figure 9 Measurements of narrow traces

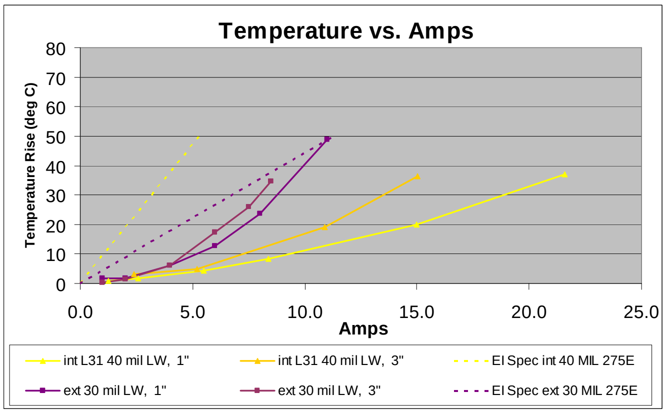


Figure 10 Measurements of medium traces

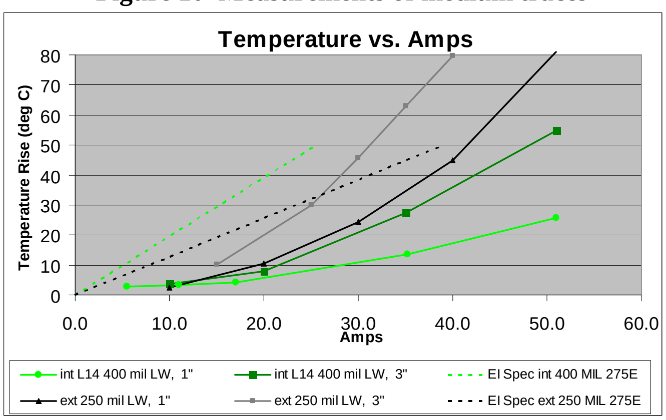


Figure 11 Measurements of very vide traces

Modeling and Simulation

In order to predict and understand the measured results, models were built and simulations were performed on the test vehicle structures. The simple model was built by using thermal resistances and a single heat source representing the via or trace structure. (**Figure 12**)

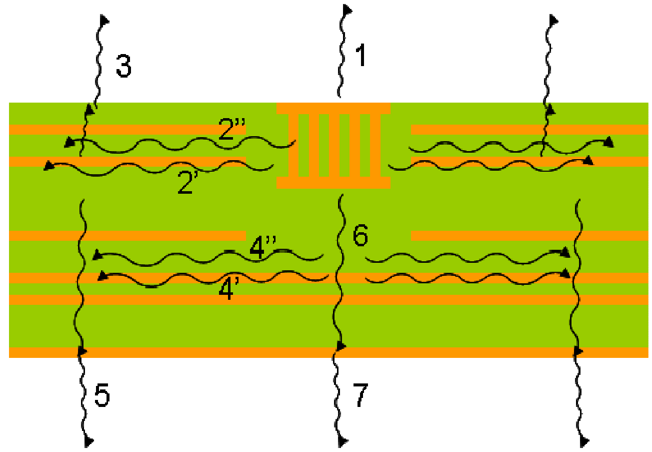


Figure 12 Schematic showing heat flow paths in the test vehicle design

Intuitively, one might expect that path 1 (**Figure 12**) directly above the via structure is the most effective path for heat dissipation. However, due to the relatively high thermal conductivity of copper (385 W/mK) and dielectric (0.3) vs. air (0.03), it turns out that cooling paths 2+3 and 4+5 conduct the majority of the heat. Also, the copper paths of 2' and 4' dominate the heat spreading effect, 2'' and 4'' are much higher thermal resistance. Using simple thermal resistance models:

Rectangle:
R_t = length/Area/T_{cond} (T_{cond} = thermal conductivity)
3D Trapezoidal or Conical shape:
R_t = length/A_{eff}/T_{cond}, where A_{eff} = sqrt(Area1*Area2),

Thermal resistances 2, 4 and 6 are calculated. Thermal resistances 1,3,5 and 7 involve the fluid dynamics of air and are difficult to calculate. A curve fit based on empirical data was used [4]. The total model has significant inaccuracies due to the imperfections of estimating thermal resistance of a board surface to air, and due to the simplified models. The model is probably accurate to a factor of 2 and is designed to be conservative bound. It is meant to develop an understanding of the heat flow of a system and to make a quick estimate of the temperature a structure reaches at a given current.

An example of the simple thermal resistance model is shown in **Table 1.**

Table 1 Thermal resistances for via array model

Rt = Thermal Resistance					
Via Array Description	Rt Total C/W	Lab C/W	Rt1	Rt2'	Rt2"
256 daisy no Z-int model	7	6	84	83	1459

Via Array Description	Rt3	Rt4'	Rt4"	Rt5	Rt6	Rt7
256 daisy no Z-int model	10	56	581	12	48	68

Table 2 Thermal model results for via arrays

Via Array Description	Model total C/W	Raw Measured C/W
49 daisy no Z-int model	11.8	7.4
100 daisy no Z-int model	9.5	8.1
256 daisy no Z-int model	7.2	6.2
49 daisy 1 Z-int model	9.5	7.6
100 daisy 1 Z-int model	8.0	6.6
256 daisy 1 Z-int model	6.5	5.6
49 daisy 3 Z-int model	5.6	5.7
100 daisy 3 Z-int model	5.2	4.2
256 daisy 3 Z-int model	4.6	3.8

The via array model correlated fairly well with raw measured data. (**Table 2**) As desired, the model was usually conservative, predicting a higher temperature than the actual measurement in lab. The total thermal resistance, degrees C/W from trace models correlated well with raw measured data, but the correlation degraded at very large line widths. (**Table 3**) This was due to the measurement, not the model. Line widths of 250 and 400 mils required lots of current to heat them up, and similar problems occurred as with parallel vias; the power cable heated up instead of the trace.

Table 3 Thermal model results for board traces

Via Array Description Internal Traces	Model total C/W	Raw Measured C/W
internal 3-mil LW, 1"	3.3	2.3
internal 3-mil LW, 3"	3.2	2.3
internal 40-mil LW, 1"	3.2	3.7
internal 40-mil LW, 3"	3.0	2.6
int 400-mil LW, 1"	3.1	4.1
int. 400-mil LW, 3"	2.9	3.5
External Traces		
external 4-mil LW, 1"	6.2	6.3
ext 4-mil LW, 3"	6.1	5.4
ext 30-mil LW, 1"	6.1	N/A*
ext 30-mil LW, 3"	5.8	6.7
ext 250-mil LW, 1"	5.7	N/A*
ext 250-mil LW, 3"	5.3	5.5
* Lab measurement failed		

In the thermal models, changes with temperature are ignored. It is well known that resistivity of copper increases with temperature. However, the thermal resistance path to air decreases due to convection and radiation. These factors offset somewhat, but it is clear from calculations and lab data that the increased copper resistance is stronger than the increased air convection. This is shown by temperature vs. current curves bending upward, above a straight line (**Figure 7**). The temperature effect adds a small error to the thermal model, with the error increasing as temperatures increase. The simple thermal model can be improved to be accurate above 100 degrees C, by including a temperature coefficient of copper resistance and a temperature coefficient of air cooling.

A 3-D model of the test configuration was created to validate the results and to study the effect of varying the boundary conditions on the current carrying capacity of the vias. The 16x16 daisy chain array passing through the entire board was picked for model validation (see location in Fig.5). A finite volume computational fluid dynamics (CFD) model was created in ICEPAK ™. This model included the effects of heat generation in the via structure, conduction within the PWB, and convection/radiation on the surface of the PWB.

The via/trace field was modeled as a single heat source and the effect of including each individual via was not modeled. Although it is possible to include each via separately, it was deemed unnecessary for the purposes of this study. This can be illustrated by a simple 1-D calculation. The effective thermal resistance of vias and joining layers is calculated to be about 1750 C/W.

For the current values used in this study, the heat generated in the electrical path is <0.08W. Of this, less than 2% of the heat is dissipated (as determined in the 3D model simulations) vertically in the via barrel. The rest is conducted away through the board. This yields a temperature rise of < 3C. However, depending on the PWB and other external conditions, it might be useful to include finer details of the via structures in the model.

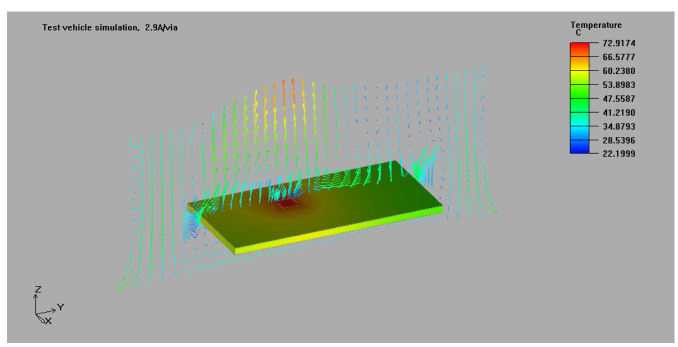


Figure 13 Flow vectors and temperature contours. 256 daisy chain array, 2.9 amps per via

Figure 13 shows representative temperature contours and velocity vectors for one of the cases studied. The adjoining table summarizes the results for all the cases. The maximum error between the modeled and measured temperature difference is about 15%. The geometry considered here is one of combined natural convection and radiation and the agreement is reasonable. In most practical situations involving high current, heat transfer is governed by conduction to a surface of fixed temperature. The predictive capability of the model is expected to be more accurate. (**Table 4)**

Table 4 3D Thermal simulation results of test vehicle 16x16 daisy-chain structure

Amps per via	Power (Watts)	Ambient (C)	Temperature (C)		% diff
			measured	model	
1.1	2.4	22	31.2	30.1	12.0
2.0	7.5	22	49.0	44.9	15.2
2.9	18.4	22	80.6	73	13.0

In a high current application, rarely is there a situation where there is no active thermal management scheme. Typically, a high performance heat-sink with forced airflow is present. **Table 5** below gives the temperature rise of the via in the form of thermal resistance as the airflow rate across the board is varied. The base value for zero airflow is the same as the value obtained in **Table 4** for 2.9A/via.

Table 5 Change in thermal resistance as a function of airflow rate. Same PWB conditions as TV (2.9A per via in Table 4)

Airflow (m/s)	Ambient (C)	Temperature (C)	Thermal Resistance (C/W)
0	22	73	2.77
0.5	22	60	2.07
1	22	56	1.85
2.5	22	52	1.63

The 3-D model was used in a recent application to determine the current carrying capacity of the vias. A schematic of the configuration studied is shown in **Figure 14**. The 63 layer PWB consists of several uniformly distributed LGA modules. Such a configuration lends itself to characterizing a symmetric unit cell. One such unit-cell consists of two "one quarter module" sites and one power bus bar site. **Figure 14** and **Figure 15** show schematics of the configuration.

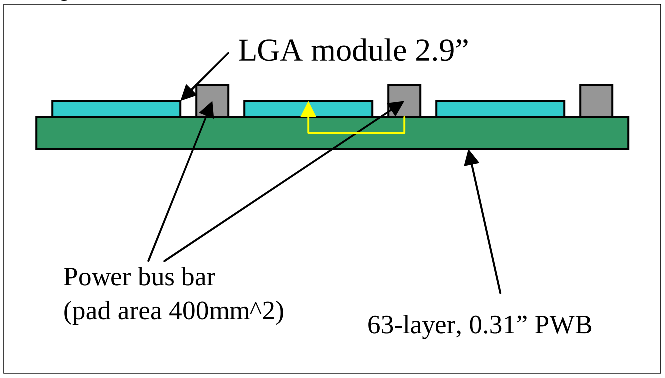


Figure 14 Cross-sectional view of PWB with LGA modules and power bus bars. Current flow path is shown by yellow arrow

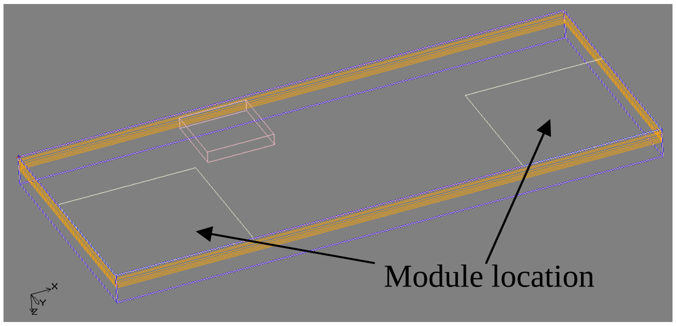


Figure 15 Unit cell configuration showing two 1-quarter LGA modules and one power bus bar

The PWB is a 63 layer 4 subcomposite/3 joining layer construction. There are 8 voltage planes (VDD11) for high current delivery. The power delivery vias were 26 mils drilled diameter and 24 mils plated. A total of 81 vias were used for voltage connections. As shown in Figure 15, the current flow is from the power bus bar through vias into eight parallel voltage planes and into the module. Figure 16 shows a schematic of current flow in the via as it splits into the eight voltage planes. One feature of this design is that joule heat generation progressively decreases along the length of the barrel as current is diverted into the voltage planes. The module is a high power component with active thermal management. The PWB surface temperature at the site of the module is 70C.

Using the boundary conditions described above, simulations were run to obtain the maximum temperature rise of the via field under the bus bar. The only path for thermal management is through the module sites. Essentially, the board is cooled by the module heatsink. This is a conservative estimate since high power systems have heatsinks, airflow, coldplates and board stiffeners that offer additional avenues for heat dissipation. Also, since only heat conduction in the board is considered, the problem setup is linear and extrapolation can be done for varying currents based on power dissipation in the vias.

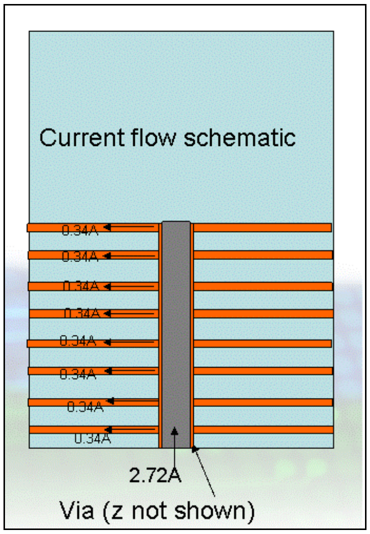


Figure 16 Schematic of current flow (2.72A) from via to multiple voltage planes

Table 6 below summarizes the board heating estimates for varying current flows in the board. The first four rows give results for the configuration in **Figure 15**. The last row is for a case where the module site 70C restriction is removed and instead natural convection and radiation conditions are imposed. Clearly, via current capacity can be significant for a temperature rise of about 10C above the module site. Also note that when the module site temperature of 70C is removed, the via temperature increases by more than 35%. Thus, if an optimized system is desired, it is beneficial to capture the actual boundary conditions in the application.

Table 6 Power bus pad via temperature rise

Current per via (A)	Temperature rise above module site (70C)
2.7	1.7
3	2.1
5	5.7
7	11.3
7 without module site cooling	15.3

Conclusions

Z-interconnect paste easily meets MIL-275D specs for current carrying capacity. Via arrays, or trace or any heat source, quickly spread much of their heat through the board by way of the copper planes. The high thermal conductivity of the copper conducts heat from the source, to every inch of the available board. The shortest cooling path is usually straight out of the board to the air, but it doesn't necessarily conduct the most heat. Other cooling paths can be very significant. For instance, there's a very good cooling path where heat goes out the sides of the heat source, through the dielectric and copper planes of the board. In addition, any actively cooled components such as high power modules can provide cooling paths for heat dissipation. In general, these additional paths improve the path from the heat source to the background temperature so that cooling is much better than just a heat source sitting in ambient air. Due the heat spreading, larger via arrays with constant Amps per via, get hotter since all arrays have nearly the same cooling path, but the total heat increases. Therefore, to specify accurately via current capacity, the cooling environment must be detailed and understood. Standard via current charts, such as MIL-275D, assume a via by itself on a board, which is not typical of real design. Therefore a simple model can be used for a first analysis. Then 3D thermal analysis simulations can be run to get an accurate prediction of temperature vs. current.

References

1. Das, R., Egitto F., and Lauffer, J., "Electrical Conductivity and Reliability of Nano- and Micro-Filled Conducting Adhesives for Z-axis Interconnections" *Proc 56th Electronic Components and Technology Conf*, May 2006.
2. Rowlands, M., Das, R., Lauffer, J. and Markovich, V. "Manufacture and Performance of a Z-interconnect HDI Circuit Card" *Proc IPC-APEX Conf*, April 2008.
3. Jouppi, M. "Current and Conductors" *Printed Circuit Design & Manufacture*, May 2003.
4. Wolbert, B. "Designing P.C. Board Heat Sinks" *Micrel Application Note 17*, 1997.
5. Das, R., and Rowlands, M., "Electrical Performance of an Organic, Z-interconnect, Flip-Chip Substrate" *Proc 57th Electronic Components and Technology Conf*, May 2007.