# Virtual Access Technique Augments Test Coverage on Limited Access PCB Assemblies

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***Abstract***
*Increased pressures to reduce time to market and time to volume have forced many manufacturers of populated printed circuit boards to rely on capacitively coupled, un-powered, vectorless in-circuit test techniques to identify open pins on ICs and connectors. Unfortunately, faster signals and higher-density printed circuit boards (PCBs) have placed pressures on designers to reduce the number of test pads that provide electrical access for vectorless test techniques.*

*A powered-up test solution using boundary scan as the stimulus generator and a capacitive sensor plate for detection can address this loss of access. This virtual access method can quickly and effectively identify connectivity defects between boundary scan based ICs and other devices, including non-boundary scan devices, connectors, and sockets that lack physical test access.*

*This test approach employs a novel set of time domain auto-correlation and cross-correlation algorithms that eliminate many of the restrictions associated with existing frequency domain alternatives. More specifically, this test method does not restrict the operating frequency of the boundary scan's clock signal (TCK) or the number of scan cells in the boundary scan chain. Analyzing the temporal response of a single event pulse in the time domain by use of matched filtering eliminates the need to generate the narrow range of stimulus frequencies that traditional capacitive sensor plate methods require.*

*This virtual test method works with any boundary scan device that complies with the IEEE 1149.1, 1149.4 or 1149.6 standards. A discussion of this test method as well as recent field data, lessons learned and obstacles overcome while implementing this technique on a high-end computer server product at a high volume production facility are disclosed.*

**Introduction**
Detecting open solder connections on printed circuit board (PCB) assemblies continues to be a major challenge on today's manufacturing floor. Capacitive based vectorless techniques such as FrameScan FX$^{TM}$ have met the demand of finding such manufacturing defects on the majority of a PCB's solder connections. Vectorless test is a capacitive based sensing technology whereby a node on the board is excited by a low level sinusoidal signal and a capacitive sensor plate is placed proximate to the IC, socket or connector that is being interrogated for connectivity defects. This technique compares the capacitively coupled resultant signal amplitude against pre-determined test limits to determine whether there is an electrical connection to the device. This vectorless technology has become very popular in the in-circuit test industry due to the simplicity of program development and good coverage results. However, for this technique to be a viable test option, the in-circuit test platform requires electrical access to the component that is being interrogated.

Electrical access has been slowly deteriorating on printed circuit boards in certain market segments for some time now [1]. The affected markets include computing, networking/communications and RF. There are several factors behind this erosion of electrical access on these products. The first issue involves the increase in the PCB component I/O and wiring density and the subsequent move to employ high density interconnect (HDI) technologies on the PCB assembly in order to retain circuit connectivity. HDI boards generally exhibit line widths and spacing that are less than 4 mils with via geometries less than 6 mils and with connection densities greater than 130 pads/in$^2$. In addition, HDI assemblies can have small blind and buried vias and via-in-pad that allow area array packages to be connected on inner layers without exterior PCB layer access, thereby eliminating the possibility of a test pad. With such high board densities, it is simply impractical to place hundreds to thousands of conventional test pads that are 18 mils to 35 mils in diameter on the board for in-circuit test access.

The second driving force that is eroding electrical access is related to the increase in signaling speed on printed circuit board traces. Many signal integrity (SI) engineers are reluctant to place test pads on high speed nets for fear of signal integrity degradation. Placing a test pad on a high speed signal creates an impedance discontinuity on the transmission line that can cause reflections and other signal degradation when the board is operating in mission mode. Test pads, when placed directly on top of the signal etch, can be compensated by placing anti-pads in the reference plane to raise the characteristic impedance at the pad to better match the line impedance, but few, if any SI engineers are willing to undergo the added simulation time and increased board complexity to implement such a compensation scheme.

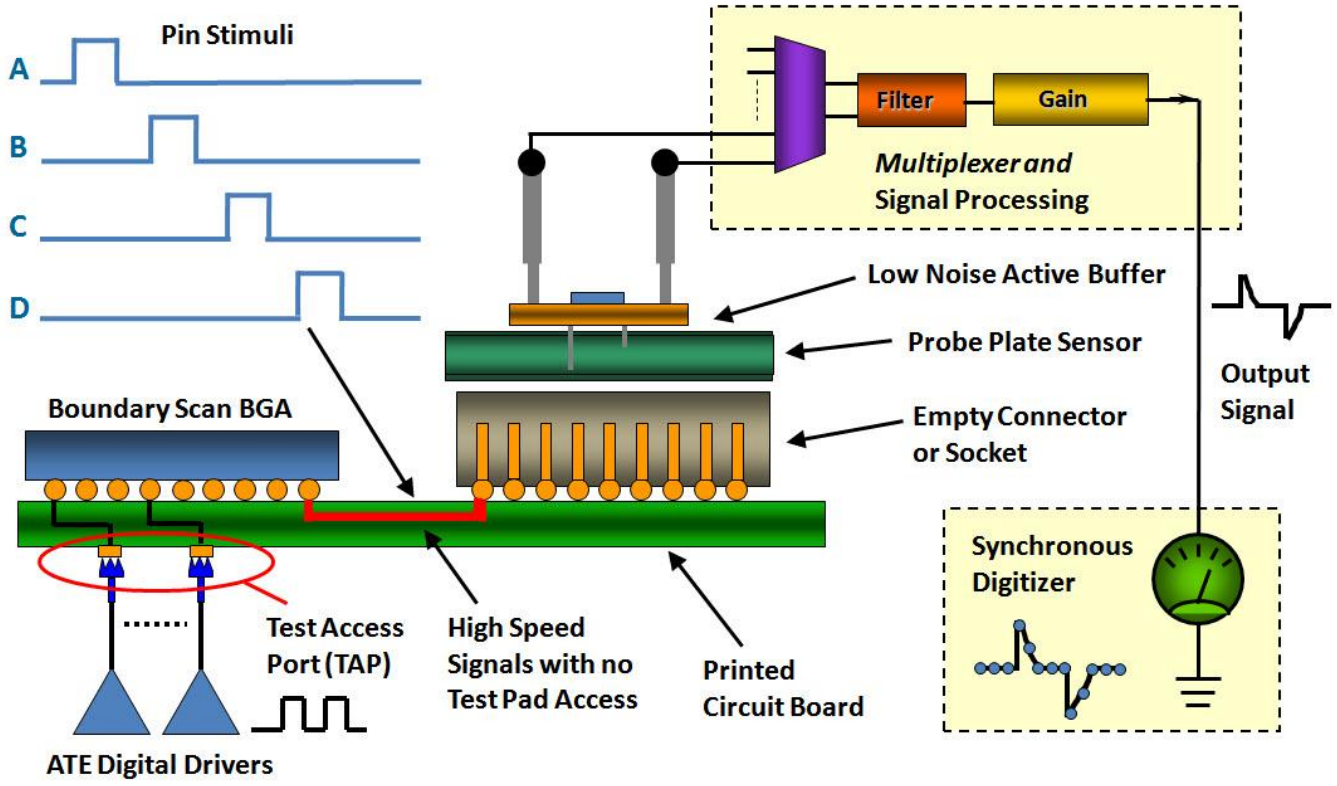


**Figure 1. Block diagram of powered opens technique**

With the increased loss of electrical access on certain PCB assemblies, alternative test methods can be implemented in order to retain test coverage on the assembly. Traditional IEEE 1149.1 boundary scan is one possible solution to the problem. Boundary scan compliant integrated circuit (IC) devices utilize built-in testability structures on the input and output device pins for the purpose of identifying typical process defects including open and shorted connections. Shorts between nets can typically be identified using boundary scan, provided that the pins of the device have self monitoring capability.

Boundary scan devices that are interconnected to other scan devices can readily be tested for connectivity defects, but often times a boundary scan part connects to a socket or a connector that is vacant during the time that the assembly is being tested. These board interconnect scenarios require a different test method to regain fault coverage and pin level diagnostics.

**Virtual Access Test Method**

Powered Opens is a test technique developed several years ago that combines boundary scan and capacitive based opens technologies to create virtual access to PCB signal nets that may not have conventional test point access [2]. With this technique, a boundary scan device acts as an on-board stimulus generator while a capacitive sensor plate provides a means of detecting the resultant test signal. A high level block diagram of this combined test method is illustrated above in Figure 1. In this illustration, the test platform's digital resources are connected to the test access port, or TAP of the boundary scan device. The test system uses the TAP to initialize the device and to generate the required set of test vectors. The output stimulus consists of a single digital pulse per pin that is being tested. Whenever possible, all other pins on the device under test are held at a static logic level in order to isolate the sensor plate from any other on-board signal activity. Each pin that is tested has a unique time slot that is non-overlapping with any other pin activity to eliminate diagnostic ambiguity.

The digital pulse from the boundary scan output pin is capacitively coupled to the sensor plate and is amplified by a local transimpedance amplifier that resides on top of the sensor plate. This signal is then processed through continuous time analog filters, is then digitized and then analyzed in the time domain to determine potential connectivity issues.

There are two basic processes involved in identifying these connectivity defects. The first is called the "learn phase", whereby a known good PCB assembly is tested to acquire the characteristic pin amplitude readings of the assembly during test program development. Typically several known good PCB assemblies are "learned" and an average profile is used as a reference for each connection. The second phase is the actual production test phase whereby boards of unknown quality are tested for open and short defect conditions using pass/fail thresholds that have been calculated from the learn phase.

**Domains of Testing**

The boundary scan device that is used as an on-board stimulus generator can supply a repetitive signal such as a square wave, or a non-repetitive signal that can be a rising edge, a falling edge, or a pulse that combines the two edges. The signal analysis of the resultant signal can be performed in the time domain, or in the frequency domain. As a result, there are four possibilities in terms of signal generation and signal processing. The method described in this paper uses a non-repetitive pulse that is analyzed in the time domain because this combination offers a number of benefits over the other combinations as detailed below.

Most vectorless capacitive opens test methods use a repetitive sinusoidal signal that is then processed in the frequency domain. The test frequency that is applied to the device under test is in the narrow range of approximately 8KHz to10KHz. Applying a lower test frequency results in lower resultant signal amplitude that will ultimately decrease fault coverage. Signal frequencies above 10KHz will yield a larger signal, but can cause signal coupling between the printed circuit board and the sensor plate. The result is an increase in the quantity of false pass opportunities because the sensor plate is receiving signal strength from the board as well as from the tested component on the PCB.

Frequency based testing, when applied to powered opens has a fundamental limitation in being able to successfully synthesize the minimum desired pin toggle frequencies under all board conditions. The reason for this is that the maximum boundary scan output pin toggle frequency is approximately equal to the boundary scan clock (TCK), divided by two and also divided by the number of scan cells that are active in the boundary scan chain (see Equation 1 below).

$$\mathbf{F_{toggle}} = \frac{\mathbf{TCK}}{\mathbf{2 \cdot (Number\ scan\ cells)}}$$

**Equation 1. Boundary scan output pin toggle frequency**

If, for example the boundary scan clock is operating at 2MHz, then a boundary scan chain with more than 125 scan cells will lower the pin toggle frequency below the desired 8KHz envelope. Increasing the frequency of the boundary scan clock is one possible solution, but specialized fixture electronics may be needed to deliver a clean clock signal to the board under test. In addition, today's devices that contain boundary scan can contain many hundreds of scan cells and the I/O count is predicted to increase in the future [3]. Utilizing a single event pulse to excite the device under test mitigates the dependency between the number of scan cells in the chain and the pin toggle frequency because the test is not constantly re-loading the scan chain to drive alternating one and zero patterns to an output pin to generate many cycles of a square wave test signal.

A second advantage of using a single pulse rather than a periodic signal is that the throughput is improved. Figure 2 shows families of throughput curves as a function of the number of scan cells in the chain and the percentage of scan cells that are

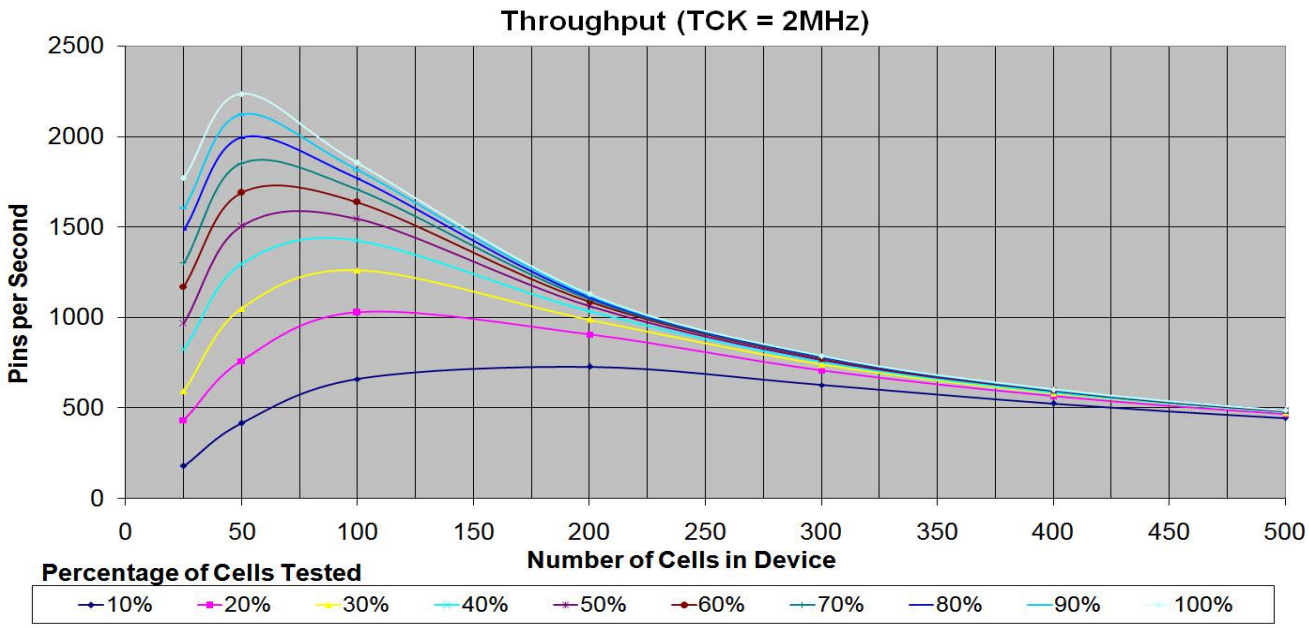


**Figure 2. Powered opens throughput in pins tested per second**

actually being tested using a 2MHz TCK signal. In many instances, the number of pins per second that can be tested is much greater than the traditional un-powered analog opens techniques which can typically test 500 pins per second.

**Signal Analysis**

A method of "matched filtering" correlates a known signal or template with the measured signal that is in question. Matched filters offer the maximum achievable signal to noise ratio (SNR) in the presence of white noise and are commonly implemented by cross correlation methods (Equation 2, second term) [4]. This signal processing technique can be found in radar signal processing and is used in this pulsed version of powered opens signal processing as well.

Equation 2 details the auto correlation and cross-correlation functions where X(i) and Y(i) are the respective learned and production data vectors, Mx and My represent the mean values of these digitized data vectors and R(d) is the correlation coefficient that denotes the likelihood that the measured pin signal matches the learned reference signal in both temporal response and in magnitude.

As part of the "learn" process during program development, multiple de-normalized auto-correlation values are calculated from the digitized data vectors for a pin and are averaged to create a reference autocorrelation coefficient and a reference data vector for the production floor cross correlation operation. The auto correlation section of the analysis also allows one to calculate the mean and standard deviation of a number of auto-correlation values to ensure that there is not excessive variation due to noise. Should there be excessive variation as indicated by a standard deviation value that is large, as compared to the mean value, the pin will be discounted from the test because the pin thresholds cannot reliably be set.

The digitized data for a pin is sorted out from the digitizer's memory and reconstructed into a single long data vector ($X_{(n)}$). This vector is created by simply placing the negative edge data samples directly after the last data point of the positive edge data samples.

$$\mathbf{R_d} = \sum_{i=1}^{N-1} [\mathbf{X_{(i)}} - \mathbf{M_X}] \cdot [\mathbf{X_{(i)}} - \mathbf{M_X}] \qquad \mathbf{R_d} = \sum_{i=1}^{N-1} [\mathbf{X_{(i)}} - \mathbf{M_X}] \cdot [\mathbf{Y_{(i)}} - \mathbf{M_y}]$$

**Equation 2. Denormalized autocorrelation and cross correlation, respectively**

During production testing, if the de-normalized cross-correlation value (Rd) is either less than or greater than the learned de-normalized auto-correlation value by a certain percentage, then the pin is then deemed to be defective, otherwise the connection is considered a good one. The correlation technique that is described is very resistant to random noise in the signal which dramatically helps to reduce false calls on the manufacturer's production floor.

**Lessons Learned in Production**

As the name implies, powered opens is a test technique where at least a part of the board is powered up to allow the boundary scan devices to function. As a result, the PCB is considerably noisier than the traditional unpowered capacitive opens counterpart. As part of the test program development, it is important to minimize as much unwanted board activity by inhibiting or disabling items like crystal oscillators, phase locked loops, and un-needed switching power supplies.

Secondly, good fixturing practices are vital for the success of any of the powered opens technologies. Specifically, the sensor probe plate needs to land consistently and reliably on the target device to be tested. This is especially true in the case of high pin count LGA processor sockets. In order to ensure this action, it was necessary to re-design the sensor plate and have the hangers attach directly to the plate rather than the buffer amplifier and to increase the number of hangers that attach the probe plate to the test fixture This change is illustrated in Figure 3.

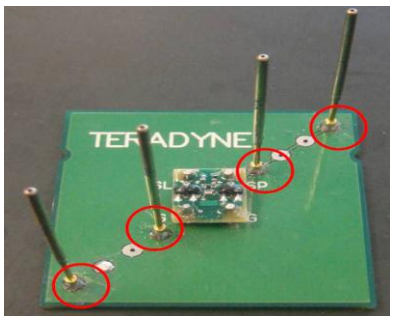


**Figure 3. Powered Opens sensor plate**

**Powered Opens Performance**

The following section details some of the key performance metrics that were recorded on the LGA 1366 processor sockets on a server motherboard. The first metric that was evaluated relates to the repeatability of the measured pin values (when connected or open) across twenty three PCB assemblies and across three different operators. Referring to the left half side of Figure 4, the properly connected pins of all 22 boards are very tightly grouped and are very consistent in amplitude. The same is also true for the faulted pins shown at the bottom of the graphic. Note that the measured difference between a good and a faulted pin is greater than 12 to 1, allowing for easy fault identification. The boards were re-run a second time, as shown on the right half of the illustration and again, there was very good consistency between good pins and also with the open pin group. Using three different in-circuit operators to perform the tests (operators A, B and C) had no observable effect on the measurements indicating that there is no operator influence on the test outcome.

A second metric deals with the standard deviation of the pin measurements and is an indicator of the relative amount of noise in the measured values. Referring to Figure 5, the independent axis depicts the pin number on the socket, while the dependent axis plots the ratio of the standard deviation to the mean pin value. This metric is an indicator of the noise to signal ratio and the lower the number, the better the repeatability of the measurements. As shown in the Figure, the average sigma/mean ratio is only 1% on average, which demonstrates how well the matched filtering via correlation techniques can reject board noise.

The next metric to discuss is the process capability, of the CPK of the pin measurements. CPK, as defined in Equation number 3, is inversely proportional to the standard deviation, or variability, of a specific process or measurement.

$$\mathbf{CPK} = \mathbf{Min}[[\frac{\mathbf{USL} - \mathbf{mean}}{\mathbf{3} \cdot \sigma}], [\frac{\mathbf{mean} - \mathbf{LSL}}{\mathbf{3} \cdot \sigma}]]$$

**Equation 3. Process capability of measurement system**

The higher the value of a Cpk, the narrower the process distribution is as compared to the specification limits, and the less likely a false indictment of a pin will occur during production test. Most process engineers prefer a CPK of greater than 1.4 for a double sided test limit. Theoretically, a CPK of 1.4 infers that the false call rate will be about 27 parts per million. The production tests on the LGA 1366 processor sockets performed very well with an average CPK of 10.0. Note that it is possible to artificially generate a high CPK value by simply increasing the upper and lower test limits. In this powered opens technique, the test limits are set within +/-30% of the average pin measurement to ensure that there will be few, if any false pass opportunities. These tight test limits also ensure that the CPK Figure is not inflated and is a realistic calculation.

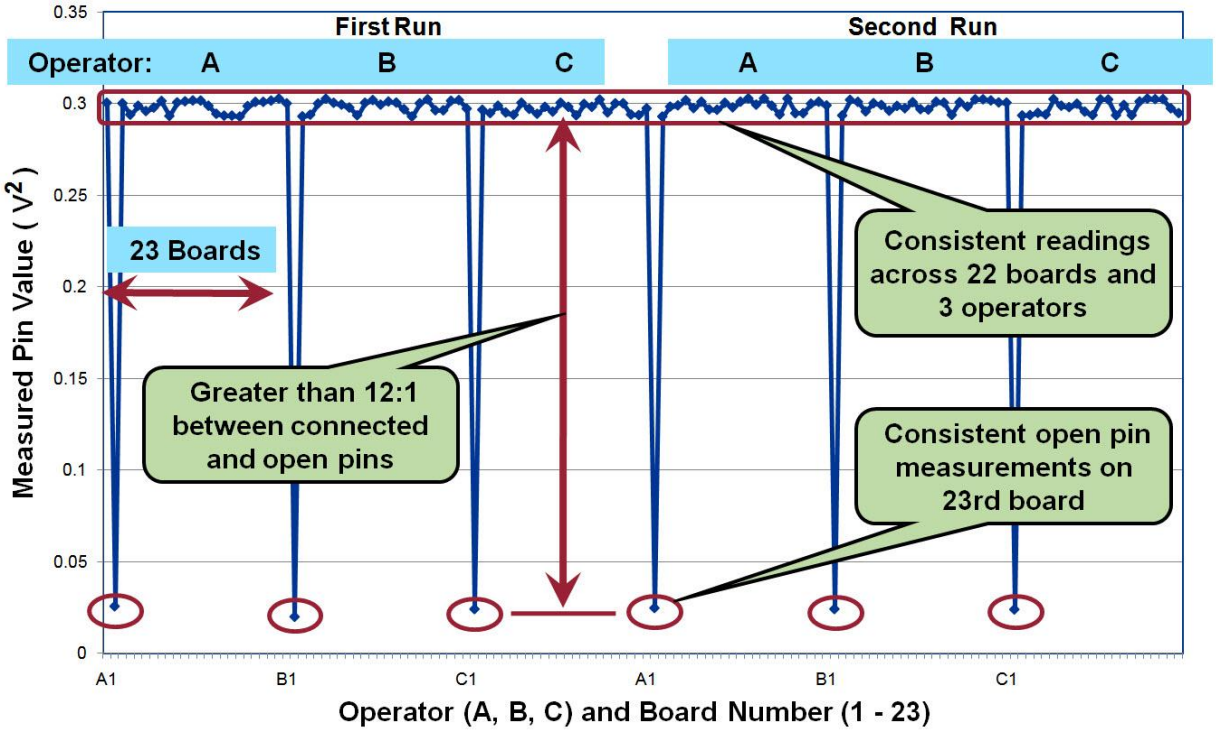


**Figure 4. LGA 1366 socket pin measurements**

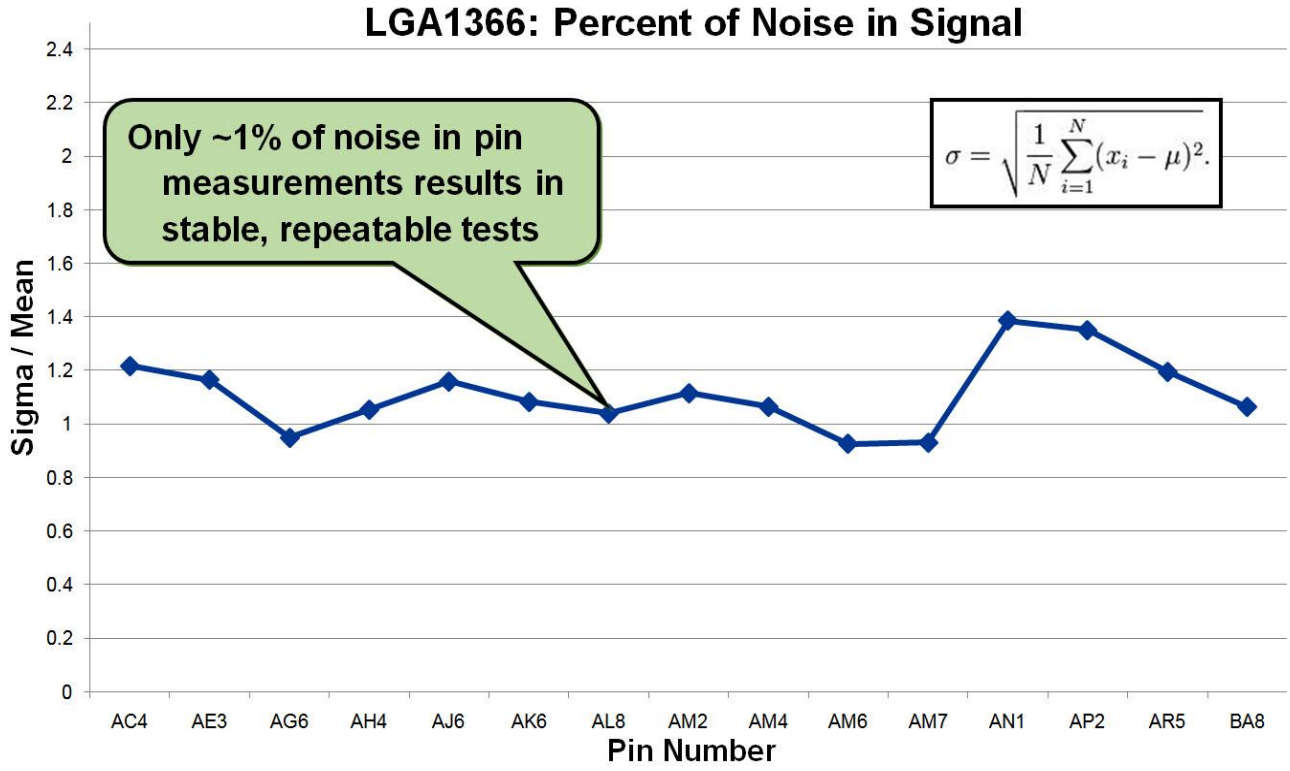


**Figure 5. Standard deviation to mean ratio for pin measurements**

**Technique Limitations and Future Solutions**

Although the combination of capacitive opens and boundary scan can increase coverage on boards with density issues that cannot afford large test pads or on boards with high speed nets, there are several limitations that need to be mentioned.

The first limitation is that the boundary scan component pins can act as a stimulus source only if the pin is either an output pin or a bi-directional pin. As a result, nets that connect to boundary scan inputs are un-testable with this method.

A second limitation relates to differential signals and fault diagnostics. If one of the two signals that comprise a differential pair is open, there will be a discernable signal change that can be used to diagnose an open pin condition on one of the two nets. If both pins are connected, the signals cancel each other and the capacitive detection scheme measures virtually no signal. The same "no signal" condition is also detected if both pins of the signal pair are open. As a result, a fault class of both nets open cannot be distinguished from a condition when both nets properly connected.

However, a recently balloted IEEE P1149.8.1 standard proposes enhancements to the boundary scan standard by adding new capabilities that will solve the above mentioned limitations with regard to input pins and differential signal diagnostics [5]. This same proposed standard also describes a solution that will effectively decouple the earlier described dependency of a boundary scan pin toggling frequency to the boundary scan chain length.

**Conclusion**

Powered opens allows for virtual access on high density PCB assemblies where there is limited board real-estate for test pad access and on high speed PCB signals that cannot tolerate the negative effects of electrical test pads.

Matched filtering from cross correlation offers the maximum possible signal to noise ratio in a noise-prone powered up environment and minimizes the opportunity for false calls on the production line. Production data from LGA1366 sockets on server boards confirms that the pulse based test method is very capable in terms of noise immunity, throughput, repeatability and false call rate.

When using time domain edge analysis instead of the more traditional frequency domain analysis, there are no restrictions on the number of scan cells in the chain. As a result, the time domain technique can identify common process defects and is compatible with present and future boundary scan compliant silicon devices.

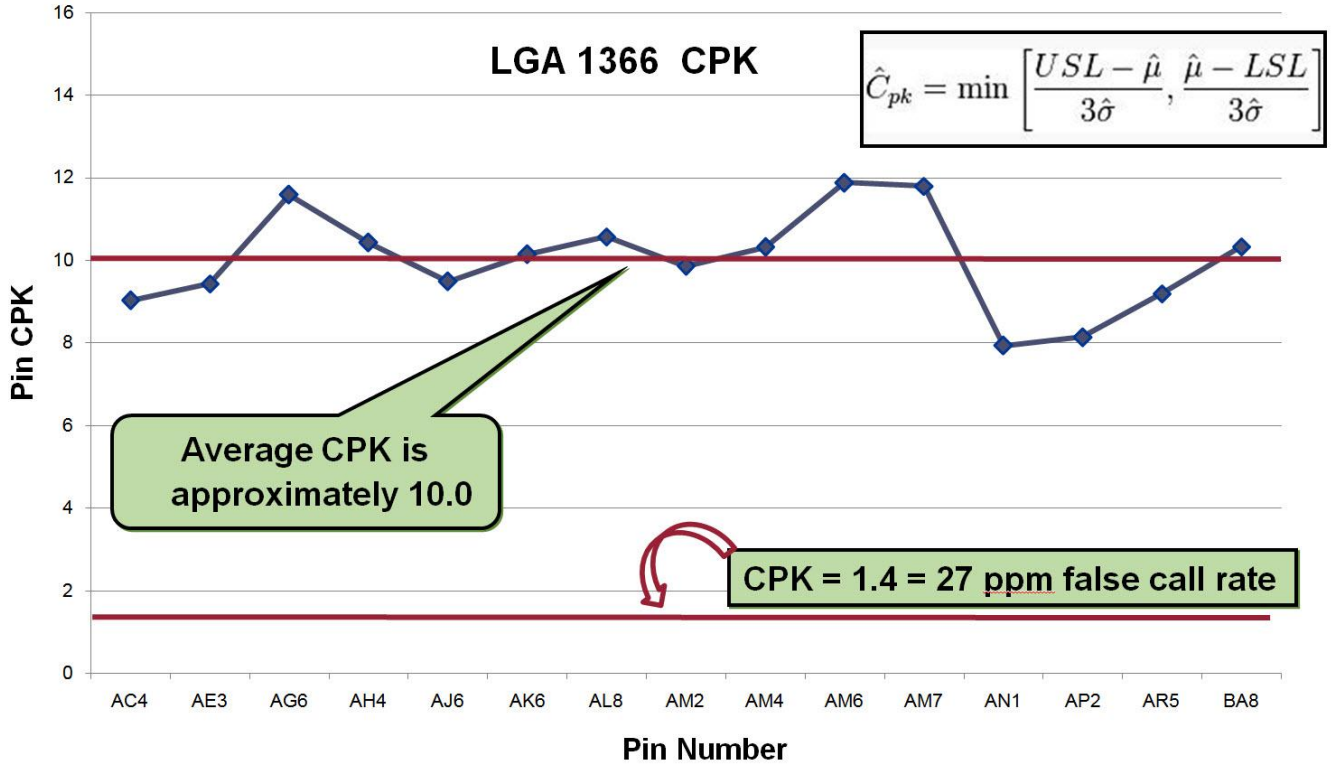


**Figure 6. Process capability of LGA 1366 processor socket**

**References**


[1] iNEMI, “Test, Inspection, and Measurement”, Roadmap, 2011. www.inemi.org.

[2] Anthony J. Suto, “Power to the Opens”, Test & Measurement World, May 2010, pp33-37.

[3] iNEMI, “Test, Inspection, and Measurement”, Roadmap, 2011, pp13. www.inemi.org.

[4] George L. Turin, “An Introduction to Matched Filters”, IRE Transactions on Information Theory, pp. 311-329, June, 1960.

[5] IEEE, P1149.8.1, “Draft Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components”, http//grouper.ieee/groups/1149/atoggle/


# Virtual Access Technique Augments Test Coverage on Limited Access PCB Assemblies

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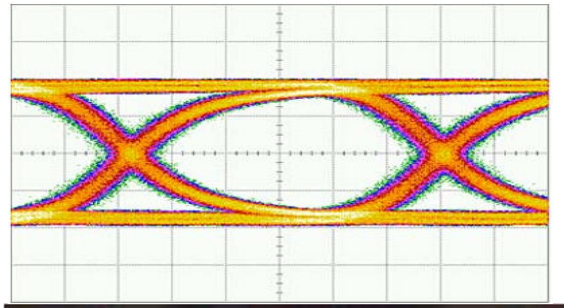
**2012 Apex Expo**

# Outline

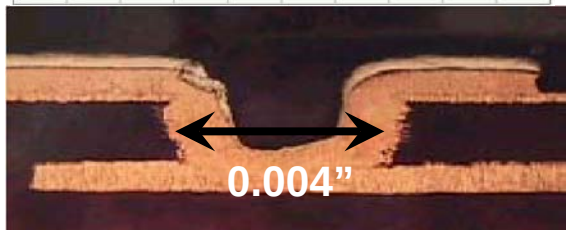
- Industry PCB trends
- Powered Opens Description
- Tradeoffs in Powered Opens Techniques
- Production Data
- Limitations and Future Solutions
- Summary

# Trends Causing Loss of Electrical Access

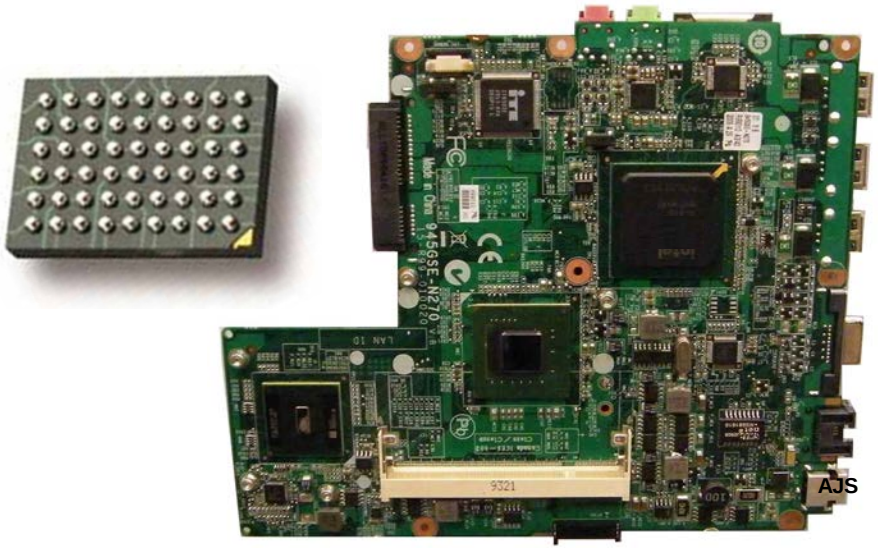
- Higher speed signaling



- HDI on PCB assemblies




- Area array packaging



- Board miniaturization

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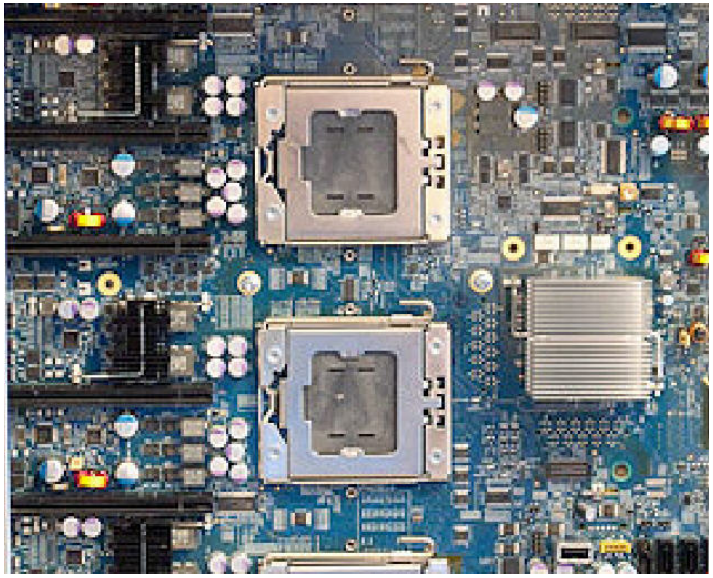
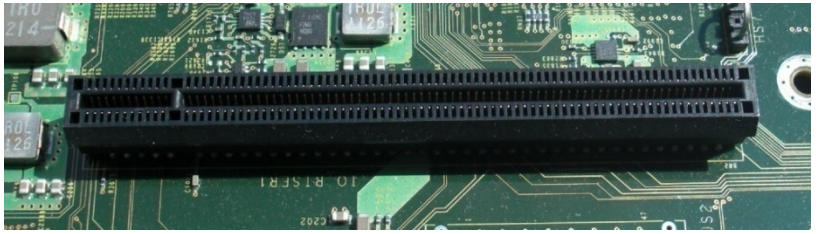
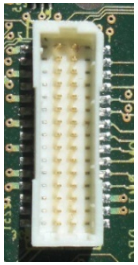
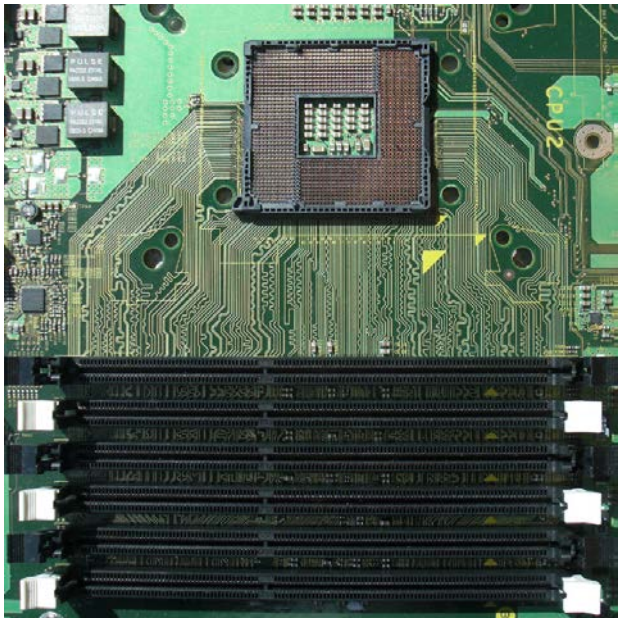
# Boundary Scan Nets to Vacant Sockets and Connectors

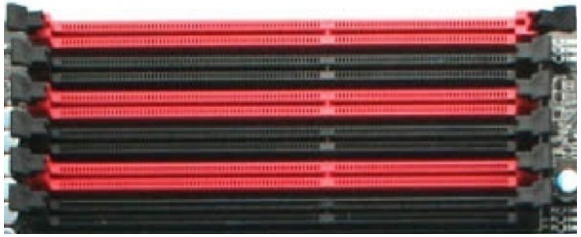


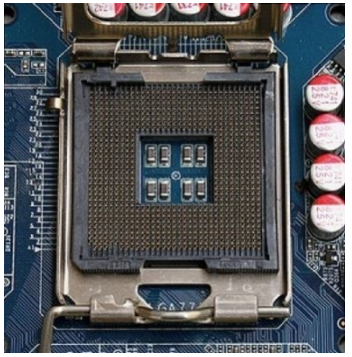


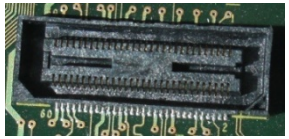
How to test ?





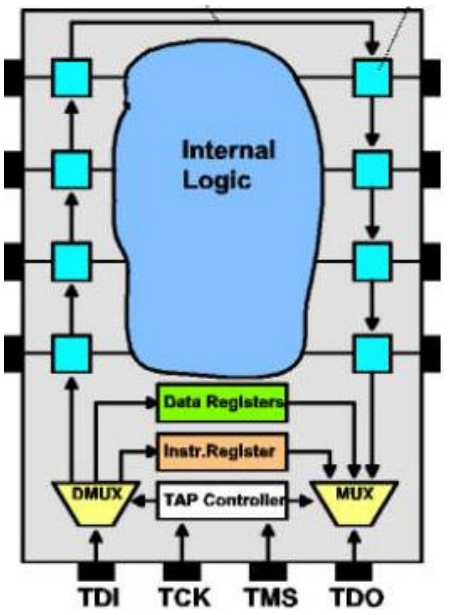


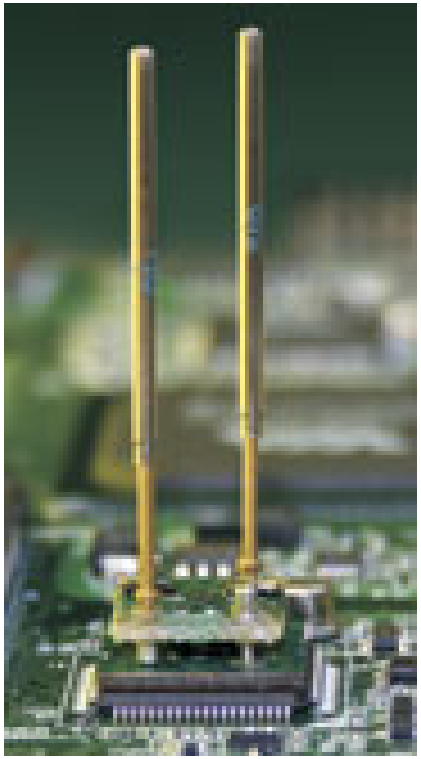




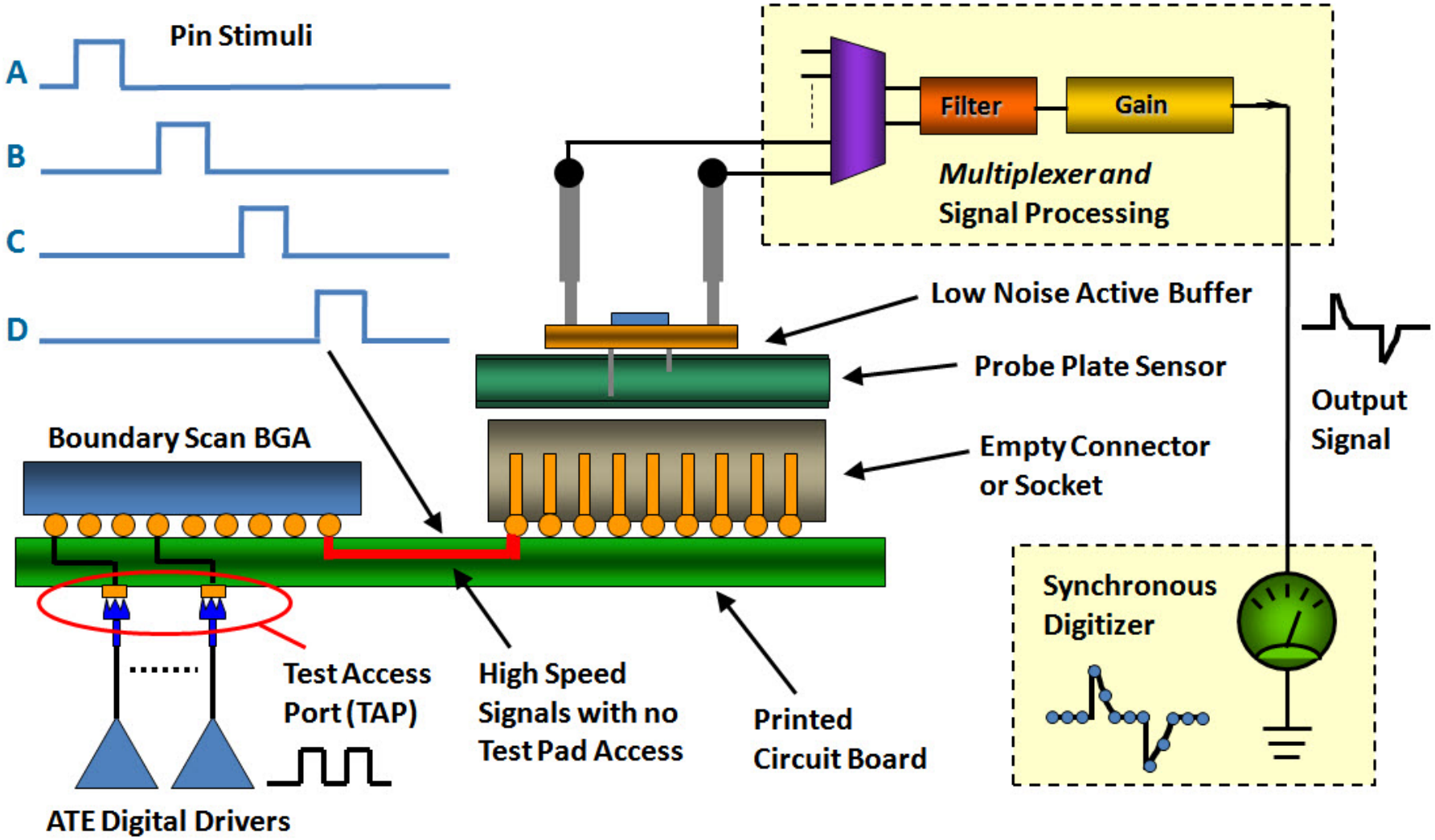
# Powered Opens Solution

- Combines boundary scan and vectorless techniques
- Uses Boundary scan devices as digital stimulus
- Signal detection uses capacitive based technology
- Gains ***virtual access*** to identify opens on connectors, sockets and IC devices
- Helps retain testability on densely populated PCB assemblies and on high speed signals



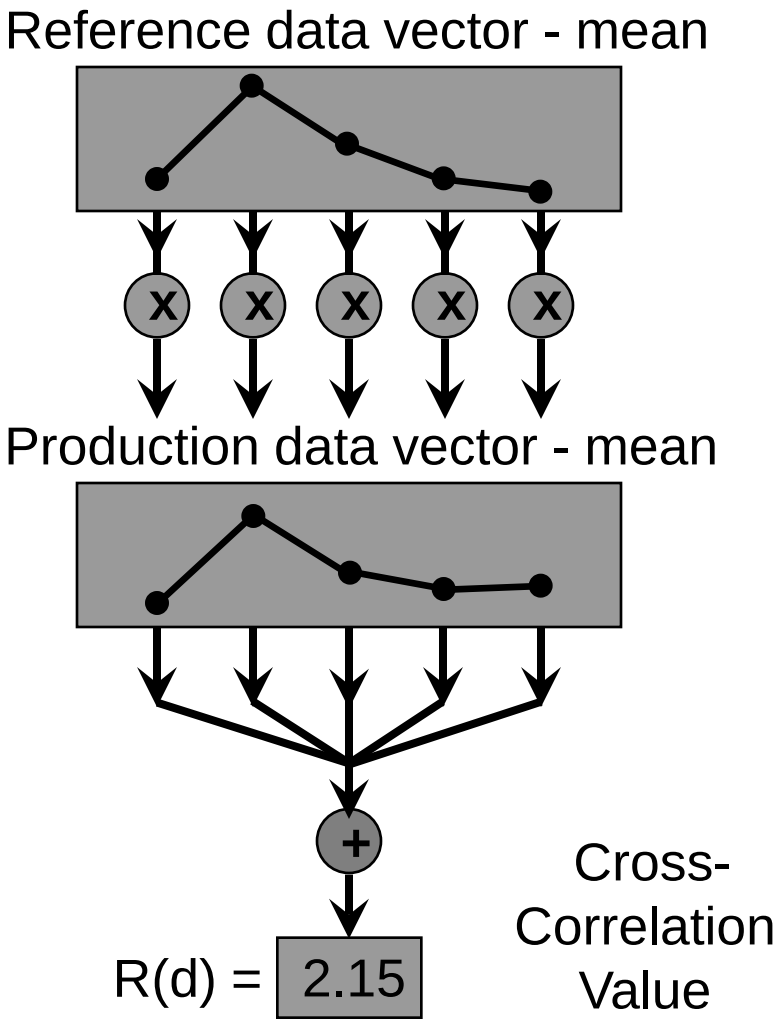
# Functional Block Diagram



# Matched Filtering via Cross Correlation

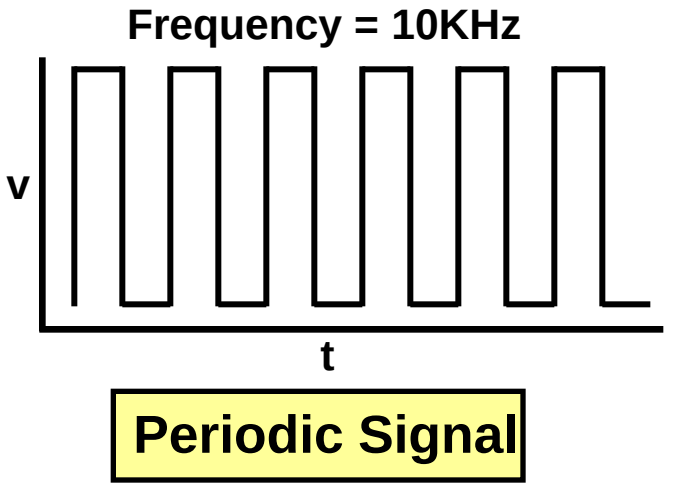
$$R(d) = \Sigma [ X(i) - Mx ] \times [Y(i - d) - My ]$$

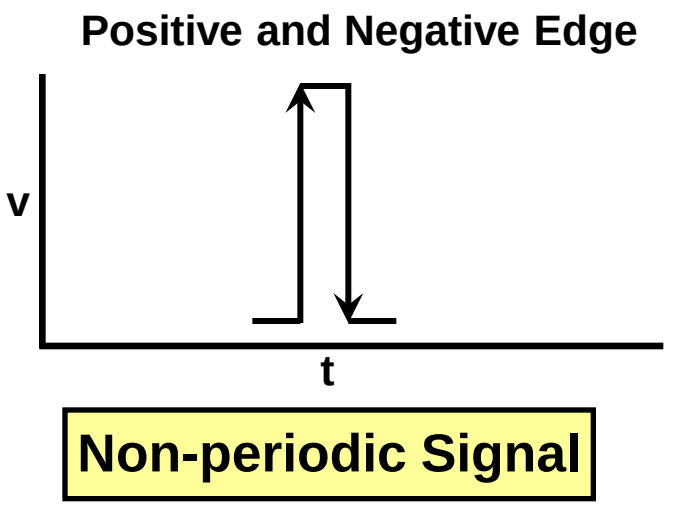
- Uses a single pulse to test each pin connection
- During the learn phase, many pulses are synchronously digitized, point-by-point averaged and a reference data vector is created along with an autocorrelation value
- During production, the pin data vector is cross-correlated with the averaged reference data vector
- The production correlation coefficient is compared against high and low test limits relative to the learned autocorrelation value to determine pin connectivity



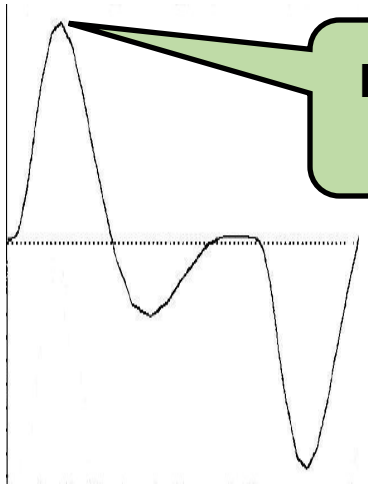
# Why not Use Frequency Based Testing?

- Conventional opens techniques using frequency domain analysis require a test frequency of about 10KHz
- Frequency at IC's cell output linked to TCK frequency
  - Approximately (TCK/2) / (number of cells in the chain) + overhead
- Typical ICT tester clock capabilities:
  - ~ 2MHz clock without fixture electronics
- Large cell devices or chains may become un-testable using frequency technique
  - ~ 100 cell scan chain maximum limit @ 2MHz



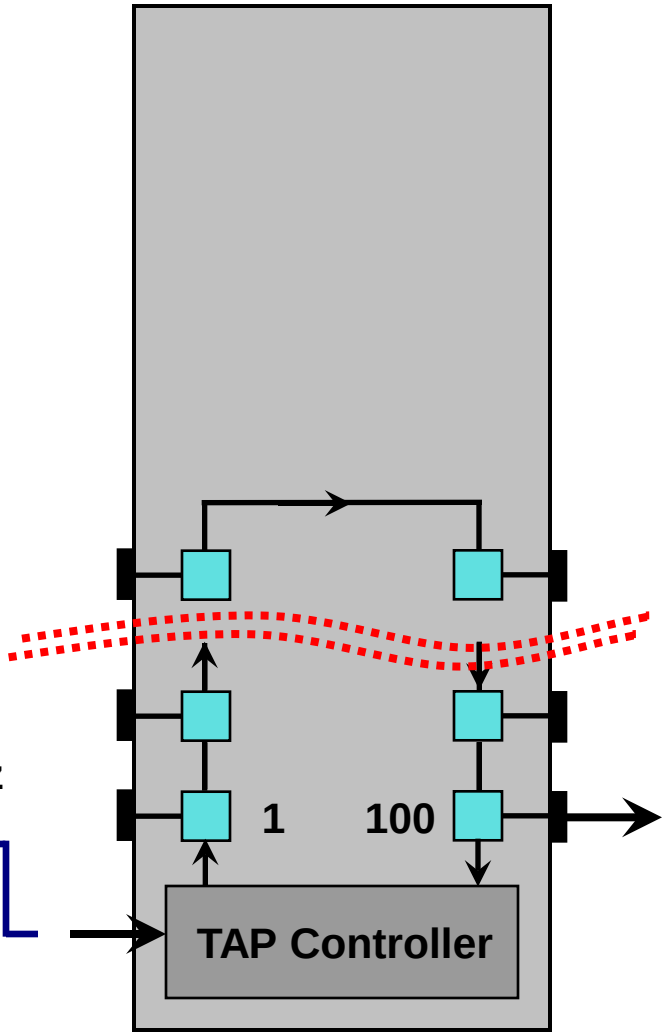



# Frequency Testing with 100 Scan Cells



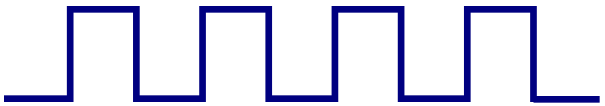
Large signal and good coverage

Part of mux output signal



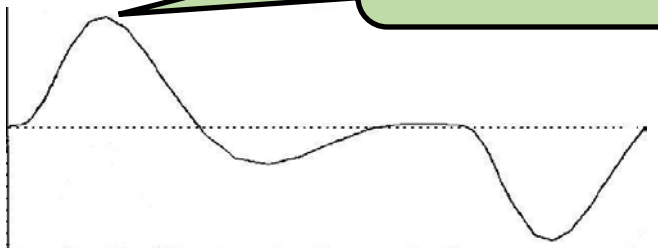

TCK = 2MHz

F toggle = 2MHz/2 / 100 = 10 KHz



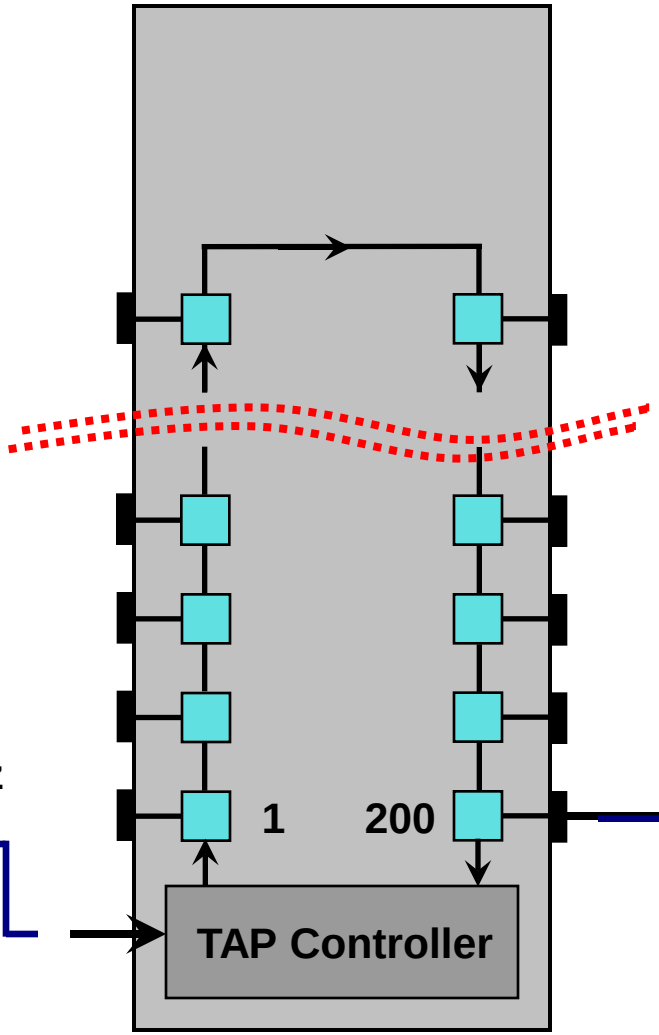
# Frequency Testing with 200 Scan Cells

Smaller signal and lower coverage



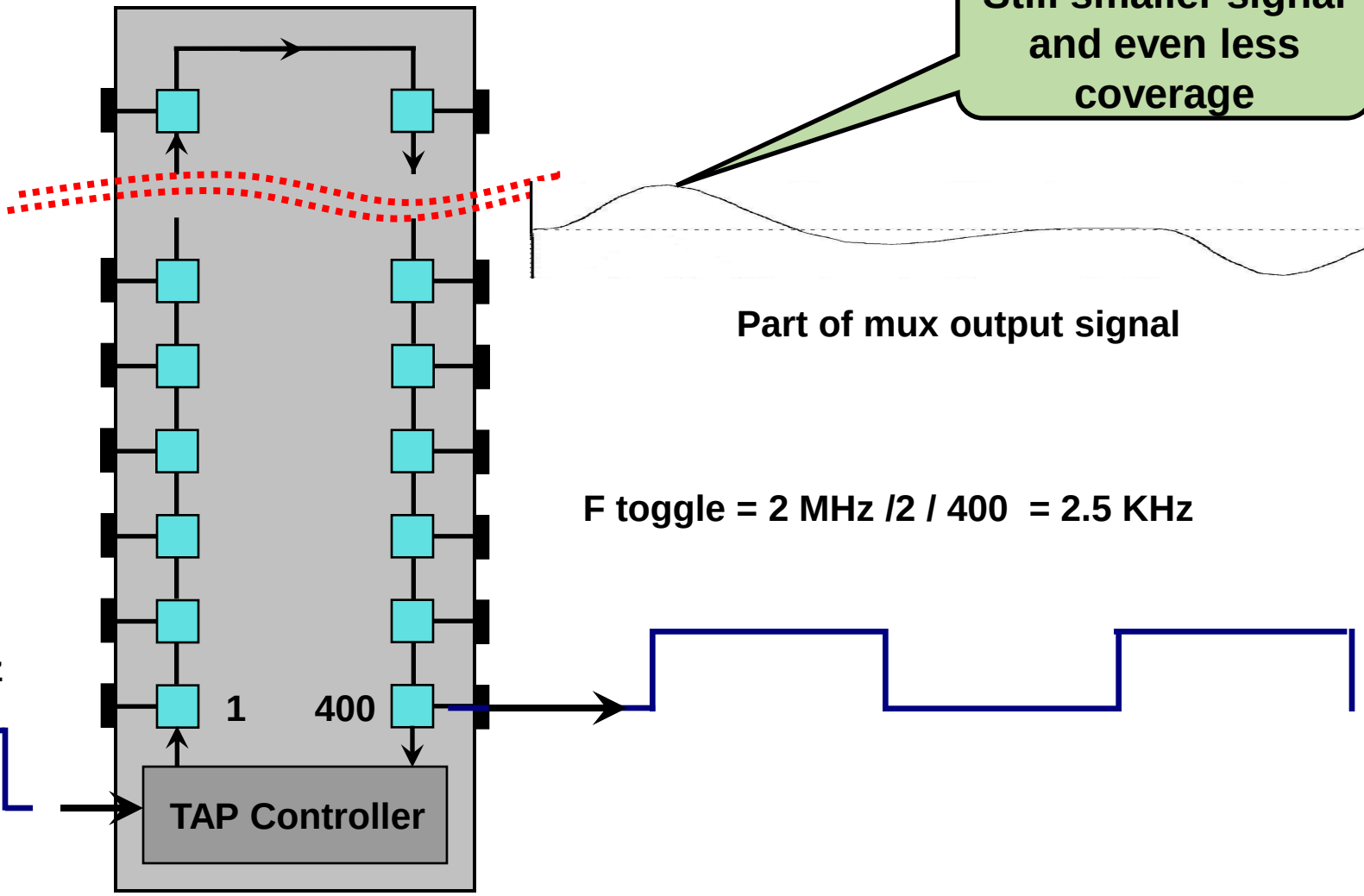
Part of mux output signal

F toggle = 2 MHz/2 / 200 = 5 KHz

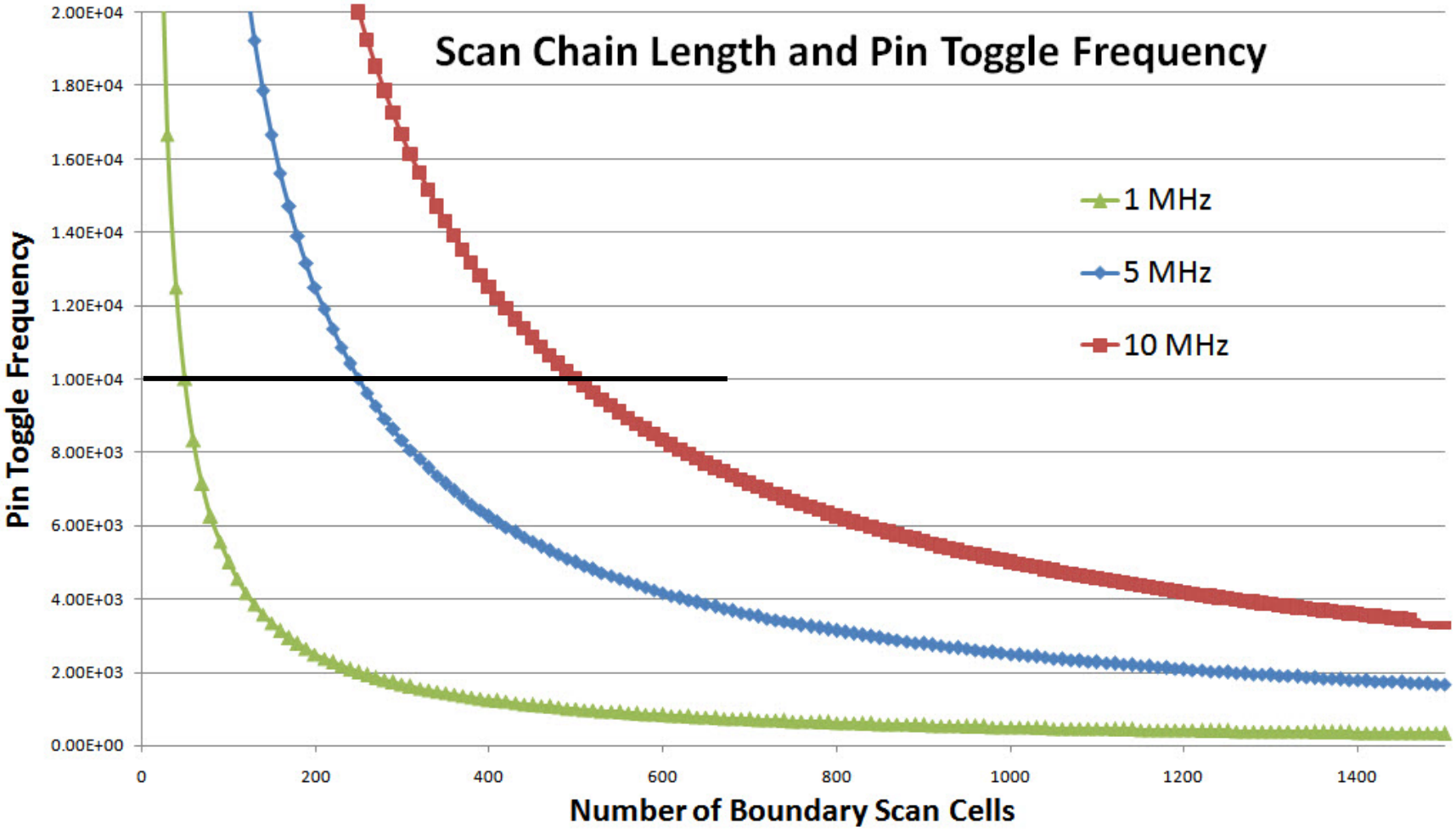



TCK = 2MHz

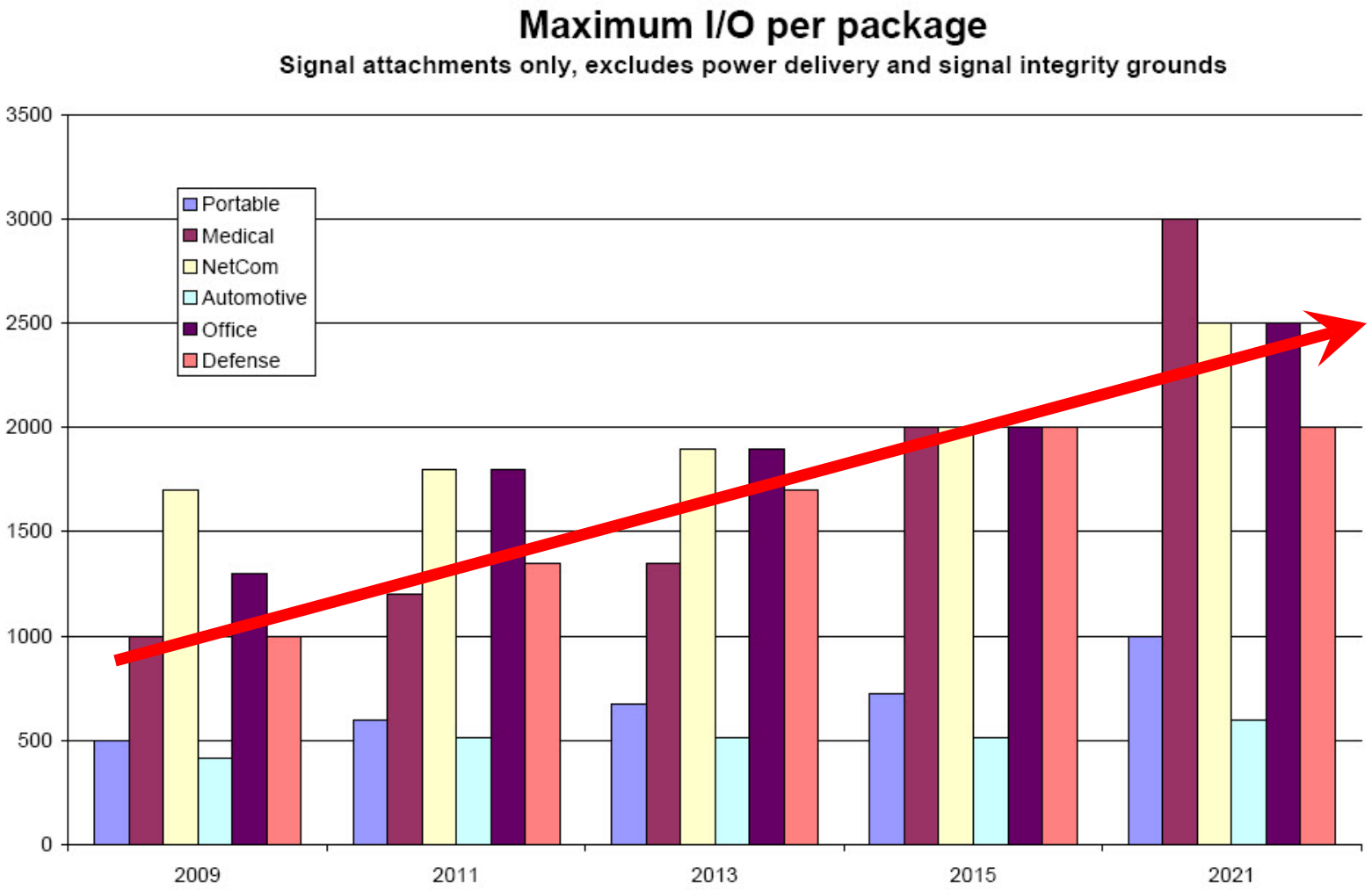
# Frequency Testing With 400 Scan Cells



# Scan Chain Effect on Toggle Frequency



# IC I/O and Cell Count is on the Rise

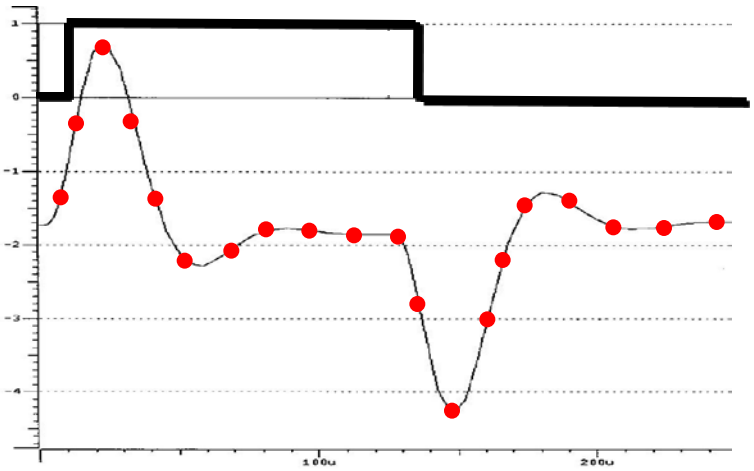



Source: iNEMI 2011 Test and Inspection

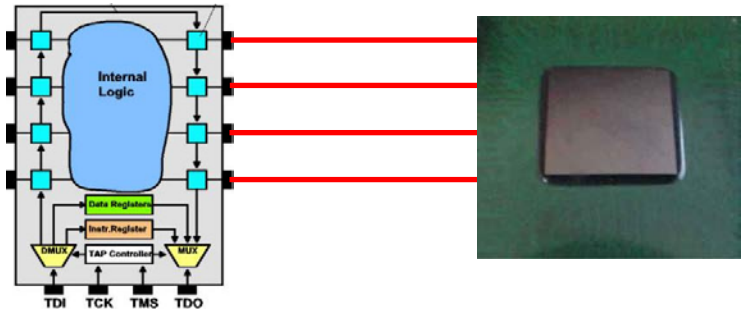
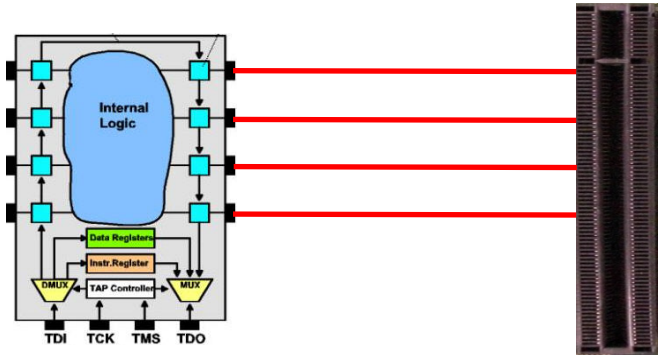
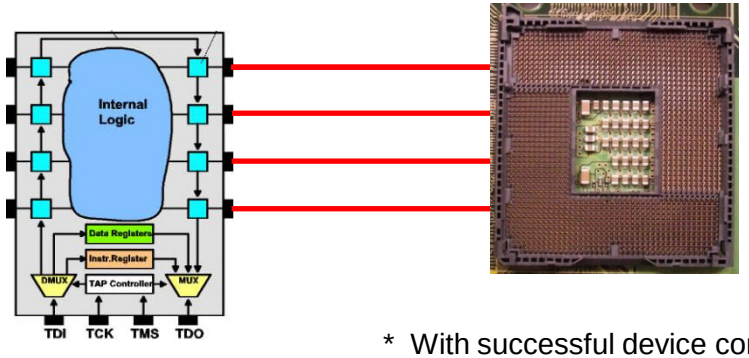
# Time Domain / Edge Detection Method

- Key Benefits
  - No dependence upon output toggle frequency when analyzing the temporal response of edges only
  - No restrictions with the number of scan cells in boundary scan chain
  - Technique operates with today's existing silicon, no need for custom, non-standard silicon or added tester / fixture hardware

$$r(d) = \frac{\sum_i [\,(x(i) - mx) * (y(i-d) - my)\,]}{\sqrt{\sum_i (x(i) - mx)^2}\sqrt{\sum_i (y(i-d) - my)^2}}$$



# Resolves Some Boundary Scan Limitations

| | | Test Coverage? BS | Test Coverage? PFS |
|---|---|---|---|
| Boundary Scan IC to Standard IC |  | Maybe | Yes* |
| Boundary Scan IC to Connector |  | No | Yes |
| Boundary Scan IC to Socket |  | No | Yes |



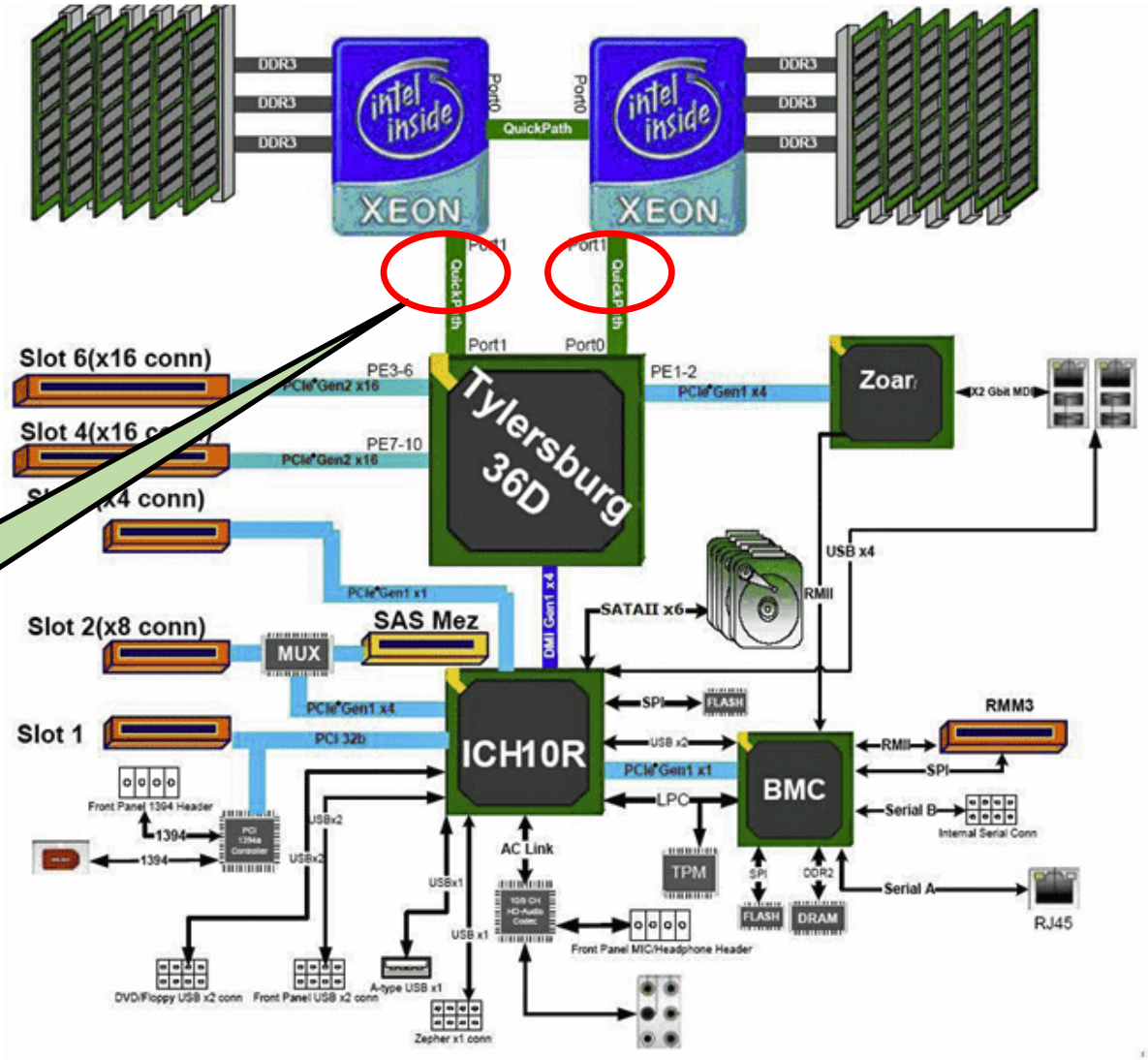
* With successful device conditioning/disabling

# Powered Opens Test Case

# High End Server Application

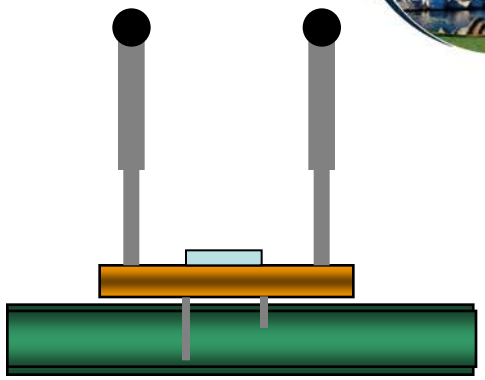
- Dual Nehalem processors with LGA1366 sockets
- Tylersburg IOH with boundary scan capability

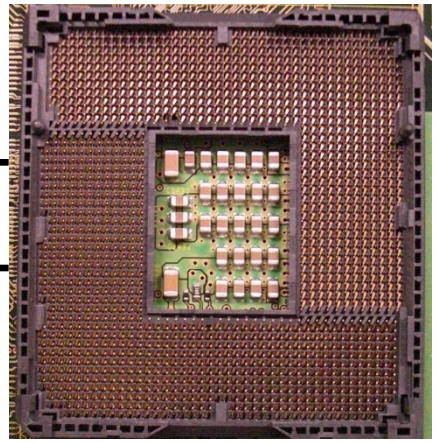
**Testing the QPI busses for connectivity**

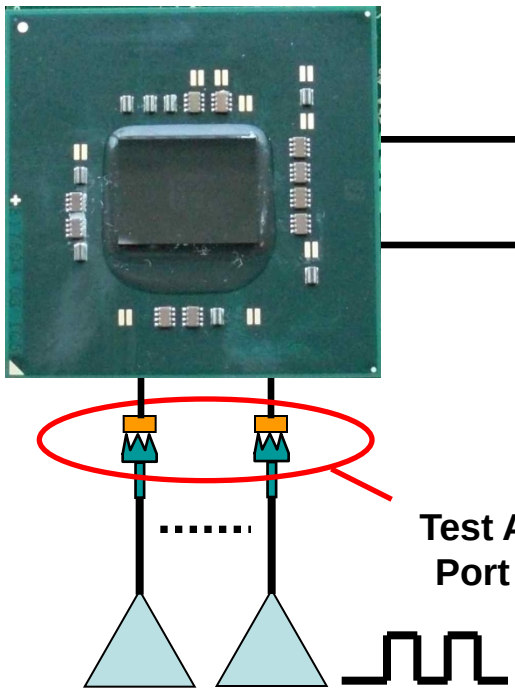


# LGA 1366 Socket

Server board processor socket

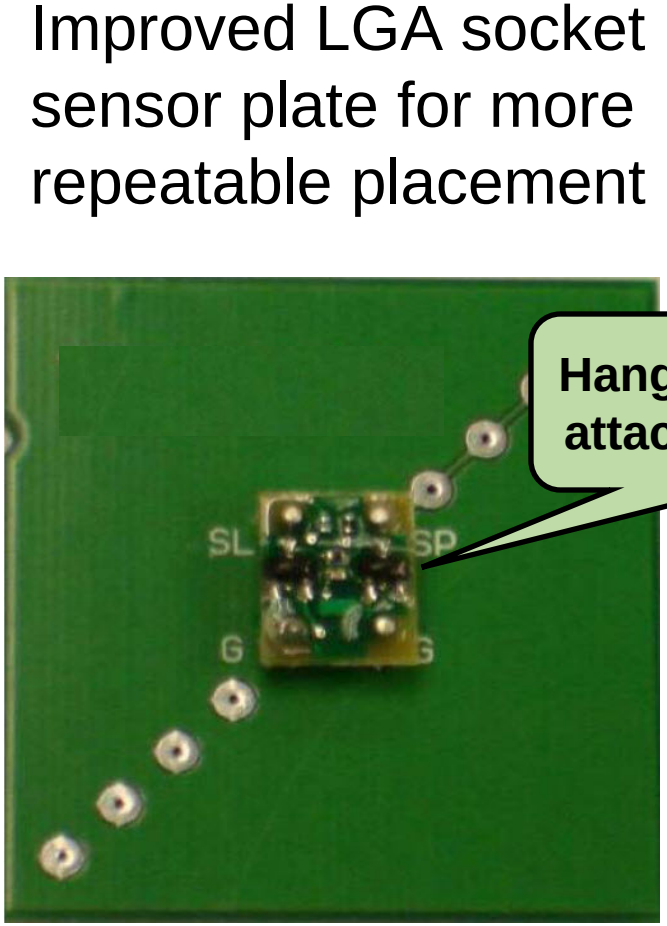




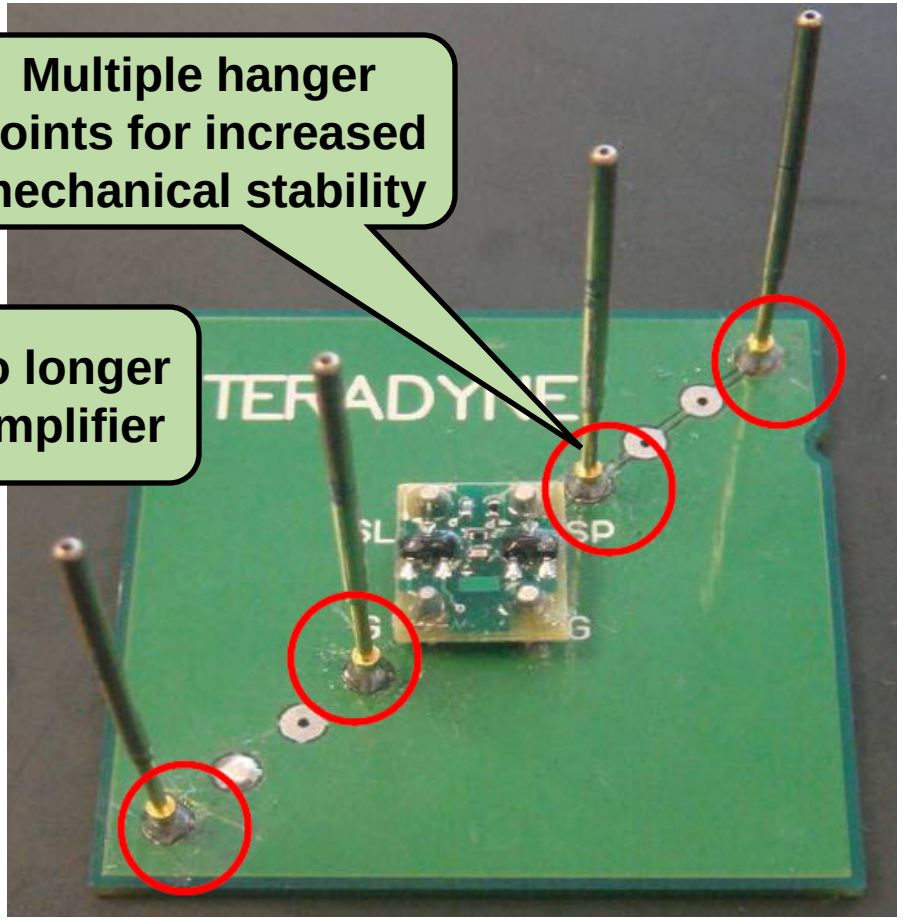


# Sensor Plate Technology

- Improved LGA socket sensor plate for more repeatable placement

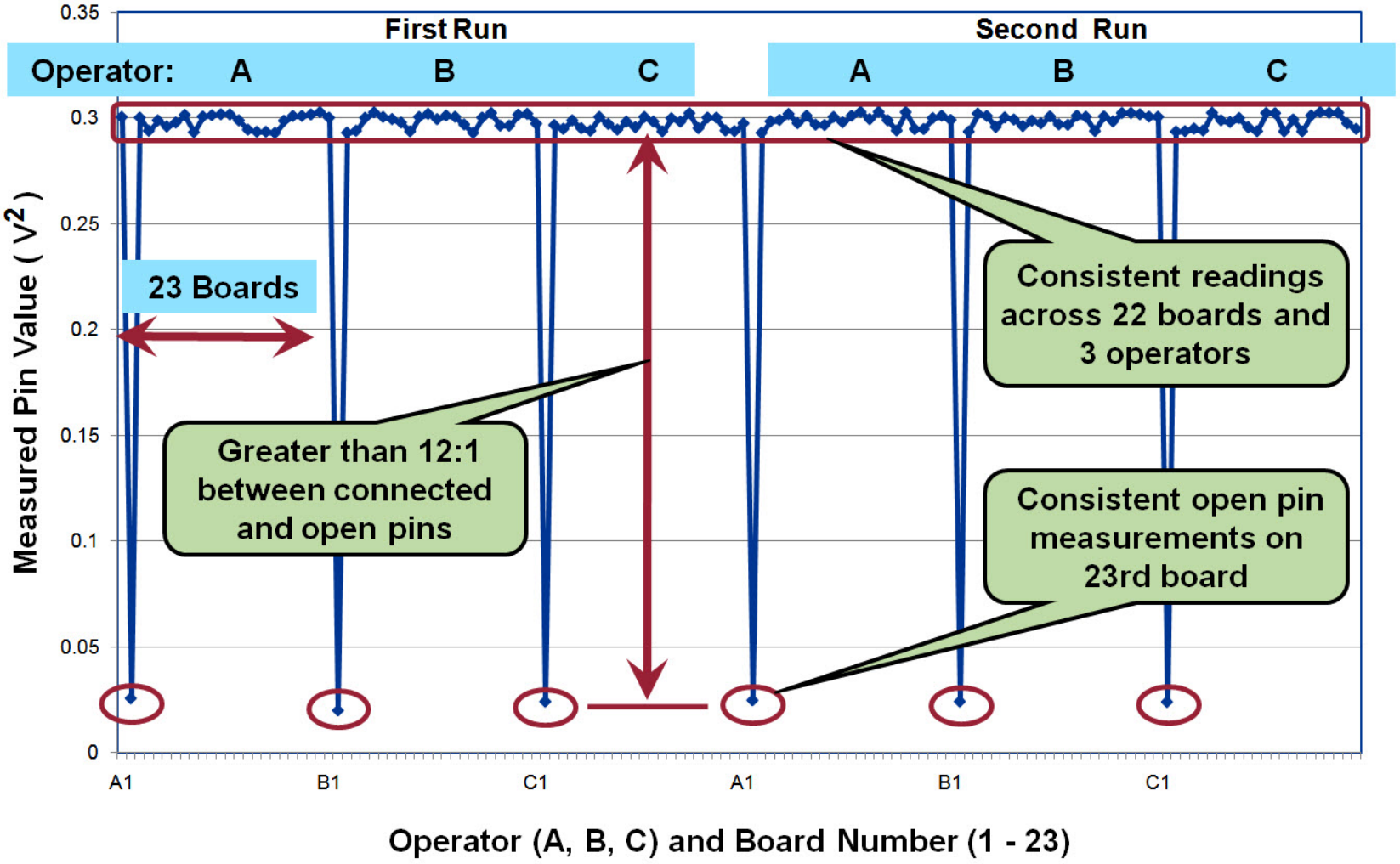



Hangers no longer attach to amplifier

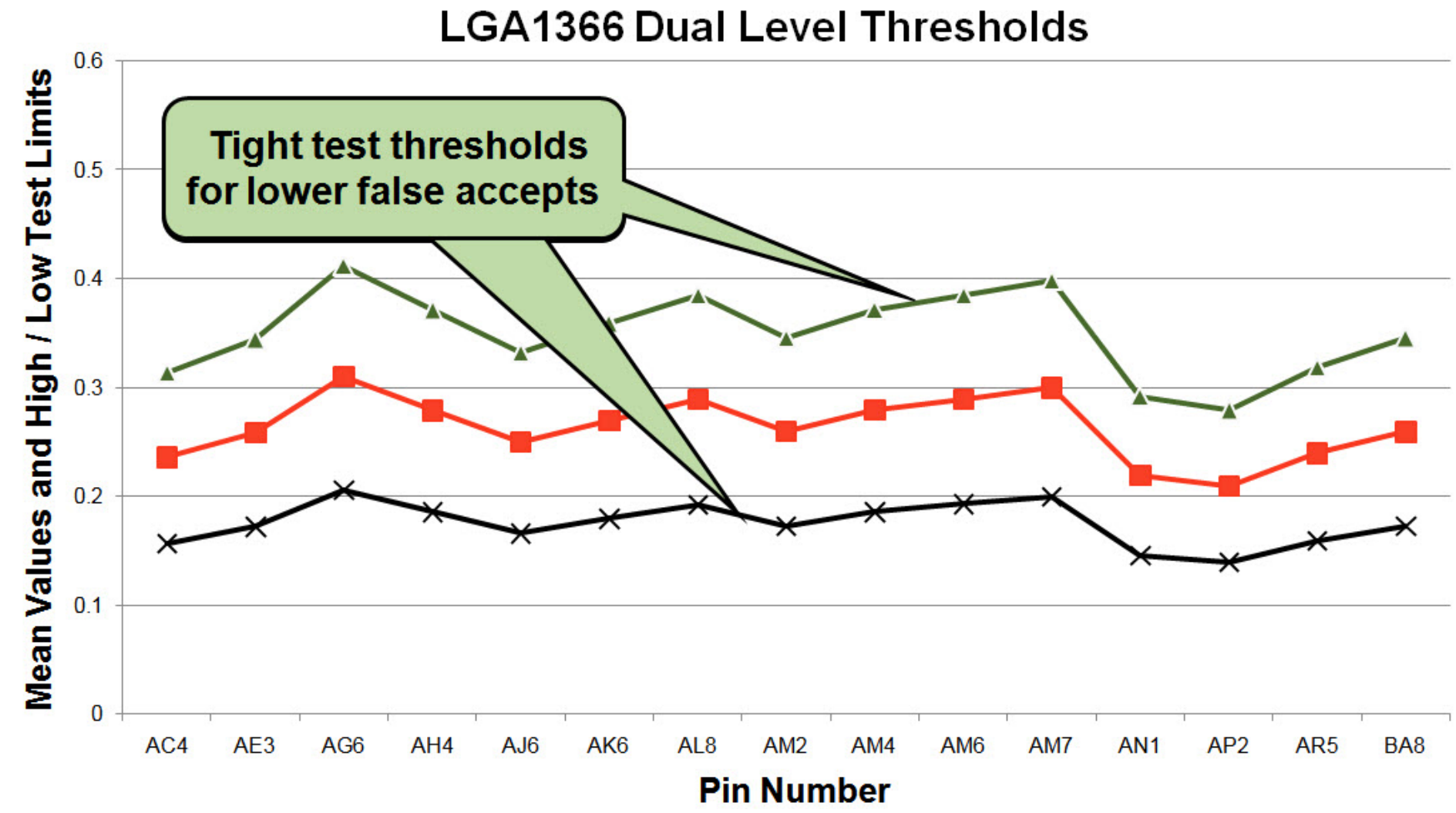



Multiple hanger points for increased mechanical stability

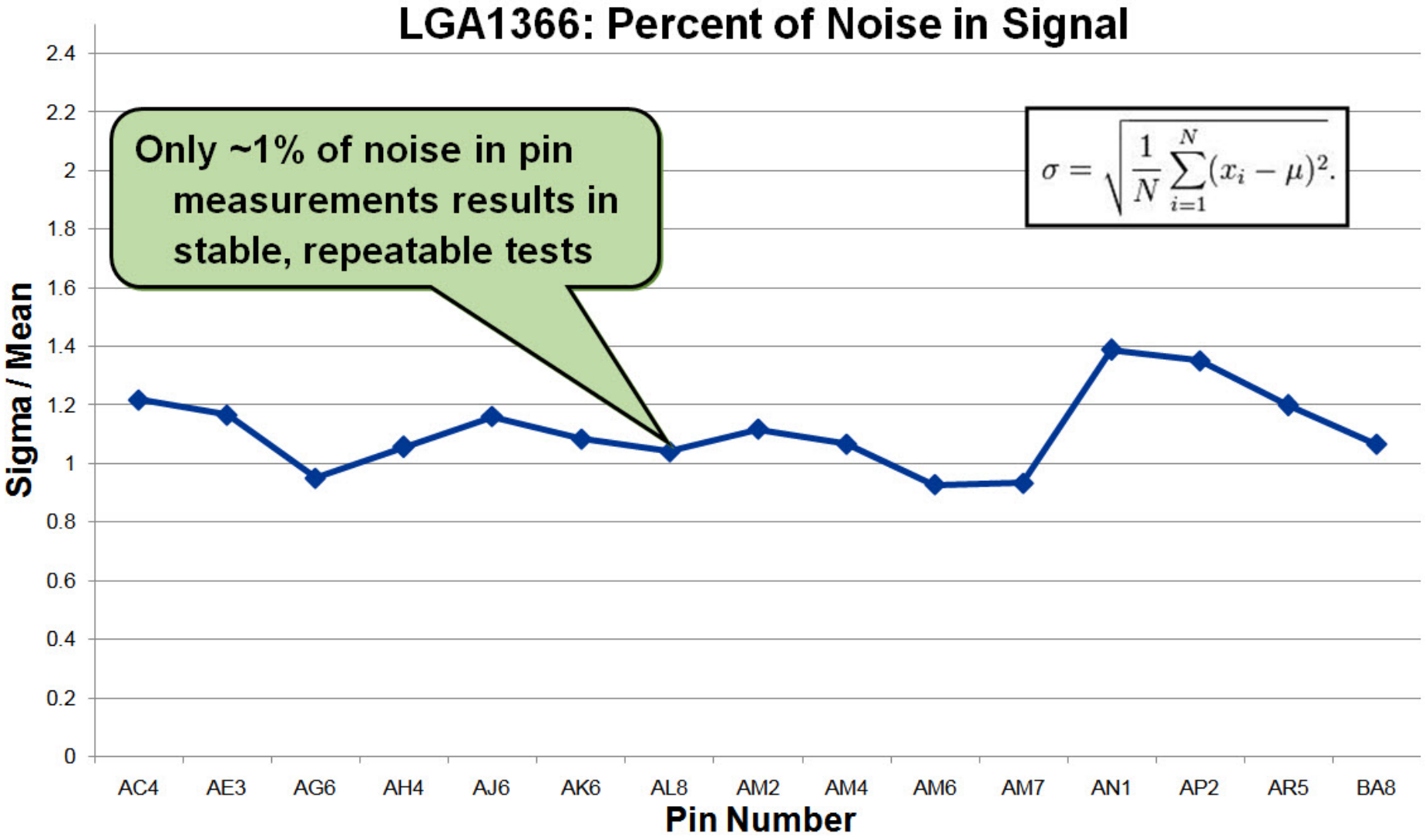
# Connected and Open Pin Values



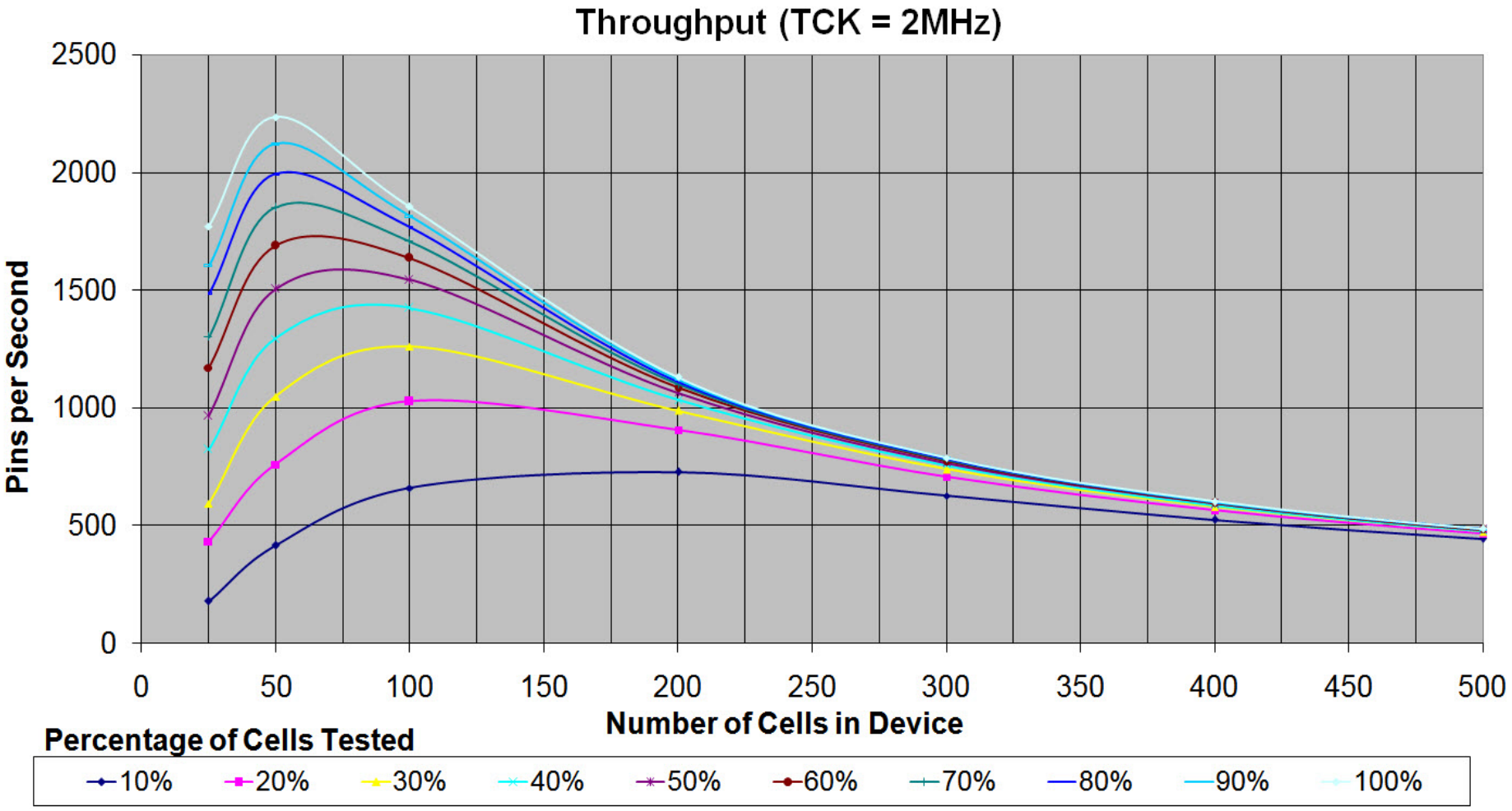
# Mean Values and Threshold Settings



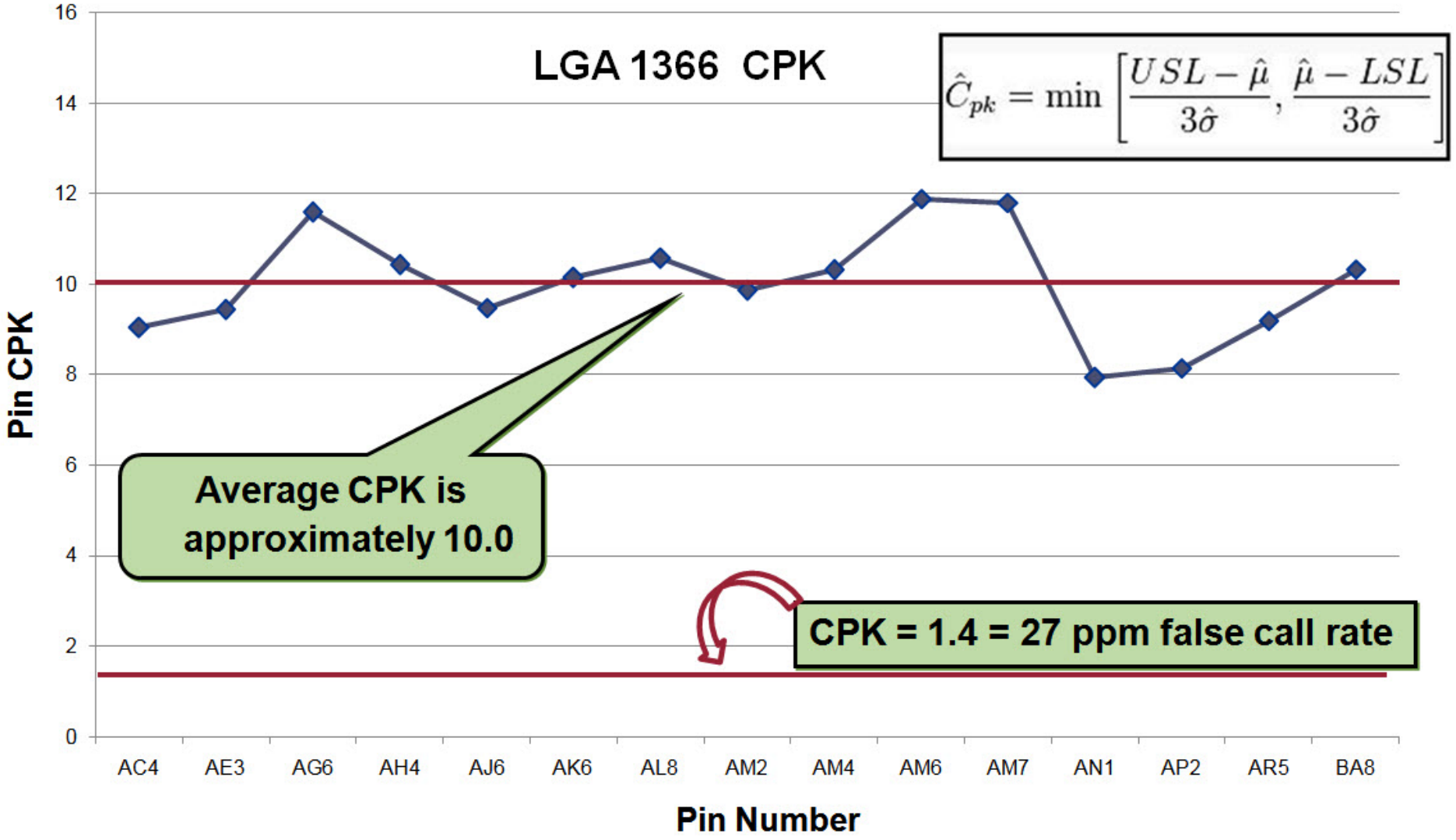
# Pin Standard Deviations / Noise



# Throughput of Pulsed Technique

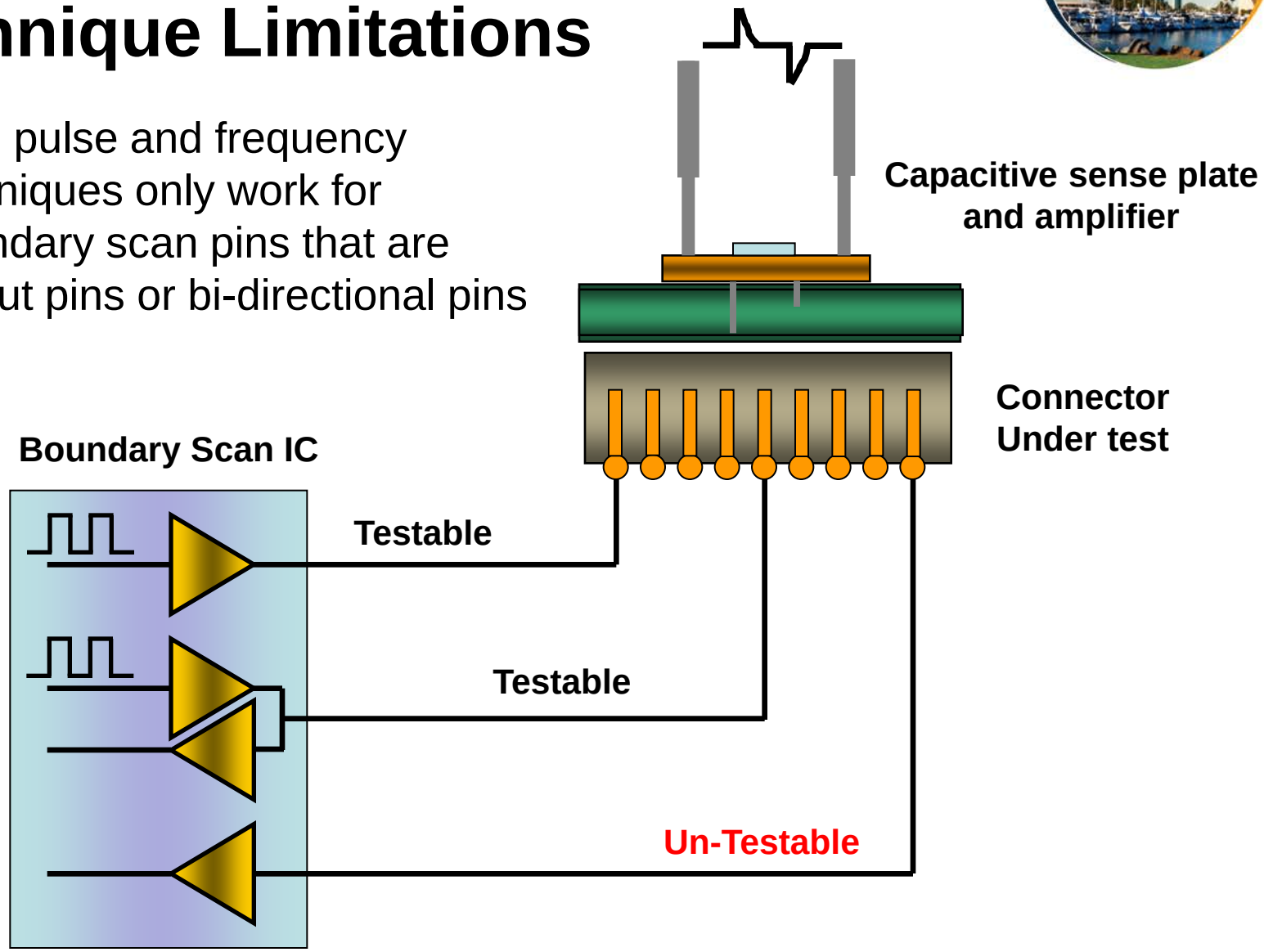


# Excellent Process Capability (CPK)



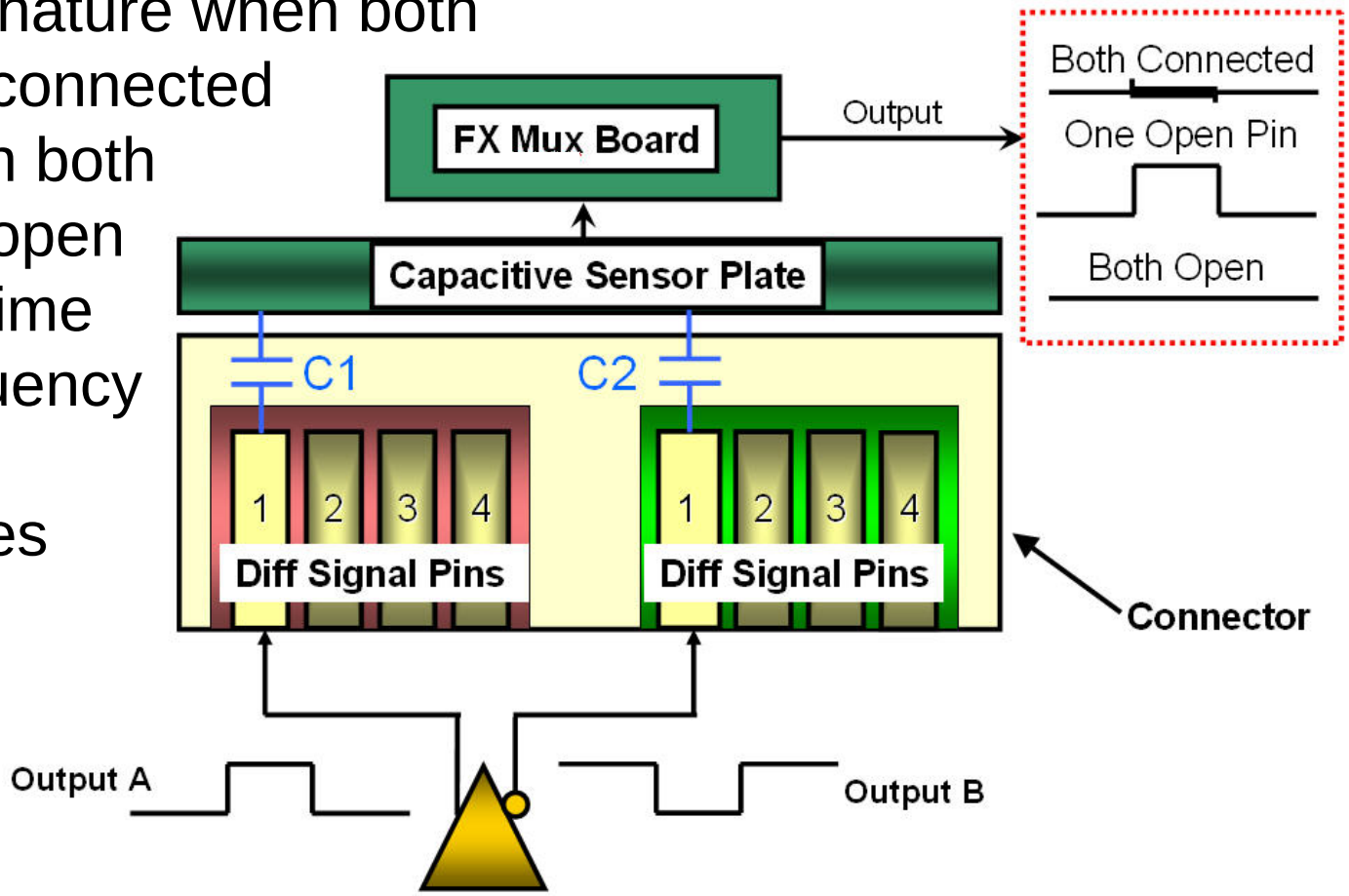
# Technique Limitations

- Both pulse and frequency techniques only work for boundary scan pins that are output pins or bi-directional pins



# Technique Limitations

- Differential signals have the same signature when both pins are connected and when both pins are open for both time and frequency domain techniques



# Solving Technology Limitations

- IEEE P1149.8.1 standard proposes enhancements to the boundary scan standard by adding new capabilities:
- A solution to provide stimulus capabilities to input only pins
- Resolution of diagnostic ambiguity with differential pins
- Providing a method of making a pin toggle frequency independent of the boundary scan chain length for frequency based test methods

**http://grouper.ieee.org/groups/1149/atoggle/**

# Powered Opens Summary

- Virtual access test solution for nets with no test pad access or on dense boards that cannot afford test pad real estate
- Operates with all 1149.1 and 1149.6 compliant boundary scan devices with no cell count restrictions
- Low false call rates from matched filtering and time domain algorithms
- Can save on fixturing costs by removing fixture nails
- Helps solve tester pin-count limitations

# Discussion