

Pushing the barriers of wafer level device integration:

High-speed assembly, the case for MicroTape.

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1. Background

Over the last 10 years, the adoption of wafer-level packaging (WLP) has expanded to a wide range of semiconductor devices applied in a cross-section of industries from Automotive to Mobile Phone, Sensors to Medical Technology.

Of the two basic WLP form factors, bare die, requiring gold wire attachment to integrate chip function into a circuit, has typically been used for low-pin-count (<50 I/O) applications, including analog devices such as power amplifiers, battery management devices, MOSFETs, image sensors and integrated passives.

The second form factor, flip-chip, providing greater performance, has provided expansion into many device types, ranging from sensors, and high-performance logic to a variety of devices found in wireless products.

Today, an increasing number of suppliers of application-specific ICs (ASICs), field-programmable gate arrays (FPGAs), digital signal processors (DSPs), chipsets, graphics, memory and microprocessors are expanding their use of flip-chip packages. Many companies plan to use flip chip for higher-pin-count applications (>100 I/O),

According to Techsearch's Flip Chip and WLP: 2006 Market Update and Technology Developments Report, a compound annual growth rate (CAGR) of more than 24% for WLP's (combined flip-chip and bare die) between 2005 and 2010 is projected.

This represents good news for technology companies involved in specialist wafer fab and device manufacturing, however WLP applications to date have been mostly limited to die smaller than 5mm x 5mm. Solder joint fatigue due to stresses generated by the coefficient of thermal expansion mismatch between the die and the printed circuit board (PCB) or substrate has limited adoption of WLP for large dies (Guilian et al, 2007; Patwardhan, et al, 2005).

2. Assembly perspectives

Applications in Electronics have focused upon small WLP devices, typically 0.5 mm to 3mm square. For the contract electronics manufacturing (CEM) and original design manufacturer (ODM) industries the consequences are a corresponding range of handling problems associated with small silicon devices in PCB, substrate and reflow processes. This has served to restrict the use of WLP devices.

Traditional solutions to these problems are orientated towards semiconductor manufacturing techniques rather than PCB assembly. 'Die Bonders' evolved from semiconductor back-end plastic packaging technology assembly applications into the PCB industry. These equipments pick devices directly from wafer using foil and film-frame; however, there are a number of downsides to die placement systems of this type. These are:

1. For both CEM and ODM, high-cost (typically \$3-500,000 USD) specialist die bonder platforms are required with operational, training and financial implications.
2. Assembly speeds tend to be slow, 5,000 cph in comparison to 50,000 cph+ available from traditional PCB assembly platforms.
3. Users also need to take account of Quality implications in underpinning Quality Policy. As experienced by at least one major CEM the presence of both good and reject WLP devices from wafer using such platforms can provide catastrophic yield effects as wafers may exhibit only 10% device yield.
4. Where customers do not use many die or flip chips in one production lot, the remaining part wafer is difficult to store and the blue or ultra violet (UV) activated film frame and foil does not respond well to multiple setups where repeated stretching is required every time a device needs to be removed for placement. Invariably wafers are rendered un-usable due to foil tears.

Reject WLP devices can exhibit a range of defects. Generally electrical rejects are apparent to the user as a result of wafer test and electronic mapping. However it is mechanical defects such as device chipping, cracks, absence of bumps on flip chips, contamination and handling issues inflicting post test damage which often go un-noticed using such die bonder equipment .

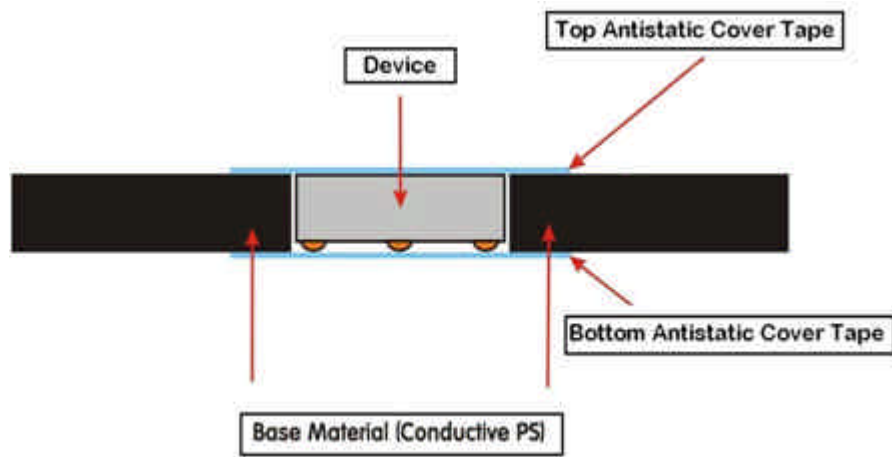
3. Solutions using standard PCB assembly platforms

For ODM and CEM's clear operational, quality and financial advantages are apparent if standard PCB placement platforms are utilized for assembly. Many such modern platforms now provide capability to place 01005 devices and are available with vision to inspect devices of this nature. Bolt on vision enhancements provide WLP capability for bump inspection down to 80 microns diameter and bump pitches sub 100 micron.

However to present WLP devices to feeders requires the use of suitable carrier tapes.

According to Siemens AG, recent testing of Reel Service Ltd.'s MicroTape has provided a conclusive solution to this problem.

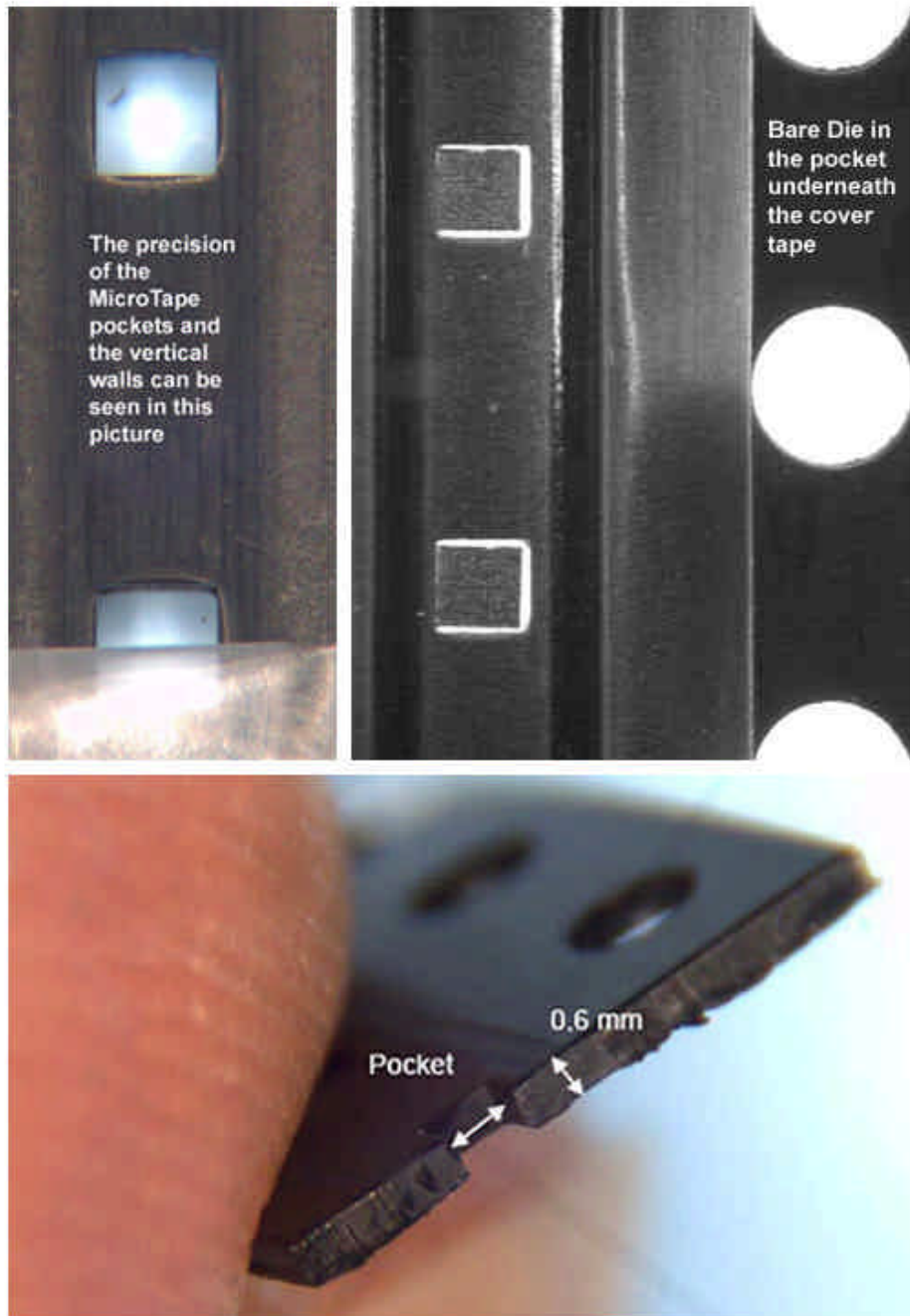
Fig 3.1 'MicroTape' construction



(source: Reel Service Ltd.)

MicroTape is an engineered carrier tape for WLP devices either in bare die or Flip Chip form factor. It exhibits high precision pockets with vertical walls not achievable using standard tape manufacturing processes, to provide absolute location for WLP devices. Base material thickness is selected to suit device thickness thus providing complete protection. Devices are located into the MicroTape pockets and retained using top and bottom cover tapes. Inspection of the device is possible as is the option to invert the device during the assembly process through the removal of either of the two cover tapes.

Fig 3.2 WLP in pocket



(source: Siemens AG.)

4. Evaluation

Siemens AG conducted MicroTape pick up and placement evaluation tests for small WLP devices.

To evaluate the MicroTape solution a device measuring 0.7mm x 0.7mm x 0.4mm thick was placed into MicroTape with a pocket size 0.8mm x 0.8mm x 0.6mm thick.

The taping & reeling process was achieved with the use of Reel Service Ltd's high performance ISORT wafer to tape & reel systems. The ISORT automated equipment provides electronic wafer map interpretation to preclude electrically failed devices from the taping & reeling process. Advanced vision capability provides for post test screening of any mechanical defects to 12 microns resolution including chipping, dicing issues, scratches, bump presence and contamination on both top side and bottom side of the WLP device. The result - only "known good die" in the MicroTape.

A quantity of 3200 bare die devices were placed from one 7" reel using a SIPLACE X2 placement platform , equipped with a 20 nozzle C&P head and standard 8mm X type feeder.

5. Results

During evaluation testing the 3200 bare die components were picked from the MicroTape and placed upon a test board with 400 placement locations. A pick rate of 99.90% was achieved at a placement rate of 21,000 cph.

6. Conclusion

Siemens AG concluded that MicroTape is well designed for high-speed-placement of components which need to be supplied within an accurate media and precise orientation. The use of standard feeders which usually already exist at the PCB assembly contractor makes for a solution which is both easy to use and straightforward for engineers to implement. A great improvement over alternative tape based solutions which require the procurement of prohibitively high-cost, long lead-time 'special' feeders.

High-speed-placement using standard PCB placement platforms provides clear advantages for both ODM's and CEM's in reducing both assembly costs and capital equipment needs.

Taped components provide for only 'known good die' and flip chips on assembly lines, negating the need to adjust Quality systems to accommodate both good and reject devices.

MicroTape, taped & reeled components are easier to handle than wafers or other adhesive based tape systems providing for less component attrition due to handling problems. Where an assembly requires only a partial quantity of devices from a wafer, MicroTape provides a guaranteed method of future placement for remaining devices ensuring that they may be used without the possibility of blue or UV film frame foil tearing rendering them useless.

For those users of multiple dies or flip chips on a single PCB or substrate assembly, standard placement machine feeder locations used with MicroTape enable multiple WLP device placement, another advantage over die bonder foil based solutions where only one wafer may be accommodated and picked from at any one time.

7. More Information

a) For more information on Reel Service Ltd. and MicroTape or sub-contract WLP taping & reeling please contact

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Bibliography and References

1. Anon (2006), *Flip Chip and Wafer Level Packaging, Trends and market Forecasts*, Techsearch International, Austin Tx.
2. Anon (2006), Study Shows Flip-Chip and Wafer-Level Package Use Expanding, *Semiconductor International*, 10/16/2006.
3. Guilian G., Haba, B., Oganessian, V., Honer, K., Ovrutsky, D., Rosenstein, C., Axelrod, E., Hazanovich, F. and Aksenton, Y. (2007), Compliant Wafer Level Package for Enhanced Reliability, Tessera Inc., San Jose; in *International Symposium on High Density packaging and Microsystem Integration, 2007*. HDP '07.
4. Heilmann, N (2008), *Testing of pickup-rate and placement rate for bare die packaged in MicroTape*, Siemens AG, Munich 01/02/08
5. Patwardhan, V.; Chin, D.; Wong, S.; Rey, E.; Kelkar, N.; Nguyen, L. (2005), Flexural testing of board mounted wafer level packages for handheld devices, *Electronic Components and Technology Conference, 2005*. Proceedings. 55th Volume , Issue , 31 May-3 June 2005 Pp. 557 - 561 Vol. 1