# ADVANCED ORGANIC SUBSTRATE TECHNOLOGIES TO ENABLE EXTREME ELECTRONICS MINIATURIZATION

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**ABSTRACT**
High reliability applications for high performance computing, military, medical and industrial applications are driving electronics packaging advancements toward increased functionality with decreasing degrees of size, weight and power (SWaP) The substrate technology selected for the electronics package is a key enabling technology towards achieving SWaP. Standard printed circuit boards (PWBs) utilize dielectric materials containing glass cloth, which can limit circuit density and performance, as well as inhibit the ability to achieve reliable assemblies with bare semiconductor die components. Ceramic substrates often used in lieu of PWBs for chip packaging have disadvantages of weight, marginal electrical performance and reliability as compared to organic technologies. Alternative materials including thin, particle-containing organic substrates, liquid crystal polymer (LCP) and microflex enable SWaP, while overcoming the limitations of PWBs and ceramic.

This paper will discuss the use of these alternative organic substrate materials to achieve extreme electronics miniaturization with outstanding electrical performance and high reliability. The effect of substrate type on chip-package interaction and resulting reliability will be discussed. Microflex assemblies to achieve extreme miniaturization and atypical form factors driven by implantable and in vivo medical applications are also shown.

Key words: organic substrates, mechanics of materials, chip-package interaction, flip chip, low loss.

**INTRODUCTION**
A wide range of applications are enabled by extreme electronics miniaturization. On the macro level, large scale systems, such as high performance computing servers, medical diagnostic tools as well as aircraft or other military systems, greatly benefit from reduced size electronic assemblies through increased functionality, performance and integration with reduced footprint and/or payload. On the micro level, small scale systems, such as portable, handheld and implantable, are produced, and may not otherwise be possible if not for electronics miniaturization. Size, weight and power (SWaP) reduction is key to meeting the wide range of requirements to support these applications.

Electronics miniaturization drives the use of increasingly smaller, higher density components, including fine pitch BGAs, CSPs, tiny SMT passives as well as bare die and stacked die. These types of components complicate the assemblies as compared to traditional PWBAs due to a number of factors including reduced ball/pad/bump size, reduced pitch, low or ultra low k (ULK) die and stacked die. In the case of advanced semiconductor die, shrinking the size of the flip chip I/O connections, along with the brittle nature of ULK materials drive a considerably more complex mechanics of materials scenario with chip-package interactions greatly impacting assembly producibility and ultimate reliability.[1,2] The mechanical properties of the substrate now become *significantly* more critical. The substrate is the foundation on which the electronics assembly is produced: the substrate material set and construction drive producibility, reliability, form factor compliance and electrical performance. Substrate attributes having significant impact on the ability to reliably assemble these very fine pitch components and bare die include:

- Dielectric Material & Filler: glass cloth vs. particle
- Dielectric Thickness
- CTE & Modulus
- Blind & Buried Vias
- Line Width & Space Capability

**PWBs FOR SEMICONDUTOR PACKAGING**
The electronics industry has a history of driving existing technologies to the limit of their capabilities before moving on to newer technologies and alternative approaches. This has been the case with printed wiring board (PWB) capability. Used extensively since the mid-twentieth century, PWB technology has progressed, but still typically incorporates some long-standing attributes such as glass cloth filler and mechanically drilled core vias. Perhaps the most notable shift occurred with the implementation of build-up technology which utilizes laser drilling for the outer wiring layers of the boards. In contrast, the semiconductor industry initially grew based on the use of rigid ceramic substrates for packaging of bare die.

As certain limitations with ceramic materials were reached, this industry sought out organic materials for improvements in electrical performance, dimensional control and reduced weight. The initial obvious organic format of choice was the PWB, as the manufacturing infrastructure was already in-place. PWBs have been implemented quite successfully as an alternative substrate to assemble bare die on to, especially in the case of wirebond configured die. But as the semiconductors advance, smaller package form factors along with high speed performance requirements demanding shorter connection paths are resulting in more die being fabricated in flip chip format. This format, coupled with new semiconductor materials used at and below the 90 nm node, poses a challenge for direct assembly onto the higher CTE rigid PWBs. The adoption of Pb-free solders only exasperates the producibility issue further, by both driving up the required reflow temperature as well as the more brittle nature of the common SAC alloys.

One of the methods being employed to alleviate these issues is to place a silicon interposer between the die and the PWB, thus evolving into what is known as 2.5D Integration.[1,2] This method has been successfully implemented particularly in the packaging of advanced field programmable gate arrays (FPGAs)[3], but face a number of hurdles toward widespread implementation, ultimately related to complexity and cost.[4] Another approach being taken is to develop organic materials with a much lower CTE, as well as extreme via aspect ratios and very fine line width and space capabilities.[5] In both of these approaches, however, the organic substrate is still based on a thick core configuration.

## THIN VS. THICK CORE

High density substrates fabricated from thin particle containing organic laminates are a good alternative to standard glass cloth containing PWB dielectrics. Figure 1 shows a cross-section comparison of the silica particle filled epoxy-based CoreEZ® thin laminate vs. a standard buildup PWB. The absence of glass cloth in the dielectric provides several distinct key advantages including reduction to thickness, core via pitch and surface topography, along with improvements to assembly yields and reliability.

**Substrate Thickness:** The particle filled dielectric layer thicknesses are substantially less than glass cloth counterparts, therefore, the overall laminate stack-up is much thinner.

**Core Via Pitch (CVP):** Formation of vias in the particle containing dielectric materials are readily accomplished with UV lasers, as opposed to mechanical drilling for PWB core vias and $CO_2$ lasers for blind and buried via formation in PWB buildup layers. The smaller via size subsequently reduces capture pad area requirement and enables a much tighter core via pitch (CVP), on the order of 9X, as shown in Figure 2. When CVP is nearly equivalent to die bump pitch, it enables Z-escape routing to all wiring planes which can eliminate the need for additional buildup layers. This can also relax the line width and space requirements for signal routing as all of the wiring planes are accessible, thereby improving manufacturing yield.

**Surface Topography**: The absence of the glass cloth also results in a smoother surface finish on the particle filled dielectric, enabling higher resolution photolithography for finer line widths and spaces, which results in improved electrical performance.

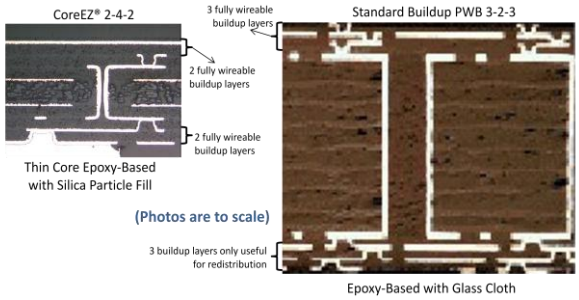



**Figure 1. Comparison of Standard Buildup PWB to Thin Core Particle Filled Substrate.**

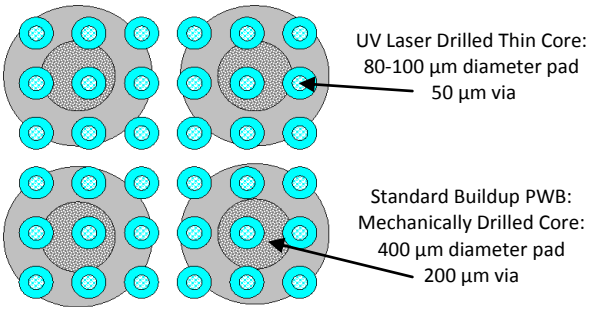



**Figure 2. Core Via Pitch (CVP) Comparison between UV Laser Drilled Particle Containing Laminates vs. Mechanically Drilled Standard Buildup PWBs.**

**Assembly Yields:**

The greatest temperature cycle gradient an electronics module experiences is during solder reflow assembly operations. It is under those conditions that CTE mismatches and design imbalances can manifest into defects and low assembly yields. Figure 3 is a qualitative depiction of the core via Z-axis displacement over a temperature cycle from cold to reflow. The substrate expansion at higher temperatures combined with the effect of the PTH restraint creates a Z-axis expansion stress on buildup layers and soldermask, resulting in potential halo delamination. The finer core via size and pitch, and thinner core substrate, will have correspondingly less surface Z-deformation when subjected to temperature excursions. The difference in Z-expansion between a relatively stiff copper via, and surrounding dielectric, can be substantial. By reducing the size and corresponding stiffness of a via, the resulting surface deformations are reduced. As illustrated in Figure 3, this reduction of deformation can significantly reduce the tendency for via stress-related

underfill delamination, which is often observed in a halo-mode related to under-die core vias.

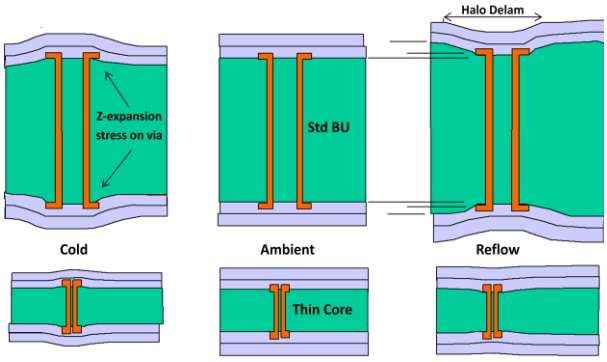



**Figure 3. Illustration of Core Via Z-Axis Displacement over Temperature Cycle.**

**Reliability:** A detailed discussion of package reliability is given later in this paper. Of additional note to that discussion is that the risk of CAF (conductive anodic filament defects) is eliminated entirely with the omission of glass cloth.

## EMBEDDED PASSIVE AND ACTIVE DEVICES

Passive components can comprise a significant portion of today's electronic assemblies. An effective strategy to reduce the surface area consumed by discrete passive components is to embed them into the substrate. Current interconnect technology to accommodate surface mounted passives impose certain limits on board design, which limit the overall circuit speed. Embedding passives reduce parasitic effects and improve performance in addition to saving substrate real estate and conversion cost.[6]

Processes for embedding thin film resistors into organic substrates have become fairly routine, substantially minimizing the discrete resistor count. The shape of the embedded resistor design can be optimized to allow for the placement of vias as shown by the serpentine structures in Figure 4. Laser trim aids in meeting design requirements for tight resistor tolerances.

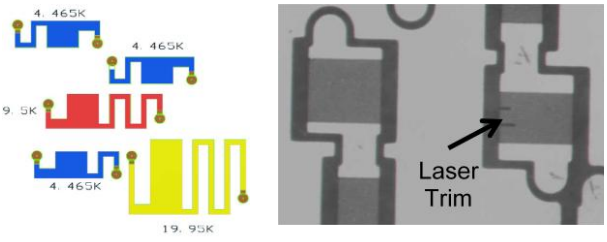



**Figure 4. Embedded Thin Film Resistors.**

Among the various passives, embedded capacitors deserve special attention as they provide the greatest potential benefit for high density, high speed and low voltage IC packaging. Capacitors can be embedded into the interconnect substrates (printed wiring board, flex, MCM-L, interposer) to provide decoupling, bypass, termination, and frequency determining functions [7,8]. In order for embedded capacitors to be useful, the capacitive densities must be high enough to make layout areas reasonable. Available commercial polymer composite technology is not adequate for high capacitance density thin film embedded passives. Several polymer nanocomposite studies so far have been focused on processing of high capacitance density thin films within small substrates/wafers [9-12]. One of the important processing issues in thin film polymer nanocomposite based capacitors is to achieve high capacitance density on large coatings. The miniaturization and embedding of components that SiP provides will greatly reduce the size, weight and power (SWaP) of the application.

New technologies for embedding active die are being developed and implemented into the manufacturing environment. A variety of active silicon die with metal pads, have been embedded and electrically connected to develop highly integrated packages.

## SYSTEM-IN-PACKAGE (SiP)

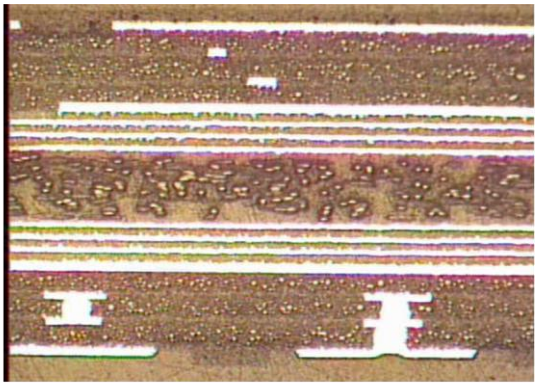
System-in-Package (SiP) designs that implement embedded passive and active components further enable SWaP reductions. Thinner, high-density substrate technologies lower inductance, driving down the need for decoupling capacitors in the design. For example, high density interconnect technology combined with embedded passives and small die and component body sizes have been shown to achieve as much as 27 times reduction in physical size for existing printed wiring board assemblies, with significant reductions in weight and power consumption. Primary reductions in power are due to reduced interconnect lengths and corresponding load. Shorter interconnects can also reduce or eliminate the need for termination resistors for some net topologies.

## MATERIAL OPTIONS

Several different materials sets have been developed and successfully implemented for fully qualified production processes compliant with industrial and military standards and compatible with Pb-free assembly where required. The selection of the material set is driven by a number of factors including the electrical performance requirements, thermal, mechanical, reliability, form factor and system integration. Specific material sets discussed here include the epoxy-based CoreEZ®, PTFE-based HyperBGA® and liquid crystal polymer (LCP).

The particle filled, epoxy-based CoreEZ® shown in Figure 1 can be fabricated with up to 4 buildup layers, with a total cross-sectional thickness range of approximately 0.5 – 0.7 mm. This highly versatile material set can be configured to support diverse design requirements. Thin film resistors and embedded capacitance layers can be incorporated into the cross-section (Figure 4). Original implementation was based on a p-aramid fiber core, but more recently, a thin, 25 µm LCP layer can be used in lieu of the p-aramid to

result in a basically coreless structure (Figure 5) with improved electrical performance and a thinner cross-section. The process fabrication flow for producing the CoreEZ® laminate is also compatible with embedding discrete components including bare die and even batteries. This technology has been successfully implemented for a wide range of applications including military and Pb-free assembly, and it is also rad hard compatible.



CoreEZ® 3-8-3 with Embedded R&C

**Figure 4. CoreEZ Substrate with Embedded Resistors and Capacitance Layers.**

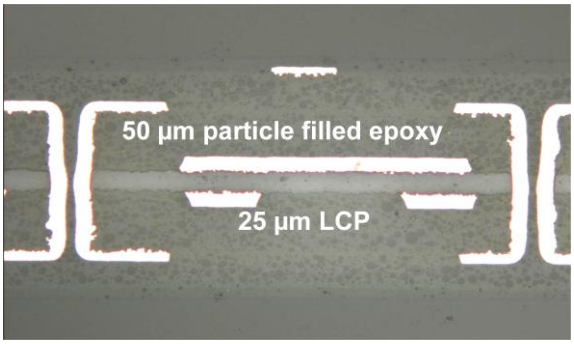



**Figure 5. CoreEZ® Substrate with 25 µm LCP Core.**

A particle based PTFE substrate technology, HyperBGA®, has been in production since 1992. This material set combination was specifically engineered to provide a compliant laminate for reliable assembly of very large, high I/O ASIC die for high performance computing. Since then, however, it has been implemented for a number of other applications, both mil-spec and industrial grade. The low loss PTFE/KPPE material set is particularly well-suited to support both very high speed digital as well as RF applications beyond 20 GHz. Figure 6 shows a cross-section of a typical 9-layer HyperBGA®. This material set, however, has been produced up to 13 layers, and can be configured in a number of different ways including 3-7 layer cores, up to 3 buildup layers, soldermask and embedded thin film resistors. The HyperBGA material set combination of the low CTE Cu-Inva-Cu core coupled with the low modulus particle-filled PTFE provides a compliant laminate for very high reliability, low stress assembly of challenging die materials including ultra low K (ULK) advanced semiconductors, GaAs, SiGe as well as very brittle CZT crystals. Figure 7 shows a cross-section of a 65 nm FPGA flip chip assembly onto a 9-layer HyperBGA® substrate. The FPGA has greater than 5300 I/O and is approximately 19 x 20 mm in size. This is a direct flip chip assembly accomplished *without* the use of a silicon interposer. This package is in production, and tested for full industrial grade compliance. Similar system-in-packages have also been produced and are fully compliant with a range of mil-spec standards.

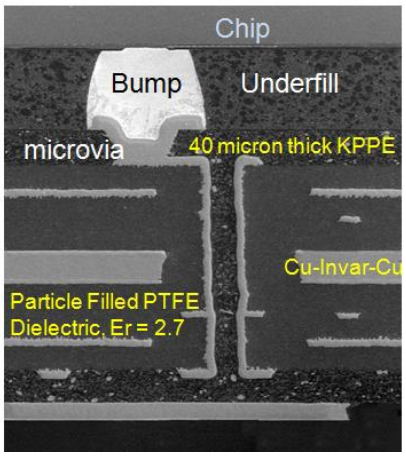



**Figure 6. 9-Layer HyperBGA Cross-Section.**

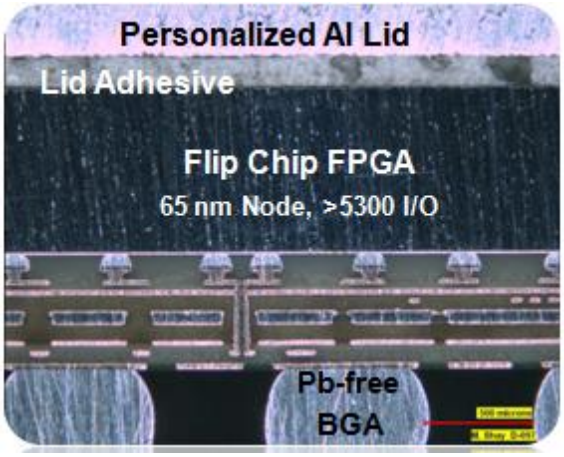



**Figure 7. Cross-Section of Direct Flip Chip FPGA Attach onto HyperBGA Assembly.**

Liquid crystal polymer (LCP) is a newer material to be implemented for advanced packaging applications, driven by performance requirements not met by the alternatives. LCP has several key attributes, including low loss, inherently near-hermetic, light weight, radiation hard, moldability and biocompatibility. It is, however, a challenge to process into multilayer structures due to its thermoplastic nature and high Z-axis CTE. This material set has been qualified for production up to 6-layer cross-sections, and prototypes demonstrated up to 12 layers. (See Figures 8 and 9) This technology continues to evolve as demand grows, and efforts to develop embedded resistor technology along with alternative hybrid material combinations are in-work.

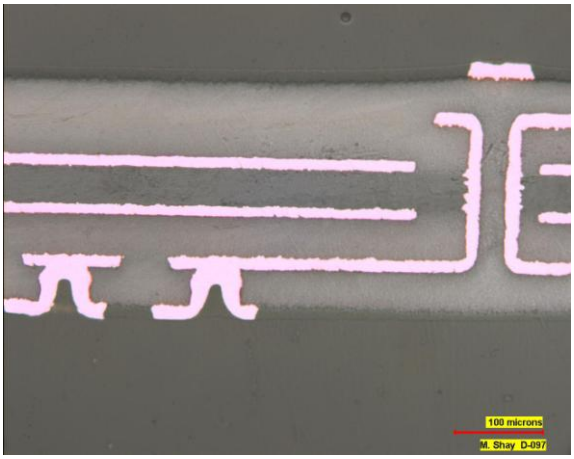



**Figure 8. 6-Layer LCP Cross-Section with Microvias.**

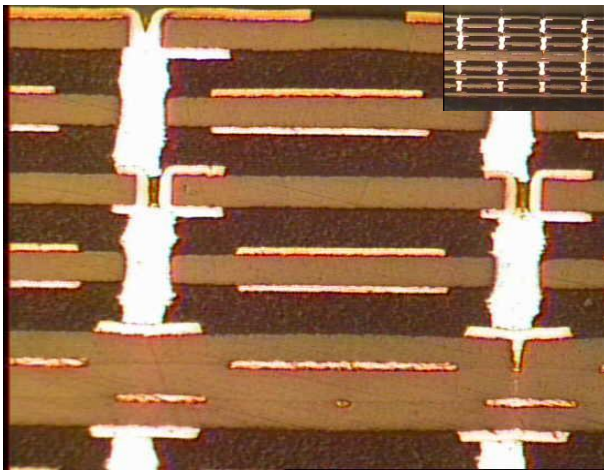


**Figure 9. 12-Layer LCP Z-Interconnect Substrate.**

## ELECTRICAL PERFORMANCE

Thin particle filled laminate CoreEZ® and HyperBGA® substrate technologies are engineered for superior electrical, thermal and reliability performance. Both technologies are fabricated with high density interconnect (HDI) groundrules, including 2 mil (50 µm) laser drilled vias and 1 mil (25 µm) line and space circuitization, with via-in-pad technology. Both technologies are fundamentally "core plus build-up" construction, but the core thickness is so small and core via density is so fine that the substrates behave as coreless. The electrical advantages of this "coreless" behavior include extremely small substrate thickness and capability for increased via densities, resulting in a direct reduction in power distribution path lengths and effective impedances. Optional embedded capacitance layers are available to reduce surface component quantities and extend supply bypass / decoupling solutions beyond the 1 GHz range. Noise due to simultaneous switching I/O is reduced as well with features such as thin dielectrics, short, high density via arrays, and low impedance paths to the power supply and decoupling capacitor. Via-in-pad capability not only results in a more compact component placement, but also can minimize the electrical parasitics and discontinuities associated with component mounting.

Substrate technologies offering medium loss (silica particle-filled high temp FR-4 with Df = 0.013) and low loss (silica particle-filled PTFE with Df = 0.003) dielectrics, combined with HDI process capability, provide an exceptional environment for signal and power distribution, even in a radically miniaturized application. Controlled impedance stripline transmission line structures with thin dielectrics result in low crosstalk and low impedance discontinuities. Extreme miniaturization accomplished with these substrate technologies can enhance loss characteristics in on-substrate high speed serial channels. Miniaturization allows for small spacing between TX and RX components which significantly reduces signal length. Low loss dielectric material and copper conductors provide low signal attenuation for that shortened signal path, compounding the loss reduction. Further reductions in loss are possible with the ability to avoid via stubs in optional stackup constructions. Substrate technologies have been demonstrated to easily support 12.5 Gbps in channels without active compensation or equalization, and early studies indicate support for 28 to 40 Gbps in actively enhanced SERDES channels. HyperBGA® has been demonstrated to support 35 - 40 GHz RF signals as well. Hybrid stackups are also available for high bandwidth analog and RF signal performance, providing opportunity for thicker effective dielectrics and larger signal cross-sectional area.

## MICROFLEX & ULTRA FINE PITCH FLIP CHIP ASSEMBLY

In instances where extreme electronics miniaturization is required, such as in the case of implantable or in vivo medical devices, the rigid substrate technologies discussed in this paper are not often suitable to achieve size and atypical form factor requirements. Advanced microflex coupled with ultra fine flip chip assembly meets the challenge of extreme miniaturization and unique form factors requirements. Microflex – very thin flex based on 12.5 µm polyimide or other very thin polymer films such as LCP – can be fabricated for assemblies that can be rolled or folded into very small form factors. Figures 10 and 11 illustrate highly miniaturized assemblies on microflex for use in in-vivo diagnostic and intravascular ultrasound catheter applications. These devices utilize double-sided and single-sided microflex substrates, respectively.

The use of semi-additive circuitization facilitates manufacture of fine-line circuit features on the flex. A smooth copper-polymer interface is ideal for this fine line circuitization, and selection of appropriate material surface preparation and metal deposition processing provides good metal adhesion to the base polyimide film. Ultra fine flip chip assembly with bump pitch on the order of 70 µm is used to produce this microflex assembly in high production volumes.

The design of microflex assemblies require significantly different criteria compared to rigid SiP. Microflex SiPs are typically based on ASIC die, to absolutely minimize the semiconductor volume requirement for the assembly. Since the microflex assemblies are often rolled or folded to achieve the final form factor, a thorough understanding of achievable bend radius based on flex and metallization thickness, along with bond ply if used or soldermask needs to be made. The end use conditions of the flex need to be well-understood: is it a one-time bend at final packaging or will the the microflex assembly be subjected to repeated flexure? All of these considerations need to be made in laying out the microflex design, component placement and selecting underfill or encapsulation. Modeling of the structure is very critical to producing a design that is both robust and reliable.

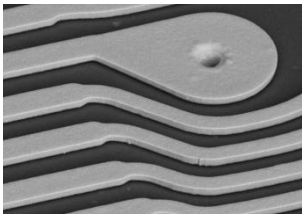


**Figure 10. SEM micrographs showing (Left) fine line circuit traces (11 µm) on thin double-sided flexible substrate (25 µm. Via diameter in the micrograph on the left is 25 µm.**

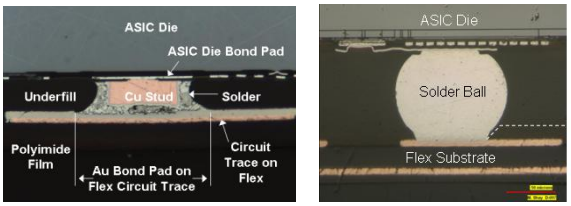



**Figure 11. Optical photograph of cross section showing (Left) micro pillar-bumped ASIC die with eutectic solder on single-sided flex substrate, and (Right) solder-bumped (SAC) ASIC die on double sided flex substrate.**

## RELIABILITY

Obtaining high reliability in extreme applications, as measured and proven by stress testing, has numerous facets that extend beyond the scope of this paper. However, understanding the impact of fundamental design attributes, especially as related to critical properties of substrates and devices, can be very instructive to reach this goal. One of the ubiquitous problems facing flip-chip assembly onto substrates is due to the interaction between the silicon chip and the substrate; the silicon has a low linearized coefficient of thermal expansion (CTE, taken as 3.0 ppm/C) that typically differs from that of the substrate. When a flip-chip die is joined to a substrate using traditional solder reflow and underfill dispense/cure, just subsequent cooling back to room temperature engenders a stress response that usually results in die warpage, stress to the die owing to this warpage, and interaction stress between the die and substrate. Using well known linear elastic composite analysis techniques, it is possible to numerically compare the effects of substrate design to evaluate specific cases of interest. What is less known are the beautiful complex response functions related to simple design parameters, such as substrate thickness, stiffness, and composite CTE.

It is understood that while a substrate has numerous discrete layers and circuitry features (which require detailed analysis for their effects), one can approximate certain substrate features into an effective composite model. It is not generally possible to accurately simulate an anisotropic layered composite with a single isotropic layer, however, for the instructive purpose of this paper, the complexity of a multilayered substrate has been modeled as an isotropic substrate with just three parameters: thickness, elastic modulus, and CTE. By way of experience, a range of effective typical parameters for various electronic substrates was selected for these comparisons. A nominal substrate modulus of 3Mpsi was selected. Similarly, properties of a typical high-reliability flip-chip underfill with glass-transition temperature (Tg) approximately 135C and cure temperature of 150C was chosen; underfill thickness was maintained at 100 microns.

Of course, the preceeding discussion has assumed that die reflow joining has taken place without issues; substrate self-warpage, bump size variation, and other sources of nonplanarity of the bump array can affect the flip chip joining process outcome. For the results shown in this work, perfectly balanced substrate designs and silicon devices were utilized, meaning no additional tendancy for warpage of a free individual substrate or individual die was included. It is noted, however, that including that effect, if any, in an actual design is vital to successful assembly, especially for thinner substrates and components. During reflow, upon contact of a bump to a substrate feature, a bump will collapse as wetting creates a new ‘joint’ geometry, thus forming a interconnected joint upon cooling and solder freeze. Bump collapse distance is a key factor to absorb nonplanarity and still form a reliable joint. Flip chip bumps, and especially copper column bumps, can have very limited ability to collapse upon reflow; bump pitch generally dictates solder volume of the bump which can be available for joining. Substrate planarity during the reflow process is critical to success of joining, and thus substrates must be correctly designed. In other words, multilayer composite models, to account for circuitry feature included on each substrate layer, are critical to success, just as it is required to accurately model an anisotropic substrate. And, in many cases, the component warpage must also be analyzed and accounted for; this is especially true with thinner components. Indeed, while the usual design goal is planarity, it is also possible and sometimes necessary to ‘match’ the substrate and device curvatures, to allow for correct bump joining, in special cases dictated by very

thin silicon or stacked silicon devices. However, for this work, we neutralize self-warp of components, and simply show the effects of the remaining idealized substrate and die parameters. The nominal die size was taken as 18x18x0.750mm, with elastic modulus 21.8 Mpsi.

In Figure 12, warpage of a typical silicon die after assembly to substrates of various thicknesses is parametrically represented. Results for substrate thickness ranging from 10 to 10000 microns are shown, for selected CTE values ranging from 5 to 30 ppm/C. It is evident that as the difference of CTE of the substrate from that of silicon grows, the warpage response correspondingly grows. At the extremes of substrate thickness, both thin and thick, warpage is reduced. Very thin substrates lack the stiffness to overcome the die stiffness, and very thick substrates cannot be flexed by the die; between these two extremes, there is a substrate thickness corresponding to a maximal warpage response. It is noted that the small nonzero warpage associated with very thin substrates is primarily associated with the 100 micron thick layer of underfill between the die and substrate.

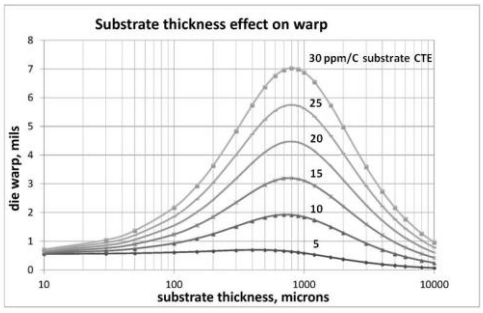



**Figure 12. Warpage of an 18x18x0.75mm flip-chip die after typical assembly, shown as a function of substrate thickness, for a range of substrate CTE.**

In Figure 13, the die stress associated with the same situations as Figure 3 is depicted. The die stress is the maximum principal stress located on the upper surface (away from the substrate); this metric is typically associated with die fracture.

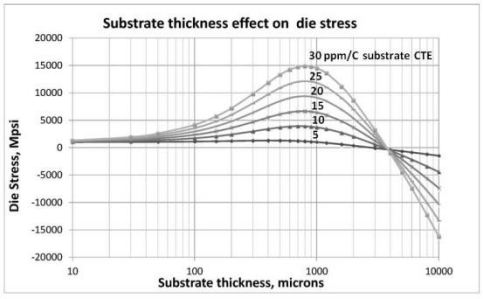



**Figure 13. Stress on the upper die surface after typical assembly, corresponding to conditions as depicted in Figure 3.**

It is interesting to see that as very thick substrates are utilized, the die is actually forced into compression (negative stress region). Not surprisingly, the die stress maximum response follows the warpage response maximum. In Figure 14, the corresponding relative shear loading between the lower surface of the die and the underfill layer is shown. This is a key metric of the die to substrate interaction stress, and is a large part of the overall stress that an underfill must resist in order to protect the die to substrate electrical interconnects. A sharp increase in this critical die to substrate interaction loading exists for very thick substrates, which points to a need for careful attention to reliability aspects for designs in that region. The interaction stress becomes very small for thin substrates, essentially being that due to the underfill which resides on the lower surface of the die. This also has implications for reliability, in that very stress-sensitive devices would be expected to perform well in this region. It is interesting to note that in the region of substrate thickness corresponding to maximal die warpage, shear loading change with respect to substrate thickness becomes invariant.

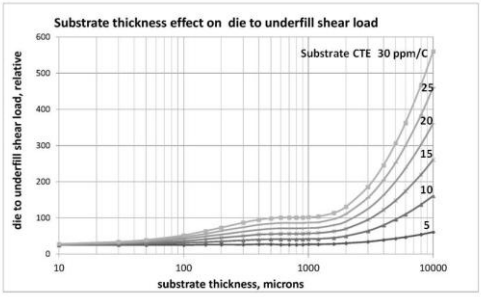



**Figure 14. Shear loading between the lower die surface and underfill after typical assembly, corresponding to conditions as depicted in Figure 3.**

Scanning the results in Figures 12-14, it is apparent that given a 'normal' die thickness, very thin substrates tend to have less warp and stress; reducing the CTE also helps. This of course points to the value of a silicon interposer, at least within this scope. However, as thinned silicon devices become more prevalent, this rule of thumb must be understood to be related to a ratio of substrate to die thickness. Further, as stacked and/or highly thinned devices (which themselves become a complex composite that cannot be modeled as monolithic silicon) become prevalent, it is clear that careful attention to analysis is required to understand the effects due to substrate interaction. Towards this end, results are shown in Figure 15 to illustrate the effect of monolithic silicon die thickness on resulting die warpage, for a range of thickness from 1 micron to 10mm. For this set of results, a common substrate

thickness of 1mm was chosen. Again, no effect of self-warp of the silicon device was included for the results of Figure 15.

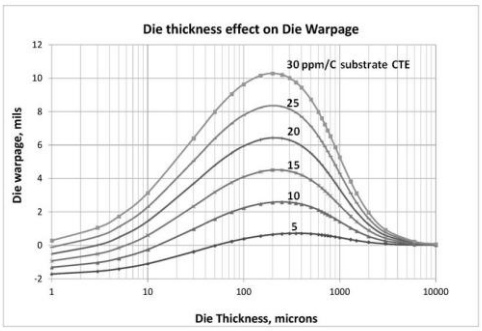



**Figure 15. Warpage of an 18x18mm flip-chip die after typical assembly, shown as a function of die thickness, for a range of substrate CTE.**

It is interesting to see that, for this particular substrate thickness, die must become extremely thin (well below approximately 100 microns) to obtain reduced warpage relative to a standard die thickness of 750 microns; handling wafers of that thickness is difficult and expensive. Silicon interposer thickness is typically in the 200-500 micron range, which engenders a complex and increased warpage response as compared to typical wafer thickness of 750 microns.

In Figure 16, the corresponding die stresses are shown, again being the maximum principal stress on the topside of the die, for a range of selected substrate CTE values. Very low die stress is observed to exist in a region of die thickness corresponding to nearly the same as the maximal warpage response region; it should be remembered that the die stress is due to a combination of bending and stretching or compression.

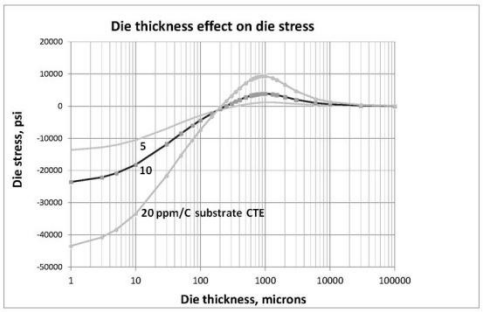



**Figure 16. Die stress on upper surface of flip-chip die after typical assembly, shown as a function of die thickness, for a several substrate CTE values.**

The negative values indicate compression of the die, and it is observed that very thin die can be readily compressed by the substrate and underfill. The scope of this paper does not include extensive detail for thin embedded silicon devices, but the implications are clear. Buckling and fracture are potential failure modes for very thin devices, and the effect of significant silicon compression on device function may become important.

The effect of die thickness on the interaction stress of the die to underfill is complex and interesting as well; corresponding results are given in Figure 17.

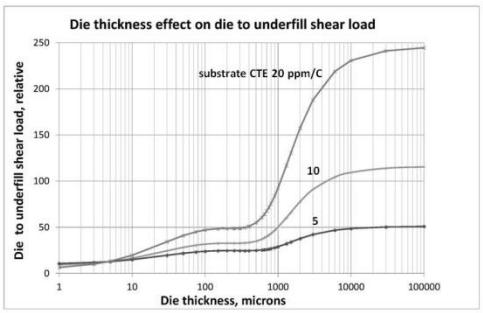



**Figure 17. Shear loading between the lower die surface and underfill after typical assembly, shown as a function of die thickness, for a several substrate CTE values.**

Stacked devices (for example, silicon on silicon interposer) can become quite thick, say 1mm or more. If that is attempted, one must pay careful attention to the design parameter influence on the resulting interaction stress, as there is a sharp increase analogous to the increase noted in Figure 5.

There are many other design attributes which can be associated with an electronics application, for example the addition of a heatspreader or overmold, which can further complicate the analysis. As mentioned, designing for assembly process yield can also become a significant design factor. Also, there are numerous other factors which can drive the packaging design choices to become non-optimal in terms of the simple response metrics shown here. However, achieving reliability which meets and exceeds the overall needs of the application is always the ultimate goal in packaging design. The use of flexible organic materials, which enables extreme package electrical performance and shrink, does not limit reliability when the application is properly designed. The aim of this work was to show some of the outcomes related to a few simple design choices; many more influences and response metrics exist, and highly detailed analysis of specific situations is generally required to achieve high reliability in challenging applications.

## SUMMARY AND CONCLUSIONS

Advanced Electronics Packaging for A&D, industrial and medical applications is driving the need for novel substrate materials, ultra high density assemblies and unique form factors. Substrate materials and construction are key to overall package performance and

reliability. By integrating the building blocks of SiP - advanced substrate technology, embedded passives and actives – coupled with concurrent engineering design-for-manufacture (DFM), advanced packaging solutions have been successfully implemented to reduce electronics volume and advance the capabilities of medical device technology. Combining physics analysis with substrate design, DFM techniques enable advanced flex circuit constructions, processes, fixtures, and equipment to be devised so as to provide fine line circuitry and accommodate mounting of modern silicon flip-chip die having ultra fine pitch and thin constructions. For advanced flex circuit constructions, processes, fixtures, and equipment must be devised to provide fine line circuitry and accommodate mounting of ASIC die having ultra fine pitch flip chip assembly. Using semi-additive plating processes (pattern plating), fine-feature circuitization can be achieved to support the requirements for extremely miniaturized, atypical form factors.

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