Design for Testability (DFT) to Overcome Functional Board Test Complexities in Manufacturing Test

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Abstract

Manufacturers test to ensure that the product is built correctly. Shorts, opens, wrong or incorrectly inserted components, even catastrophically faulty components need to be flagged, found and repaired. When all such faults are removed, however, functional faults may still exist at normal operating speed, or even at lower speeds. Functional board test (FBT) is still required, a process that still relies on test engineers' understanding of circuit functionality and manually developed test procedures. While functional automatic test equipment (ATE) has been reduced considerably in price, FBT test costs have not been arrested. In fact, FBT is a huge undertaking that can take several weeks or months of test engineering development, unacceptably stretching time to market. The alternative, of selling products that have not undergone comprehensive FBT is equally, if not more, intolerable.

Design for Testability (DFT) techniques are effective ways to reduce FBT test programming complexity. This is accomplished by improving Observability and Controllability attributes. This often implies adding test points, but access improvements can be gained from many design activities. These include JTAG/IEEE-1149.1 boundary scan access wherever they happen to be present. We examine some failure modes and show that many of them need to be tested with FBT. Still others require DFT to enable FBT to detect them. We suggest a more pro-active approach that purposely places boundary scan access to internal circuit locations necessary or instrumental for better tests. This approach requires test and design collaboration <u>during</u> the design process. Designers must understand the test requirements early enough to add the necessary access points so that path sensitization and diagnostic attributes are also improved. When complex measurements are needed to ensure functionality, increased cost of both test equipment price and lack of availability may be limiting factors. Designs can usually accommodate existing ATEs and test set ups, provided this is done <u>during</u> the design process. We propose a parallel design and test engineering activity. We argue that while the potential benefits are great, the added costs are insignificantly small.

Introduction

For new products that we manufacture we need to answer three key questions:

1. Was the product designed correctly?
2. Was the product built correctly?
3. Do all the parts (components and ICs) work correctly?

Design verification tests (DVTs) are performed by designers before the product is manufactured. Though the tests are long and complex, there is no need to automate them since they will be run only once. They include environmental stress screening (ESS) tests that provide information about the likelihood that the product will continue working properly for some time and under certain environmental strain. While the tests functionally exercise the unit under test (UUT), as we will discuss in greater detail, this is not a functional board test (FBT) that is the subject of this paper.

Manufacturing Test Strategies

Manufacturers, especially contract manufacturers who test various circuit boards they did not design, tend to limit tests to the last two questions. Primarily, they want to know that the fruit of their labor, the assembly of the product, did not create defects. Towards this end, they utilize equipment, such as automatic optical inspection (AOI) and x-ray (AXI), connectivity testers and in-circuit testers (ICT) with bed-of-nails and flying probe fixtures. They also utilize the IEEE-1149.1 boundary scan devices, often called JTAG.

Manufacturers also want to know that the components they assembled are still working to the extent that the component manufacturers assured they would. Naturally, the assembly process could inflict harm to the components during soldering, but it is also possible that the components were either faulty coming from the component manufacturer or became faulty in storage and handling. It is also possible that the assembly did not properly install the component – such as missed installation, misoriented, or mistaken for a different component. Testing for basic component operation is possible with ICT and with JTAG. The extent to which ICs and other components are tested with these tools is limited. We can probably tell if a component is catastrophically defective, but that is not the same as verifying that they work properly. Moreover, the components were tested by their vendors for operating in a different environment – one in which they operated alone. On the circuit board, they are now operating together with other components, where new situations and functions are created by the interoperability of parts. This aspect of parts testing is not performed by ICT and only partially supported by JTAG.

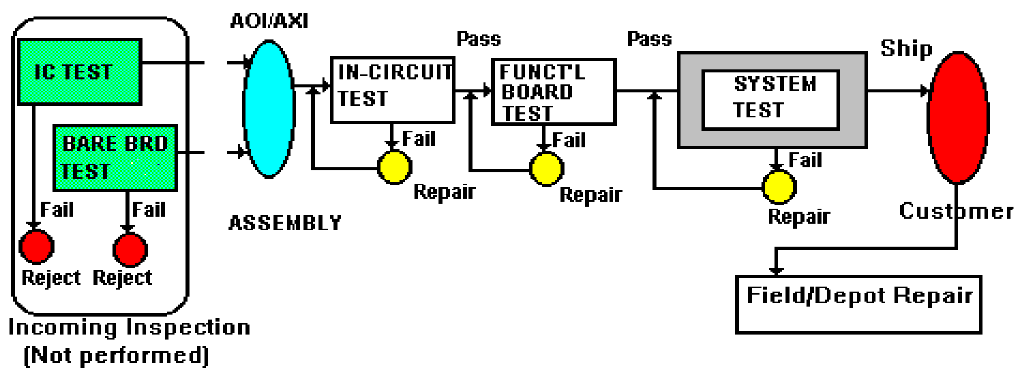

Figure 1 – Common Manufacturing Test Strategy

Figure 1 depicts a common manufacturing test strategy. [1] Components and bare printed circuit boards (PCBs) are tested by their vendors thoroughly with acceptable quality levels (AQLs) such that defect levels (DLs) range from about 5 parts per million (ppm) for passive components to 100s of ppm for application specific ICs (ASICs). It is safe to assume that no bare board PCB faults remain before assembly.

The assembly process is monitored by AOI and AXI at several stages in the assembly line. AOI is used prior to wave solder to view the solder paste, to verify that the correct components are inserted, and to view solder joints. AXI is also used to view solder joints, especially for ball grid array (BGA) devices where the pins are buried under the chip. Both AOI and AXI are used for post wave inspection.

Next, ICT tests are invoked. ICT performs a few different tests, including passive connectivity tests, which may be done instead by a Connectivity ATE or by a Manufacturing Defects Analyzer (MDA). Next, ICT makes passive component measurements for resistance, capacitance and inductance, before applying a Safe-To-Turn-On test to ensure that the board will not be damaged by applying power. When power is applied, some analog and digital components are tested. It is important to note important limitations about these tests:

1. The tests are limited to individual components and isolate that component from the rest of the circuit.
2. Access is typically not available to all nodes. Nodes that are accessible to ICT are those that are connected to bed-of-nails pins, test vias, test pads or to boundary scan cells. Typically, only about 70% of the nodes are accessible. Similar limitations, though not as many, exist with flying probe platforms as well. This number can be improved considerably by Design for Testability (DFT) planning, but even then, it is difficult to achieve 100% accessibility.
3. Only some analog parameters are tested, depending on the availability of instruments available to the ICT.
4. Digital components, especially complex components such as processors and memory, are not fully tested – often not tested functionally at all.

It is clear what AOI, AXI and ICT (which we will call AOI-AXI-ICT) can test. They find assembly faults that are essentially under the control of the assembly process. They also find some catastrophic component faults. Before we can call a circuit board "good," however, we should agree on some test related terminology.

Definitions

- ***Function*** is an action performed by a group of components influencing each other to realize an expected result. For example, in a calculator we have the *addition* function, the *multiplication* function, the *power supply* function, as well as several other functions. The same components could be part of and perform different functions.
- ***Functional Test*** is neither an exhaustive duplication of the entire function (such as adding every number to every other number we can on a calculator), nor is it merely a demonstration that one set of numbers can be successfully added. Instead, the goal of a functional test (including FBT) is to demonstrate that normal functionality is not adversely affected by some *defect*. (Most defects, such as shorts and opens, are catastrophic and visible. We include here some defects that may be intermittent or conditionally caused and are not always apparent, such as jitter in a high-speed communication that occurs only if certain combination of events has taken place.) A functional test is performed by applying strategically selected sequences of stimuli that should yield expected responses for known good or for known defective circuits. In some cases, it is easier to demonstrate the existence of a defect and in others it is easier to demonstrate its absence and the test engineer developing the test can strategically decide which one to use.
- ***Fault*** is a physical condition. It is a defect or abnormal condition that may cause a reduction in, or loss of, the capability of a functional unit to perform a required function ([International Electrotechnical Commission IEC 61508]. Faults can be generalized and categorized, such as a short, open, stuck-at-0, and stuck-at-1 fault, adjacent

pin short or dead component. Moreover, they are quantifiable and therefore a test can be graded by the percentage of (certain) faults it can detect. A threshold can be set that a test must be capable of detecting, say 95% of all stuck-at-0 and stuck-at-1 faults. Furthermore, fault isolation requirements can also be set, so that the test can identify the exact fault in, say 90% of the cases in which it detects faults.

- ***Failure*** is an event, as distinguished from "fault" which is a state. It is the functional manifestation of a fault, though not all faults result in a failure and not all failures are caused by a fault.
- ***Failure Mode*** is the physical or functional manifestation of a failure [ISO/IEC/IEEE 24765]. Per the American Society for Quality (ASQ), they are modes, in which something might fail. For example, “flat” is a common failure mode for tires. “Corrosion” is a common failure mode for old wiring. “Delays” are common failure modes for timing circuits. “Adjacent cell coupling” is a significant failure mode for RAMs. “Instability,” “attenuation” and “jitter” can all be failure modes for oscillators.
- ***Functional Failure Mode*** is a failure mode regarding the effect on the function that is considered. For example, failure to actuate or a spurious failure. The functional failure modes do give information about the effect, but not about the causes.
- ***Structural Failure Mode*** is a failure mode that includes the failure cause. For example, “frozen sensor” or “amplifier adjustment too low”.
- ***Design for Testability*** is a philosophy incorporated in the design of electronic circuits which takes into consideration the post-design testing phase, and which attempts to reduce the effort and cost of testing. [1]
- ***Failure Mode Effects [Criticality] Analysis (FME[C]A)*** is a document used to generalize failure modes - especially ones that can potentially affect the end user - and predict the consequences or effects of those failures. Criticality analysis is done when lives are at stake. FMEAs also include causes and probabilities or frequencies of occurrence. Some government agencies, such as the Department of Defense (DOD), the Food and Drug Administration (FDA) and the Nuclear Regulatory Commission (NRC) require that FMEAs be prepared for many of the products they purchase. It is recommended that FMEAs start early in product development and grow with greater details of the design. If that timing is followed, FMEAs are precious inputs to DFT analysis.

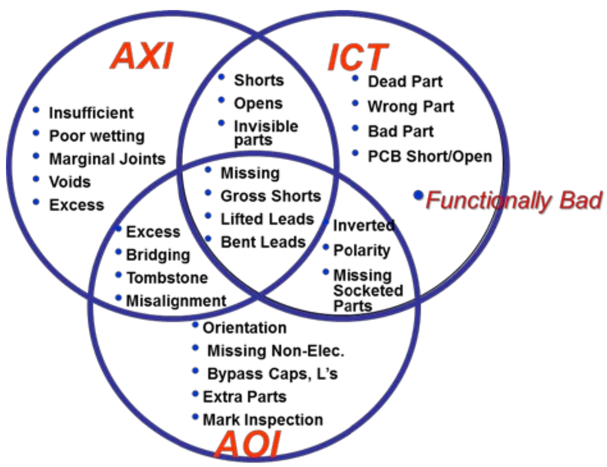

Figure 2 – Failure Modes Detected by AOI, AXI and ICT. Some Functionally Bad Circuits Fall Outside [8]

Functional Board Test (FBT)

Figure 2 shows the failure modes detected by AOI-AXI-ICT. “Functionally Bad” circuits, however, are only partially detected by ICT. When ICT is complete in Figure 1, little if any circuit board functionality has been tested. This is significant because the next stage of test, Functional Board Test (FBT) is a great deal more complicated and is often incorrectly or insufficiently performed, or worse yet, completely skipped. There are several reasons that FBT is a controversial stage in manufacturing test. Here are some of the reasons why many manufacturers limit or eliminate FBT:

1. FBT is not well defined or understood. FBT should not be a repeat of the design verification test. In fact, while DVT is intended to show correct operation, FBT is the opposite as it tries to show incorrect operation (*failure*) and to identify and diagnose the root cause *fault*. *Failure modes* provide a goal for FBT in that they aim to prove (or convincingly demonstrate) the existence or absence of the failure mode. Additionally, FBT needs to identify the fault or at least the repair action that will eliminate the failure mode. Since the number of failure modes is subjective, quantitative analysis of what constitutes a complete test is also subjective.
2. Functional tests are complex and time-consuming to develop. They require a thorough understanding of the circuit operation for both good and faulty circuits. It has been said that a test engineer developing functional tests needs to understand the circuit orders of magnitude better than the designer, since the designer only needs to know how a

good circuit operates, whereas a test engineer needs to know the hundreds of ways that circuit can fail as well. Because circuits are increasingly more complex, simulators are not able to model today's circuits, leaving the test engineer with the error-prone process of having to manually predict responses to stimuli. Added to this is a lack of good documentation, resulting in the amount of time needed before such a test is complete to be prohibitive. Only proper test and testability planning (DFT) can mitigate the complexity, without which FBT may well be unaffordable.

3. Contract manufacturers can readily price test development and equipment costs for AOI-AXI-ICT. For FBT only the test equipment cost can be predicted with confidence. Consequently, many contract manufacturers prefer not to get involved with FBT. The vendor, whose design engineer has moved on to the next design is not readily available to document or explain the operation of the product. The test engineer is on his/her own to develop the test, often complicated by a lack of DFT, which can render some circuits undetectable or difficult to detect.
4. It is well accepted that the clear majority of the faults have already been detected before the circuit reaches FBT. Numerically, 90% of the faults are structural and can be found by AOI-AXI-ICT. [2] (Although [2] is a 15 year old source, we could not find anything to dispute it. Because complexity of circuits has increased, I would expect that perhaps there are more functional failures, so only 85% of all the faults would be covered in Figure 2). Since ICT can detect no more than half of the 10% to 15% functional faults remaining, FBT will detect 5% to 7.5% of the remaining faults (provided those faults are testable by FBT). To reduce the test costs, including the time to market impact of FBT, and considering that only some of these are in fact faulty, managers sometimes decide to risk sending out some circuit boards with these faults and instead deal with the cost of customer returns. In their view, the benefits of preventing a few more faulty products is not worth the expense of a FBT operation.

From the above arguments, it is not surprising that manufacturing managers are not eager to do FBT, even if they are concerned with potential escapes. However, to better understand the impact of escapes, consider equation (1) from [3].

$$DL = 1\ Y^{(1-T)} \qquad (1)$$

Y indicates the true yield, that is, the probability that a manufactured circuit is defect-free.
Defect level ***(DL)*** is the probability of a defective circuit even after it has been tested and repaired.
T is the fault coverage.

Let's consider an example production where we produce some boards with no faults and some with multiple faults, with an average of 1 fault per board (FPB). Poisson Distribution is often used to convert the average number of FPB to the distribution of boards with 1 fault, 2 faults, or to 0 faults – the case of fault-free boards. [4] Fault-free is the incoming yield (Y) and with 1 FPB it is 36.8%. When we run AOI-AXI-ICT that has a combined fault coverage of 90% it will eliminate all faults except those it could not detect, which is DL in equation (1).

- With Y = 36.8% and T=90% for AOI-AXI-ICT, DL = 9.5% will still be faulty after ICT

If, in an attempt to ship better quality products, we increase production quality by say 2/3 - a noble goal that probably carries a high price tag – we will substantially reduce the outgoing defect level, DL. Plugging in the numbers we find that

- For Y = 61% (2/3 above 36.8%) and for T = 90%, DL = 4.81% or ***about 50% better***

If instead of the increased production quality, we introduce FBT and increase our coverage by 5% to 95% then

- Y= 36.8%, With FBT T=95%, DL = 4.9% ***– also about 50% better***

So, the value of FBT increasing fault coverage by only 5% has essentially the same impact as improving production quality by 2/3 or 67%! In this light, we can see that FBT is indeed valuable as it would likely cost much more to improve production quality by 67% than to introduce FBT.

Figure 3 also illustrates the need for FBT. [5] As shown, we start with Y_{in}=36.8% from production and after AOI-AXI-ICT covering 90% of all faults, the output yield (Y_o) = 90.5%. This is consistent with equation (1), which showed the DL remaining at 9.5%. (Figure 3 also calculates an apparent yield (Y_a), which indicates that it is the yield that would appear to us by just looking at the results after ICT if we did not know Y_{in}.)

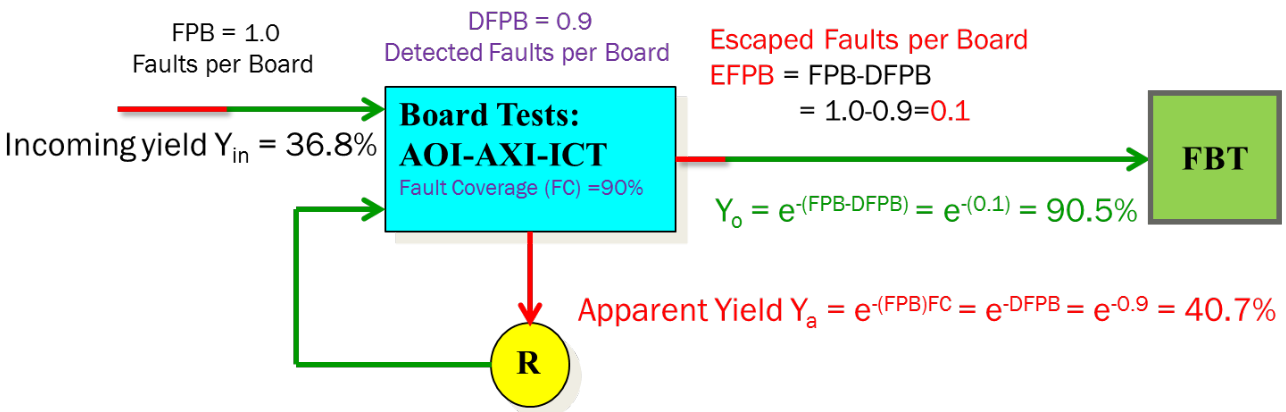

Figure 3 – Yield analysis showing that 9.5% of the boards are still faulty after AOI, AXI and ICT

Let's consider the economic value of FBT. As shown in Figure 4, the cost of escapes to later stages increases by orders of magnitude. If a fault exists during board (subassembly) test, but we don't fix it at the cost of \$10.00, it will cost us \$100.00 to fix that same fault at the system level test, a \$90 difference. Since Y_o of the ICT test is Y_{in} of FBT, we can calculate FPB entering into FBT with equation (2).

$$FPB = -\ln (Y_o) = \ln (90.5\%) = 0.1 \text{ faults per board} \qquad (2)$$

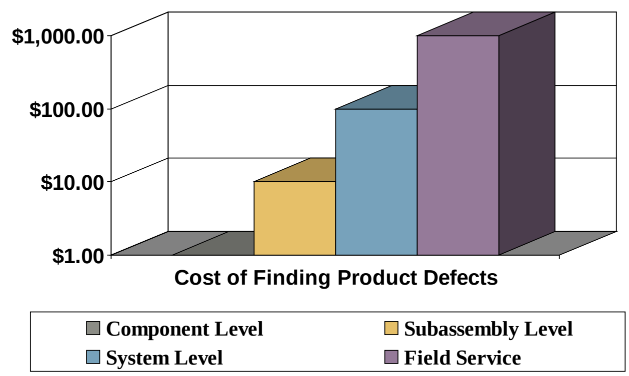

Figure 4 – Order of Magnitude (Times Ten Rule) of Test Economics

If we do *not* use FBT, we incur an additional cost of \$90 for each fault that escaped AOI-AXI-ICT because of the higher cost at System Test and repair than at FBT. Using Poisson Distribution [4] we find that for 0.1 FPB about 90% of the boards will be fault free, leaving about 10% to have one or more fault. If we have a production of 1,000 boards then 100 boards that escaped AOI-AXI-ICT and wound up in System Test are still faulty. The escape cost us \$90*100 in extra cost to find the fault at system test rather than at FBT, amounting to \$9,000 for the lot. Even if FBT only detected 95% of these faulty boards, it would have saved us 95% of \$9000 = \$8,555 or \$8.56 per board. If the 1,000 boards are monthly volumes, FBT can potentially save \$102,000 per year.

A similar case study from Sandy Bridge [6] reports that approximately 2,400 boards that could not be fixed at all prior to using FBT, were then repaired, saving approximately \$121,000 for the company.

Design for Testability

The potential savings notwithstanding, it is fair to be concerned about the high cost of developing FBT tests. Generally, and increasingly, the FBT test program is a major undertaking in terms of time and effort as shown in Figure 5. The graph shows that effective test coverage greatly diminishes as we go above 90%. In fact, the engineering effort, time or cost to get from 90% to 95% doubles, and would probably double again to get to 97%. The graph also shows, that DFT and built-in self-test (BIST) can linearize these costs.

Table 1 – Failure Modes and Failure Probabilities of a) Multiplexers, b) RAMs and c) Microprocessors [11]

IC: Integrated Circuit—Digital—Multiplexer				
Primary failure mode	**Secondary failure mode/ failure mechanism**	**No. of failures**	**Total no. of failures**	**Failure probability (%)**
Parametric failure	Degraded operation/improper output	47	101	90.99
	Degraded operation	4		
	High insertion loss	27		
	Output low/low radiofrequency output	13		
	Isolation failure/low isolation	4		
	Electrical leakage	2		
	Output high	1		
	Unknown	3		
Functional failure	Electrical failure/signal timing error	2	4	3.60
	Data bit failure	1		
	Electronic destroyed in analysis	1		
Stuck high	TTL stuck high	2	2	1.80
Stuck low	TTL stuck low	2	2	1.80
Mechanical failure	Die cracked/fractured	1	1	0.90
Open	No response	1	1	0.90

IC: Integration Circuit—Digital—Memory—RAM: Random Access Memory—SRAM				
Primary failure mode	**Secondary failure mode/ failure mechanism**	**No. of failures**	**Total no. of failures**	**Failure probability (%)**
Functional failure	Excessive water vapor/chlorine	64	134	84.28
	Data word incorrect	24		
	Data bit failure	21		
	Signal timing error	14		
	Intermittent operation	9		
	No output	2		
Parametric failure	Degraded operation/improper output	3	8	5.03
	Degraded operation/output bits would toggle from 0s to 1s	1		
	Degraded operation/address reads incorrect data; least-significant bit (LSB) appears locked	1		
	TTL floating	2		
	Output high	1		
Open	Unknown	6	7	4.40
	No response	1		
Stuck high	TTL stuck high	2	5	3.15
	Output stuck high/corrosion; open internal lead	1		
	Output stuck high/corrosion; two pins stuck high	1		
	Output stuck high/two LSB addresses locked high	1		
Short	Unknown	3	3	1.89
Stuck low	TTL stuck low	2	2	1.26

IC: Integrated Circuit—Digital—Microprocessor				
Primary failure mode	**Secondary failure mode/ failure mechanism**	**No. of failures**	**Total no. of failures**	**Failure probability (%)**
Parametric failure	Degraded operation	128	132	61.97
	Electrical leakage	3		
	Intermittent operation/unstable	1		
Open	Open circuit pin 2	3	41	19.25
	Unknown	38		
Mechanical failure	Die attachment failure/particle impact noise detection failure; loose die attach	4	22	10.33
	Mechanical anomaly	14		
	Broken pin/mechanical overstress	3		
	Cracked die	1		
Functional failure	Data word failure	4	11	5.16
	Electrical failure/signal timing error	4		
	Intermittent operation	2		
	Data bit failure	1		
Short	Multiple bridging between metallization Paths	1	7	3.29
	Unknown	6		

Table 1 shows primary and secondary failure modes and occurrences presented to the Nuclear Society [11] for three devices often used in today's circuits. We find that multiplexers tend to fail most with "Degraded operation," "High insertion loss" and "Low RF output" failure modes. Most of these parametric failures require FBT to detect. Similarly, the "Functional failure" modes constitute 84% of failure modes in RAMs and SRAMs. With microprocessors about 62% of the occurrences are parametric failures.

While the results of Table 1 were collected on units returned from the field, it is not clear whether these faults were in all cases the result of aging. Some faults may have been present all along but were escapes from manufacturing and did not exhibit themselves until the product was fielded for some time

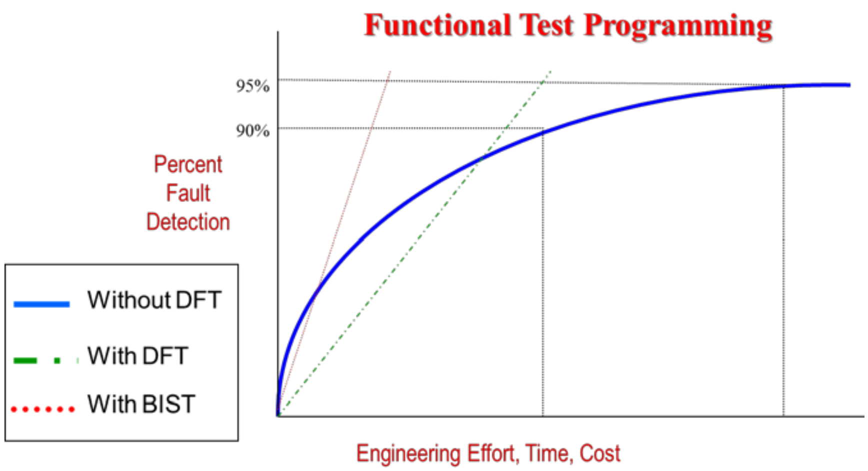

Figure 5 – Test Programming Costs for Various FBT Fault Coverage with and without DFT and BIST [1]

DFT has been discussed, promoted and standardized throughout the engineering profession. [7], [8], [9] Yet, it is a recurring subject for discussion before it is implemented. Often, DFT techniques are only considered after the design is complete and by then the redesign costs and time to market impact make it unprofitable or unachievable.

DFT is a design activity that is usually promoted and influenced by test engineers who are concerned with the difficulty of testing they will face unless the design is testable. The two unresolved questions in many organizations are: who will do DFT and when? The correct answer to the first question is that DFT must be ultimately performed by design engineers, making test engineers recipients (perhaps advisors), but not implementers. Since it is a design activity, DFT must be implemented early in the design to prevent redesign for testability. The cost of DFT is not well understood, because it depends on many factors. For example, the first time a design engineer uses boundary scan (s)he will undergo a learning cost that will not be required for subsequent designs employing this technology. Similarly, other DFT techniques can become second nature to the designers. Moreover, as many circuits are built upon previously designed circuits, once DFT has been incorporated, future generation designs will already be DFT-ready.

Because many of the ICs used today already come with JTAG/IEEE-1149.1 boundary scan, some degree of DFT is often incorporated without anyone even trying. So, despite the contentious nature of DFT, circuit board manufacturers have improved testability. Unfortunately, these techniques have benefitted mostly AOI-AXI-ICT. Few of the techniques, however, have been geared towards failure modes that FBT is supposed to test. We will now examine failure modes and identify those that require FBT to detect and diagnose. In those cases, we will discuss how DFT could assist to reduce the test program development effort and cost.

Failure Modes for Functional Board Tests

Several failure modes in electronic circuits have been studied. [10] The taxonomy of failure modes in general is still not well defined. Attempts to do so have been made in the nuclear energy industry. [11], [12], [13], [14] To better understand where FBT needs to focus its tests, we will include some of their classifications and findings.

Table 2 – Failure Modes and Detectability of Circuit Elements

Components	Failure Modes	Detectable by AOI, AXI, ICT	Detectable by FBT	DFT Considerations
General	Stuck-At Faults	Shorts, Opens but not all stuck-ats	Depends if accessible	Improve controllability and observability by utilizing boundary scan cells as controllability, observability and diagnosability test points
	Bridging Faults	ICT and even connectivity tests can readily find faults with adjacent pins shorted	Not easily	Make such faults accessible to ICT and/or boundary scan
	Delay and State Transition Faults	Not unless the delay is within a faulty IC - not likely if IC was well tested	Yes, to the degree that the FBT speeds can detect the delay	DFT may need to supply some pulse catching mechanism and/or BIST circuitry to test in situ
Capacitors	Shorted	ICT can detect especially for electrolytics.	Only its effect on other circuits	
	Wrong capacitance	Probably not	Only its effect on other circuits	Prepare for critical failures by using some delay testing mechanisms.
	Parasitic resistance	Probably not	Only its effect on other circuits	
Resistors	Open	With ICT.	Only its effect on other circuits	
	Shorted	With ICT.	Only its effect on other circuits	
	Wrong value	With ICT.	Only its effect on other circuits	This may not be easily accomplished with FBT unless specific DFT procedures are used.
Inductor and Transformer windings	Open	With ICT.	Yes.	
	Shorted to core	Not easily - high temperature or smoke test	Not easily - high temperature or smoke test	Safeguards preventing damage or injury should be part of DFT
Diodes	Open (for rectifying diodes)	With ICT.	With analog tests	
	Shorted (for zener diodes)	With ICT.	With analog tests	
	Voltage/Current surge due to transients	Maybe with ICT	Probably	Analog DFT
Oscillators	Wrong Frequency	Maybe with ICT	Probably yes, with the right instrument	
	Rise time and Fall time	Probably not	Probably yes, with the right instrument	Delay measuring DFT techniques
	Phase noise and Jitter	No.	With Bit Error Rate tester	DFT can help make this testable
	Current and Power Stability	Probably not	Probably yes, with the right instrument	Make such faults accessible
	Temperature Stability	No.	Probably yes, with the right instrument	
A/D and D/A Converters	Power levels	Maybe with ICT.	Yes with proper instruments	
	All bits stuck for D/A	Maybe with ICT.	Yes.	
	Only certain bits stuck for D/A	Maybe with ICT.	Yes.	Some DFT techniques can help
	Over maximum voltag for A/D	Maybe with ICT.	Yes.	
	Bit-wise conversion of A/D	Maybe with ICT.	Yes with proper instruments	Some DFT techniques can help
RAMs	Output Levels	With ICT.	Yes.	
	Parametric Faults	Probably not.	Maybe.	Use Memory BIST
	Power Consumption	With ICT.	Yes.	
	Noise Margin	No.	Maybe, depending on available instrumentation	DFT should be used to find noise margins for critical applications
	Data Retention Time	No.	Maybe, depending on available instrumentation	Use Memory BIST
	Stuck Faults in Address Register	Maybe with ICT.	Yes.	
	Stuck Faults in Address Decoder	Maybe with ICT.	Yes.	
	Stuck Faults in Data Register	Maybe with ICT.	Yes.	
	Cell Stuck Faults	Maybe with ICT.	Probably, but testing for all such faults would not be feasible	Use Memory BIST
	Adjacent Cell Coupling Faults	No.	Pattern sensitivity between a pair of cells is possible but is a long test.	Use Memory BIST
	Pattern-Sensitive Fault	No.	The presence of a faulty signal depends on the signal values of the nearby points – Most common in DRAMs. Need to test with refresh cycle.	Use Memory BIST
Programmable Logic - PLAs and FPGAs	Stuck Faults	Only at I/O	Testing the function of the device to verify proper synthesis and operation	Use internal scan and BIST to ensure proper internal operation. Use boundary scan which is usually available and enhances FBT. Often unused FPGA pins serve as extra board test points as they have boundary scan.
	Crosspoint Faults	No.	Same as for Stuck Faults	Same as for Stuck Faults
	Extra/Missing Transistors	No.	Same as for Stuck Faults	Same as for Stuck Faults
	Bridging Faults	ICT and AXI if IC is ball grid array.	Internally to IC - maybe due to misprogramming	Same as for Stuck Faults
High Speed I/O	Single wire opens or resistive	With ICT.	Yes.	
	Shorts between signal pairs	With ICT.	Yes.	
	Leakage	No.	Yes with proper test instrument	
	Clock failure	Maybe with ICT.	Yes with proper test instrument fo	May use DFT and BIST circuitry for high speed test
	Tx drive weaken	Maybe with ICT.	Yes with proper test instrument fo	May use DFT and BIST to pair Tx and Rx to mutually test each other
	Rx sensitivity weaken	Maybe with ICT.	Yes with proper test instrument fo	May use DFT and BIST to pair Tx and Rx to mutually test each other

Failure Modes, Functional Board Test and Design for Testability

A good way to assess the benefits of FBT is to consider the many failure modes that cannot be detected by AOI- AXI- ICT. Table 2 includes a larger number of failure modes, including many that can only be detected by FBT.

We can see that passive components can be detected by AOI, AXI and/or ICT, but as we begin to look at more complex circuit types, functionality becomes more important. For some of these functions, even FBT is only marginally effective. That is why we included a column in Table 2 that discusses needs for DFT and BIST to assist detection. For example, for RAMs many of the functional tests are either difficult to accomplish or become prohibitive. For that reason, memory BIST (MBIST) is an essential capability. We recommend as a matter of policy that designers be urged to use memory with MBIST and buying any memory without it should be an exception that needs to be justified.

Similarly, we would encourage a policy that whenever possible, designers choose boundary scanned components. Boundary scan has assisted manufacturing test primarily with ICT. It can, however, become a very helpful tool for FBT. Recently, boundary scan has been shown to also provide a health monitoring and a fault isolation capability on aircraft, testing even while normal functions are being performed. [16] This could be a valuable tool to improve prognostic health management (PHM) for aging circuits and provide information to mitigate false alarms and No Fault Found (NFF) events. [18], [19]

Managing Design for Testability with Functional Board Test

Reducing test costs usually involves reducing test equipment costs and outsourcing to contract manufacturing is a good way to getting well manufactured products from the manufacturers. Contract manufacturers, who produce circuit boards for several customers and applications want test equipment that will be universally applicable to all their customers. It is a bonus that with AOI, AXI and to some degree even with ICT, there is no need to have an intimate familiarity with the product's functionality. By not performing FBT the contract manufacturer is only required to assure its customer that the circuit board was built correctly (without assembly faults) and not that it is ready to be sold or integrated into the system housing it. DFT to the manufacturing organization is a necessary but incomplete set of techniques that will make it easier for AOI-AXI-ICT to detect faults that may have been inserted during the manufacturing process. Other DFT techniques and guidelines that pertain to functionality are not of great concern to the manufacturer, but should be.

DFT and BIST techniques can assist FBT to achieve three very important areas of test cost reduction:

1. **DFT reduces test equipment costs.** This cost is easily recognized. DFT can find ways to reduce the number of test instruments needed, the price of the instruments and the logistics cost of test equipment training, use, maintenance and disposition. If DFT can reduce the complexity and the cost of the automatic test equipment (ATE) - perhaps by creating BIST circuitry on the board - then it results in savings visible to corporate management. In fact, DFT and BIST could take the place of ATE and of FBT.
2. **DFT reduces the cost of test program development.** As we have seen in Figure 5, test program development is an expensive undertaking that can be substantially reduced if DFT is employed, even more so when BIST is employed. In most cases the cost of test program development is more expensive than the cost of the equipment over its lifetime, but because the costs are not necessarily covered by the same budgetary line items, they are often obscured. Nonetheless, DFT can be instrumental in reducing test development costs considerably. For example, DFT and BIST should be able to reduce test development times from months to days and engineering costs should be reduced in the same proportion. Additionally, this reduction will result in faster time to market, which also has important benefits.
3. **DFT reduces test escapes.** We have seen that test escapes can be quite expensive even without taking the cost of customer dissatisfaction into account. The recent case of a smartphone manufacturer's batteries catching on fire attests not only to the cost of escapes, but even more importantly that the cost of the wrong "fix" that company undertook when replacing the battery for millions of its customers failed to change the outcome. [17] Then, with no understanding of the failure mode that caused the problem, that company chose to recall its smartphone product line at an estimated cost of about $5 billion to date, plus a $15 billion loss to its stock value. Some estimates believe that this debacle will cost the company $17 billion in expenses before the product is fully removed. This demonstrates an important factor that test management must consider, namely, that the cost of failures can far exceed the cost of the products that fail! If with about 170 faulty units the company incurs $17 billion dollars of expenses, then each bad smartphone cost $100 million in penalties, while the manufacturing cost was probably no more than $100.

> Basically, the penalty was a million-fold! Perhaps DFT would not have uncovered the cause, but it may have, or the DFT analysis would have hinted something that was obviously overlooked, since to date there is no indication that anyone knows the root cause.

How does DFT happen in an organization? Since DFT is a *design* activity, it should be performed during the design. It is also true that the motivation for DFT comes from test engineering and therefore test engineers should be part of the DFT process. This is not to imply, however, that the designers first complete a design, have test engineers "check" it and file their complaints and suggestions. Instead of introducing design changes, proper DFT management teams design and test engineer during the design. For example, many DFT tasks require that a test strategy and perhaps test equipment have already been selected, yet that selection cannot be made unless the test engineer can rely on the DFT to be in place. So, instead of a reiterative process, designers and test engineers need to work together so that the test equipment, the test programming and the testability of the design are coordinated. To achieve this, management must facilitate this team effort.

To initiate the process, designers and test engineers can develop a set of failure modes, or even a full FMEA very early in the design – perhaps at the block diagram stage or even before. The failure modes of blocks, such as Power Supplies, Memory, Microprocessors, FPGAs, and I/O Ports may provide sufficient information about the test strategy and equipment that will be used. Some test equipment with long lead times can be procured, while others with a high cost can be replaced by a lower cost equipment if certain DFT techniques are employed. That tradeoff can be dealt with early and will involve designers, test engineers and their managers. As the design is detailed further, including the design of circuits within the FPGA, the set of failure modes will grow and considerations on the best way to test them will also be defined. The tradeoff between design and test considerations and constraints will be an ongoing process. During the design phase, test engineers can develop some, if not all the tests, including FBT tests. In fact, little if any additional time will be placed on either designers or test engineers than if they did not have DFT at all. Because test programs are started earlier and because DFT makes it less time consuming to develop tests, it is expected that when the design is complete, the test completion is not far behind. The savings in time to market will probably make up for any additional costs, and it is possible to obtain DFT for little or even no cost at all.

In many organizations, it is difficult to change organizational habits. To take advantage of DFT for FBT, however, we believe that such a change is warranted.

Summary and Conclusions

FBT complicates manufacturing test strategies. While AOI-AXI-ICT find visible and catastrophic faults, FBT is needed to find the more obscure, subtle, and often intermittent faults that can disturb circuit boards. While the clear majority, in fact 90%, of all failures are detectable without FBT we have made a compelling case why this stage of test should not be skipped. The cost of escapes is much higher than the cost of the product or that of test and the penalty of releasing only a few bad units can be devastating. Consider the case of the smartphone that we discussed where only about 170 of the 2.5 million phones manufactured, only about 68 ppm, exploded or bust into flames. Yet it resulted in having the product recalled and discontinued at a cost in the billions of dollars. Would FBT and DFT had mitigated this. Perhaps not, but at least it strongly suggests that failure modes should not be ignored.

In this paper, we focused on failure modes. As studies by the Nuclear Energy Agency show, many failure modes occur in the field that are difficult or impossible to detect without FBT. If FBT is not performed at manufacturing test, they may well wind up failing in our nuclear reactors. We then presented our own set of failure modes. While not all failure modes were included, Table 2 demonstrates a need to have FBT detection for many failure modes. It also demonstrates that some can only be detected if the design is testable.

We ended with a discussion on how DFT should be managed. Having design and test engineers working as a team offers many benefits and we believe it can reduce the cost of the DFT activity. Though we make a convincing case for this team effort, many organizations see this as contrary to traditions and are not eager to adopt it any time soon. We need a cultural change. Rather than view electronics as a collection of the $10 or $15 worth of parts, we need to view it as the potential cause of a tragedy that could come in many forms and at costs far outweighing their original purchase price. It makes no sense to spend $8 to test a $15 product, but it does not have to cost that much.

With DFT, test costs can be lowered while comprehensiveness is increased. As IC manufacturers have done for years, circuit board manufacturers must also invest in better test through DFT.

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Design for Testability (DFT) to Overcome Functional Board Test Complexities in Manufacturing Test

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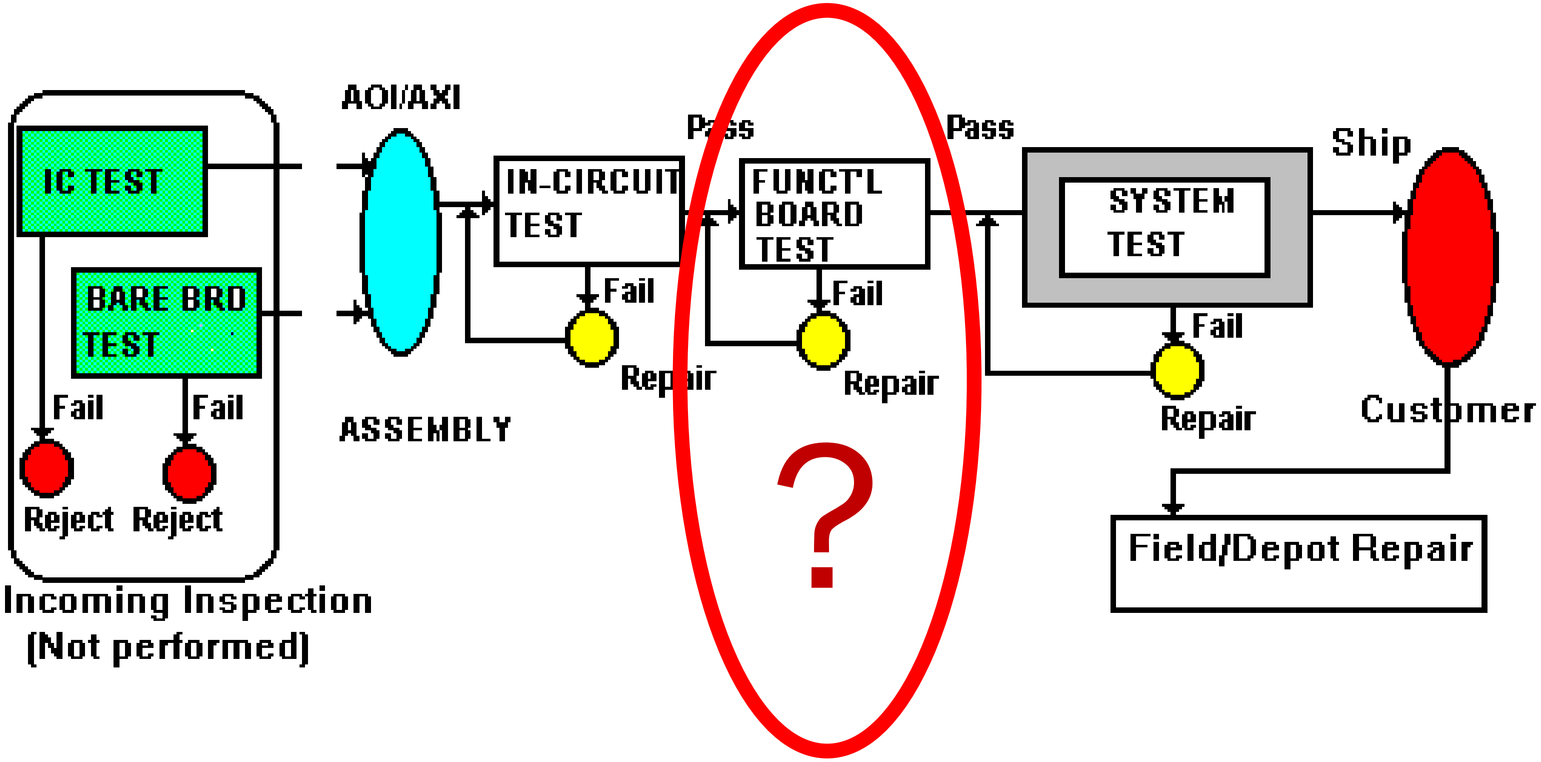
Introduction

- Common Manufacturing Test Strategies
  - *AOI-AXI-ICT*
  - *Functional Board Test (FBT)*
  - *System Test*
- Definitions for Tests
- Failure Modes
- The Economics of DFT for FBT
- Design for Testability and FBT Failure Modes
- Managing DFT
- Summary and Conclusions

Common Manufacturing Test Strategy Using Automatic Test



Definitions

- Function
  - *Action performed by a group of components influencing each other to realize an expected result.*
    - The same components could be part of and perform different functions.
- Functional Test
  - *Neither an exhaustive duplication of the entire function*
  - *Nor is it merely a demonstration that one set of numbers performs a function*
  - *Goal of a functional test (including FBT) is to demonstrate that normal functionality is not adversely affected by some defect*

Definitions

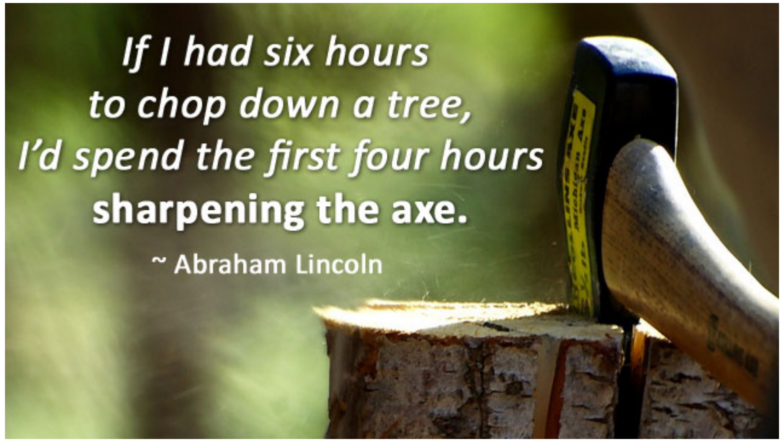
- Fault
  - *A physical defect or abnormal condition that may cause a loss of, the of a functional unit to perform a required function ([International Electrotechnical Commission IEC 61508].*
- Failure
  - *An event, as distinguished from "fault“, which is a state.*
  - *It is the functional manifestation of a fault, though not all faults result in a failure and not all failures are caused by a fault.*

Definitions

- Failure Mode
  - *Physical or functional manifestation of a failure [ISO/IEC/IEEE 24765].*
  - *Per the American Society for Quality (ASQ), they are modes, in which something might fail.*
    - “Flat” is a common failure mode for tires.
    - “Delays” are common failure modes for timing circuits.
    - “Instability,” “attenuation” and “jitter” can all be failure modes for oscillators.
- Functional Failure Mode – Info on Effects but not about Cause
  - *Regarding the effect on the function that is considered.*
  - *For example, failure to actuate or a spurious failure.*
- Structural Failure Mode – Includes Cause on Failure
  - *For example, “frozen sensor” or “amplifier adjustment too low”*

WHAT IS DESIGN FOR TESTABILITY?

- Design for Testability is a philosophy incorporated in the design of electronic circuits which takes into consideration the post-design testing phase, and which attempts to reduce the effort and cost of testing.



Testability = Controllability + Observability

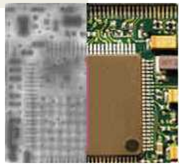
Failure Mode Effects (Criticality) Analysis – FME(C)A

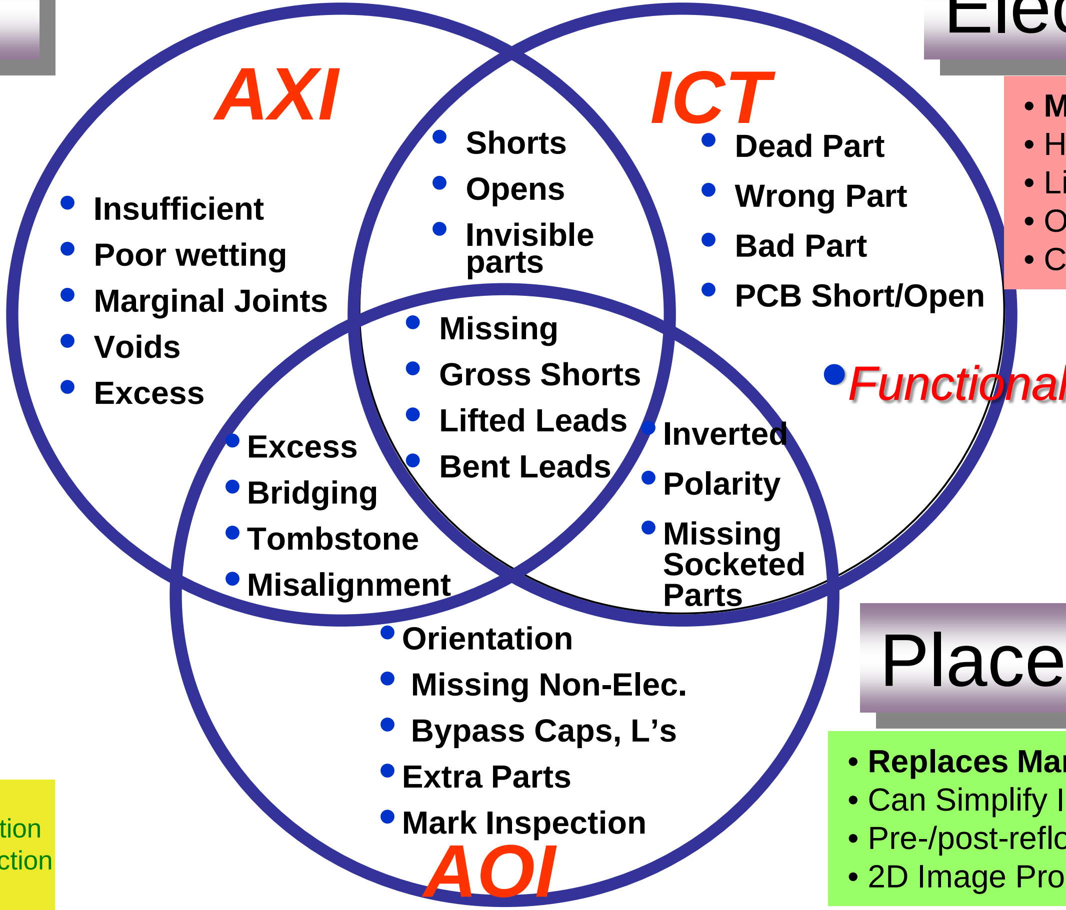
- FMEA is a document used to generalize failure modes
  - *Include causes and probabilities or frequencies of occurrence.*
  - *Some government agencies, such as the Department of Defense (DOD), the Food and Drug Administration (FDA) and the Nuclear Regulatory Commission (NRC) require that FMEAs be prepared for many of the products they purchase.*
  - *It is recommended that FMEAs start early in product development and grow with greater details of the design.*
    - If that timing is followed, FMEAs are precious inputs to DFT analysis.

Test Coverage Choices

Solder

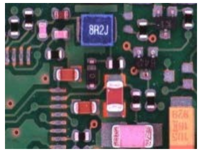
- **>95% Solder Coverage**
- No Access Required
- Reduces Field Failures
- Prototype Inspection
- No Node Count Limits
- 3D Joint Size/Shape





Electrical

- **Most Versatile Solution**
- High Volume Global Mfg.
- Limited Access Test
- On-board Programming
- Combo Test



Placement

- **Replaces Manual Inspection**
- Can Simplify ICT Fixtures
- Pre-/post-reflow, End of Line
- 2D Image Processing of Parts, Joints

ICT: In-circuit Test
AXI: Automated X-ray Inspection
AOI: Automated Optical Inspection

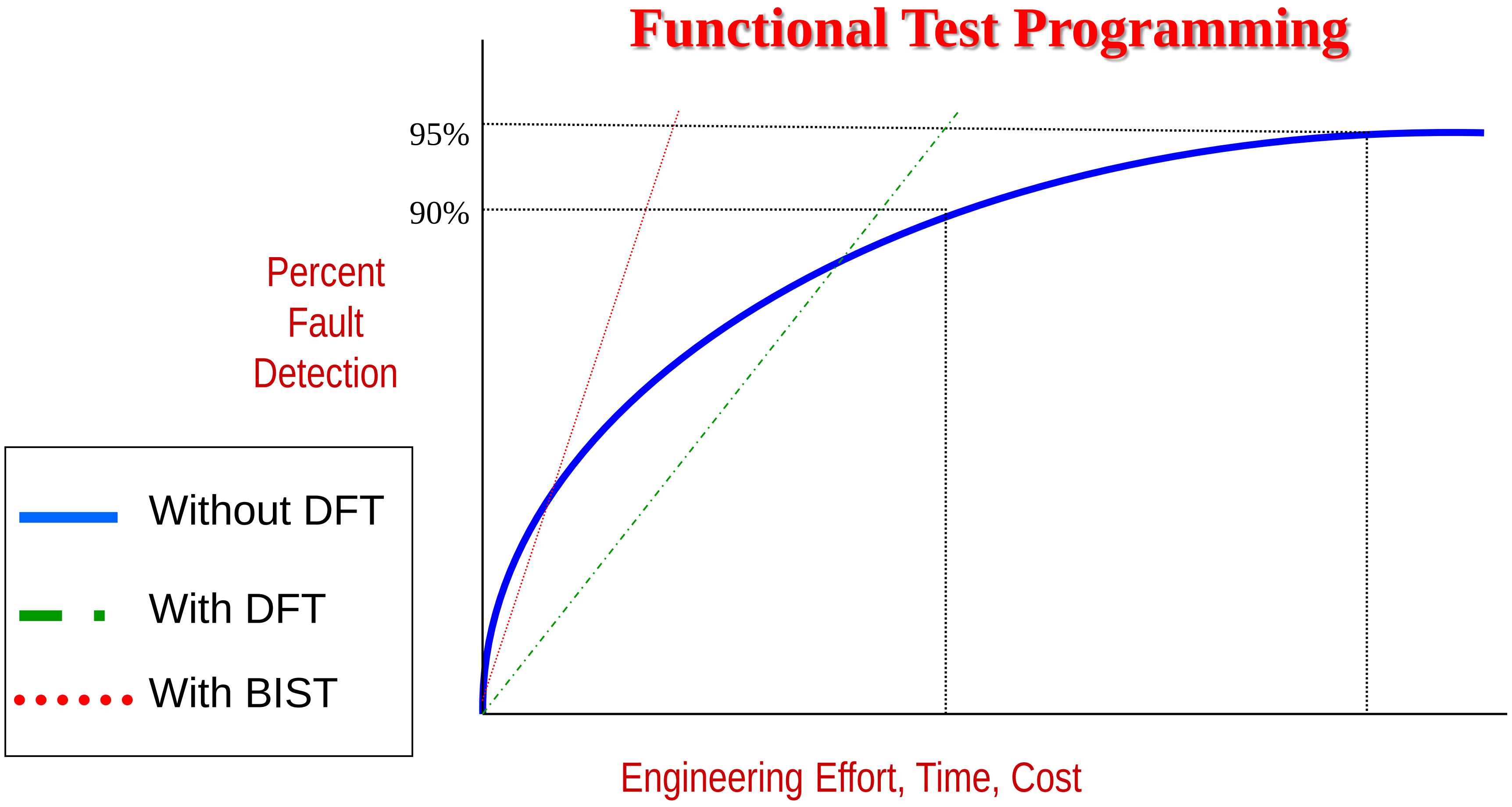
[1]

Fault Spectrum

From: Stig Oresjo, One Billion Solder Joints, Circuit Assembly, Feb. 2001

- Defect Distribution
  - *41% Solder Opens*
  - *20% Shorts*
  - *20% Solder Quality*
  - *8% Placement*
  - *8% Electrical*
  - *3% Other*
- Detection Methods
  - *Imaging detects ~92%*
  - *In-Circuit detects ~76%*
  - *Functional detects ~69%*
- Defect Spectrum
  - *90% Structural*
  - *10% Electrical*

Test Programming - The Greatest Cost of Test



Why Management Doesn't Want FBT?

- FBT is too subjective and faults, failures and failure modes are not quantified.
  - *Can choose failure modes and find x% of those failure modes*
- Functional test are too costly to develop.
  - *True, but DFT can change that*
- AOI-AXI-ICT are easily priced. FBT is not.
  - *True, but DFT can change that too*
- If AOI-AXI-ICT detect 90% to 95% of the fault it doesn't appear to make sense to spend so much for the last 5%.
  - *Test economics does not agree. We will explain why.*

Average Faults Per Board (FPB) to Calculate Yield

Based on Poisson Distribution

$$Y = e^{-FPB}$$

where: Y = Incoming Yield

FPB = Average Faults per Board

- You can calculate FPB from historical manufacturing data
  - *E.g. 100,000 boards with 100,000 faults*
    - Some with 3+ faults, with 3 faults, some with 2 faults, some with 1 fault
    - Some with 0 faults
      - *Fault Free = Y*

QUALITY AS A FUNCTION OF YIELD AND TEST COVERAGE

Let QUALITY (Q) = 1 - DL (DEFECT LEVEL)

– *Using Poisson Distribution, we can derive that*

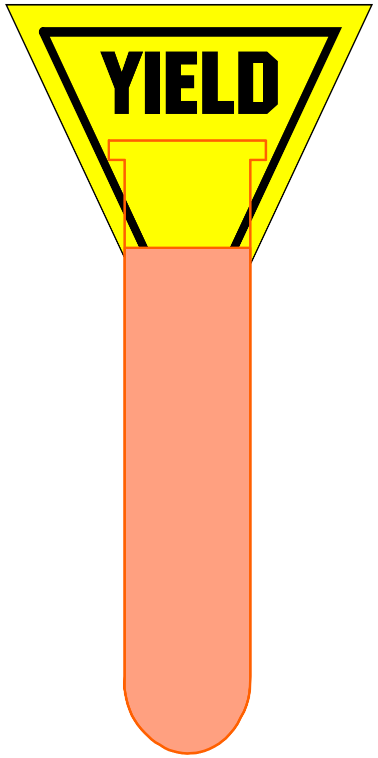
$$DL = 1 - Y^{(1-T)}$$

WHERE

DL = DEFECT LEVEL

Y = YIELD

T = TEST COVERAGE

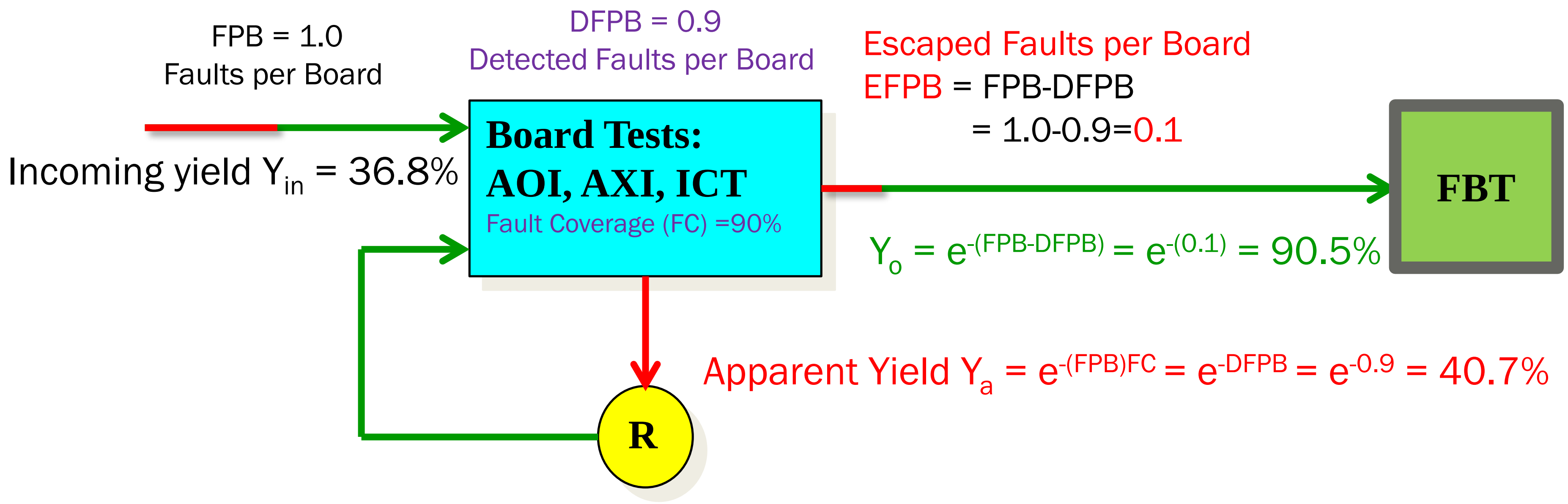


From: Williams, T.W., and Brown, N.C., *"Defect Level as a Function of Fault Coverage,"* IEEE Trans. on Computers, vol. C-30, no.12, Dec 1981, pp. 987-988.

Calculating Outgoing Defect Level from a Test

- Baseline Case – 1 FPB, Y=36.8%. AOI-AXI-ICT coverage T=90%
  - $DL = 1 - .368^{(1-.9)} = 9.5\%$
- Improve production quality by 67% so Y=61%, AOI-AXI-ICT coverage T=90%
  - $DL = 1 - .61^{(1-.9)} = 4.81\%$ - **~ 50% Improvement**
- Instead of production quality improvement, use FBT in addition to AOI-AXI-ICT and improve coverage by 5% so T=95%
  - $DL = 1 - .368^{(1-.95)} = 4.9\%$ - **~ 50% Improvement**
- Cost of FBT << Cost of improving production quality by 2/3, so FBT makes sense

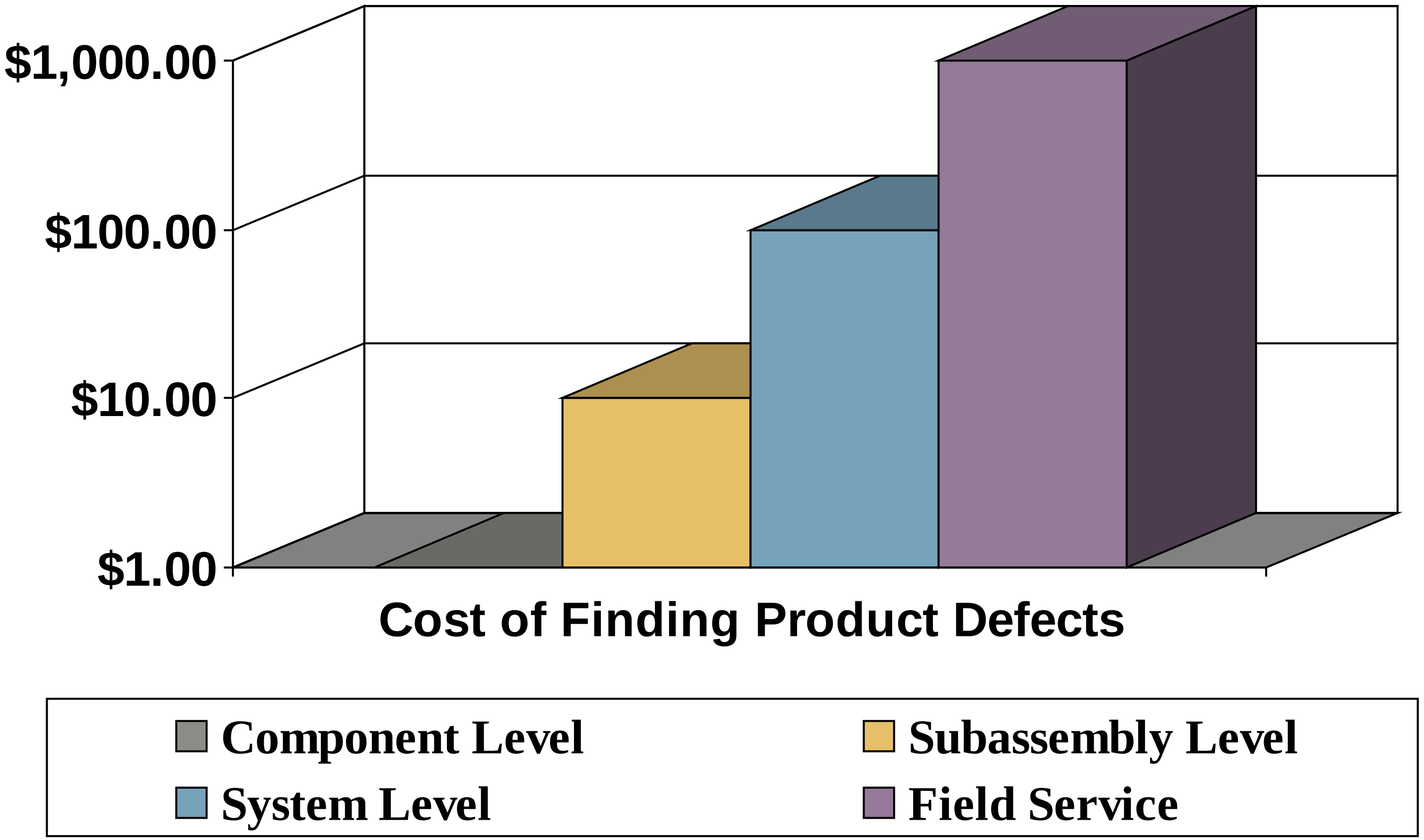
Effect of Board Test on Yields



From: Brandon Davis, Economics of Automatic Testing, McGraw-Hill, 1994

Times Ten Rule

- FBT at Y_o = 90.5%
  - *FPB = -ln(90.5%)=0.1*
- Skipping FBT will cost
  - *$100-$10 = $90/fault*
- In 1,000 boards/mo
  - *There are 100 faulty*
    - Poisson Distribution
- Cost of skipping FBT
  - *100*$90 = $9,000*
- Savings with 95% FBT coverage
  - *0.95*$9000 = $8,555/mo = $121,000/ year*



A Case Study for Functional Board Test (FBT)

- The board functional test (BFT – we call FBT) failed 2,418 boards per year with 10% classified as dead boards – no repair
- 50% of the bone pile was recovered due to more testable circuits, resulting in the recovery of $90,750 in costs
  - *242 X 50% X$750 = $90,750*
- Debug time was reduced by 50%
  - *242 X 5 X $50 X 50% = $30,250*
- Total savings = $121,000
  - *$90,750 + $30,250 = $121,000*

Elements of Test	Number, Cost or Yield Data
Server Boards	20,000 per year
Board Cost	$750
ICT Yield	93% or 1,400 failures per year
Board functional test (BFT) Yield	87% or 2,418 failures per year
Boards unrecoverable from BFT failure (dead boards added to the bone pile)	242 (10% of BFT failures)
ICT Fixture Cost	$30,000 per design
ICT Test Development Cost	$30,000 per design
BFT Station Requirements	Four stations at $29,000 per station
Debug Cost and Time	$50 per hour and 5 hours average debug time

[2]

Microprocessor Failure Modes

- A large fraction of microprocessor failures appears as performance degradation
  - *Most are degraded operation*

IC: Integrated Circuit—Digital—Microprocessor				
Primary failure mode	**Secondary failure mode/ failure mechanism**	**No. of failures**	**Total no. of failures**	**Failure probability (%)**
Parametric failure	Degraded operation	128	132	61.97
	Electrical leakage	3		
	Intermittent operation/unstable	1		
Open	Open circuit pin 2	3	41	19.25
	Unknown	38		
Mechanical failure	Die attachment failure/particle impact noise detection failure; loose die attach	4	22	10.33
	Mechanical anomaly	14		
	Broken pin/mechanical overstress	3		
	Cracked die	1		
Functional failure	Data word failure	4	11	5.16
	Electrical failure/signal timing error	4		
	Intermittent operation	2		
	Data bit failure	1		
Short	Multiple bridging between metallization Paths	1	7	3.29
	Unknown	6		

Sacit M. Cetiner, Kofi Korsah, Michael D. Muhlheim, "Survey on Failure Modes and Failure Mechanisms in Digital Components and Systems," *Nuclear Society International Topical Meeting on Nuclear Plant Instrumentation, Control, and Human-Machine Interface Technologies* 2009

Memory Failure Modes

- Most memory failures are functional failures
  - *Excessive water appears to be the most prominent failure mechanism*

Sacit M. Cetiner, Kofi Korsah, Michael D. Muhlheim, "Survey on Failure Modes and Failure Mechanisms in Digital Components and Systems," *Nuclear Society International Topical Meeting on Nuclear Plant Instrumentation, Control, and Human-Machine Interface Technologies* 2009

IC: Integration Circuit—Digital—Memory—RAM: Random Access Memory—SRAM

Primary failure mode	Secondary failure mode/ failure mechanism	No. of failures	Total no. of failures	Failure probability (%)
Functional failure	Excessive water vapor/chlorine	64	134	84.28
	Data word incorrect	24		
	Data bit failure	21		
	Signal timing error	14		
	Intermittent operation	9		
	No output	2		
Parametric failure	Degraded operation/improper output	3	8	5.03
	Degraded operation/output bits would toggle from 0s to 1s	1		
	Degraded operation/address reads incorrect data; least-significant bit (LSB) appears locked	1		
	TTL floating	2		
	Output high	1		
Open	Unknown	6	7	4.40
	No response	1		
Stuck high	TTL stuck high	2	5	3.15
	Output stuck high/corrosion; open internal lead	1		
	Output stuck high/corrosion; two pins stuck high	1		
	Output stuck high/two LSB addresses locked high	1		
Short	Unknown	3	3	1.89
Stuck low	TTL stuck low	2	2	1.26

Multiplexer Failure Modes

- Most multiplexer failures are parametric failures
  - *Degraded or improper operation*
  - *Low frequency output*

IC: Integrated Circuit—Digital—Multiplexer				
Primary failure mode	**Secondary failure mode/ failure mechanism**	**No. of failures**	**Total no. of failures**	**Failure probability (%)**
Parametric failure	Degraded operation/improper output	47	101	90.99
	Degraded operation	4		
	High insertion loss	27		
	Output low/low radiofrequency output	13		
	Isolation failure/low isolation	4		
	Electrical leakage	2		
	Output high	1		
	Unknown	3		
Functional failure	Electrical failure/signal timing error	2	4	3.60
	Data bit failure	1		
	Electronic destroyed in analysis	1		
Stuck high	TTL stuck high	2	2	1.80
Stuck low	TTL stuck low	2	2	1.80
Mechanical failure	Die cracked/fractured	1	1	0.90
Open	No response	1	1	0.90

Sacit M. Cetiner, Kofi Korsah, Michael D. Muhlheim, "Survey on Failure Modes and Failure Mechanisms in Digital Components and Systems," *Nuclear Society International Topical Meeting on Nuclear Plant Instrumentation, Control, and Human-Machine Interface Technologies* 2009

Components	Failure Modes	Detectable by AOI, AXI, ICT	Detectable by FBT	DFT Considerations
General	Stuck-At Faults	Shorts, Opens but not all stuck-ats	Depends if accessible	Improve controllability and observability by utilizing boundary scan cells as controllability, observability and diagnosability test points
	Bridging Faults	ICT and even connectivity tests can readily find faults with adjacent pins shorted	Not easily	Make such faults accessible to ICT and/or boundary scan
	Delay and State Transition Faults	Not unless the delay is within a faulty IC - not likely if IC was well tested	Yes, to the degree that the FBT speeds can detect the delay	DFT may need to supply some pulse catching mechanism and/or BIST circuitry to test in situ
Capacitors	Shorted	ICT can detect especially for electrolytics.	Only its effect on other circuits	
	Wrong capacitance	Probably not	Only its effect on other circuits	Prepare for critical failures by using some delay testing mechanisms.
	Parasitic resistance	Probably not	Only its effect on other circuits	
Resistors	Open	With ICT.	Only its effect on other circuits	
	Shorted	With ICT.	Only its effect on other circuits	
	Wrong value	With ICT.	Only its effect on other circuits	This may not be easily accomplished with FBT unless specific DFT procedures are used.
Inductor and Transformer windings	Open	With ICT.	Yes.	
	Shorted to core	Not easily - high temperature or smoke test	Not easily - high temperature or smoke test	Safeguards preventing damage or injury should be part of DFT
Diodes	Open (for rectifying diodes)	With ICT.	With analog tests	
	Shorted (for zener diodes)	With ICT.	With analog tests	
	Voltage/Current surge due to transients	Maybe with ICT	Probably	Analog DFT

Components	Failure Modes	Detectable by AOI, AXI, ICT	Detectable by FBT	DFT Considerations
Oscillators	Wrong Frequency	Maybe with ICT	Probably yes, with the right instrument	
	Rise time and Fall time	Probably not	Probably yes, with the right instrument	Delay measuring DFT techniques
	Phase noise and Jitter	No.	With Bit Error Rate tester	DFT can help make this testable
	Current and Power Stability	Probably not	Probably yes, with the right instrument	Make such faults accessible
	Temperature Stability	No.	Probably yes, with the right instrument	
Programmable Logic - PLAs and FPGAs	Stuck Faults	Only at I/O	Testing the function of the device to verify proper synthesis and operation	Use internal scan and BIST to ensure proper internal operation. Use boundary scan which is usually available and enhances FBT. Often unused FPGA pins serve as extra board test points as they have boundary scan.
	Crosspoint Faults	No.	Same as for Stuck Faults	Same as for Stuck Faults
	Extra/Missing Transistors	No.	Same as for Stuck Faults	Same as for Stuck Faults
	Bridging Faults	ICT and AXI if IC is ball grid array.	Internally to IC - maybe due to misprogramming	Same as for Stuck Faults
High Speed I/O	Single wire opens or resistive	With ICT.	Yes.	
	Shorts between signal pairs	With ICT.	Yes.	
	Leakage	No.	Yes with proper test instrument	
	Clock failure	Maybe with ICT.	Yes with proper test instrument for the clock speed	May use DFT and BIST circuitry for high speed test
	Tx drive weaken	Maybe with ICT.	Yes with proper test instrument for the clock speed	May use DFT and BIST to pair Tx and Rx to mutually test each other
	Rx sensitivity weaken	Maybe with ICT.	Yes with proper test instrument for the clock speed	May use DFT and BIST to pair Tx and Rx to mutually test each other

Components	Failure Modes	Detectable by AOI, AXI, ICT	Detectable by FBT	DFT Considerations
A/D and D/A Converters	Power levels	Maybe with ICT.	Yes with proper instruments	
	All bits stuck for D/A	Maybe with ICT.	Yes.	
	Only certain bits stuck for D/A	Maybe with ICT.	Yes.	Some DFT techniques can help
	Over maximum voltag for A/D	Maybe with ICT.	Yes.	
	Bit-wise conversion of A/D	Maybe with ICT.	Yes with proper instruments	Some DFT techniques can help
RAMs	Output Levels	With ICT.	Yes.	
	Parametric Faults	Probably not.	Maybe.	Use Memory BIST
	Power Consumption	With ICT.	Yes.	
	Noise Margin	No.	Maybe, depending on available instrumentation	DFT should be used to find noise margins for critical applications
	Data Retention Time	No.	Maybe, depending on available instrumentation	Use Memory BIST
	Stuck Faults in Address Register	Maybe with ICT.	Yes.	
	Stuck Faults in Address Decoder	Maybe with ICT.	Yes.	
	Stuck Faults in Data Register	Maybe with ICT.	Yes.	
	Cell Stuck Faults	Maybe with ICT.	Probably, but testing for all such faults would not be feasible	Use Memory BIST
	Adjacent Cell Coupling Faults	No.	Pattern sensitivity between a pair of cells is possible but is a long test.	Use Memory BIST
	Pattern-Sensitive Fault	No.	The presence of a faulty signal depends on the signal values of the nearby points – Most common in DRAMs. Need to test with refresh cycle.	Use Memory BIST

Managing DFT for FBT

- DFT Reduces Test Equipment Cost
  - *Reduces complexity of test instruments needed*
  - *Utilizes BIST to replace many – maybe all – ATE functions*
- DFT Reduces Cost of Test Program Development
  - *Easier to develop tests*
  - *Better Controllability, Observability and Diagnosability*
- DFT Reduces Test Escapes
  - *Less undetectable faults*
  - *Less hard to detect faults*
  - *Less hard to diagnose faults*

Managing the DFT Organization

- Design and Test Engineering Teams for Block Diagram Design
  - *Develop Test Strategy*
  - *Select Test Equipment*
  - *Consider DFT Tradeoff for each*
- Design and Test Engineering Team for Design Verification Test
  - *Designers work with Test Engineers for a better DVT*
    - Test Engineers learn design as it is being developed
  - *Test Engineers develop environmental stress screening early*
    - While designs can be changed
- Design and Test Engineering Teams for Test Program Development During Design
  - *Test Engineer Develops Test Routines*
    - Consults with designers on how DFT improvements can reduce test development

Summary and Conclusions

- FBT is complex and for that reason has been skipped by manufacturers
- Failure modes suggest that without FBT many products are inadequately tested
- FBT is economically necessary and should not be skipped
  - *Defect Levels for released products are too high*
  - *Use DFT to combat complexity and cost*
- Implement DFT by reorganizing for Design and Test Teams
  - *This has already been done for years by IC manufacturers*
    - It is time for board manufacturers to appreciate the value of test and DFT

References

1. Agilent Technologies

2. From Case Study at Sandy Bridge as reported by Larry Osborne, How to Debug Dead Boards in Production – Based on a Case Study, ASSET InterTech, Inc., 2013

Thank you!

Questions & Answers