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Challenges of Manufacturing with Printed Circuit Board Cavities

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ABSTRACT

Cavity technology in a Printed Circuit Board (PCB) has existed for many years. The methodology to create the cavity in the PCB has evolved over time as technologies have advanced and the manufacturing process varies by the individual PCB fabricator as well as the reasons for using the cavity technology. For the purpose of this paper, a cavity will be defined as a hole in the PCB going from the outer copper layer to an inner copper layer, but not completely through the PCB. The cavity design and assembly issues identified during the design of experiments (DOEs), the findings, reliability results, and conclusions will be discussed in this paper.

Introduction
Cavity technology can be an effective solution in reducing the total assembled PCB thickness (Z-height) on designs utilizing taller, stacked devices, i.e. package on package (PoP), or where additional space is may be required for increasing the bend radius on flexible connections and the Z-height within the product enclosure is restricted.

Several parameters were identified that could impact the ability to assemble components on and below the surface of the PCB, and to investigate these parameters; the following designs of experiment (DOEs) were conducted. Two test boards were designed to test the DOEs shown in Table 1.

Table 1. DOE List.

DOE Legs	Condition Tested
1	Squeegee Flap Length
2	Cavity Depth to Air Gap
3	Multi-level Solder Pasting and SMT
4	SMT Component Placement & Reflow

Test Boards
Two test boards (TB) were designed to evaluate multi-level paste printing and assembly parameters of cavity technology. The cavity test boards utilized the same daisy chained (DC) 12x12mm 0.4mm pitch BGA PoP package with 796 solder balls. Cavities were placed in 4 locations and at 2 different depths on both test boards (see Table 2).

Table 2. Test Boards

Test Board	Cavity	Cavity Layer	Cavity Depths (um)	Cavity Air Gap (mm)	Squeegee Thickness (um)	Flap Length (mm)	Stencil Thickness (um)	Stencil Type
TB 1	1	2	82	2	300	5 8.9 12.7	100	Pocket
	2	5	300	2				
	3	5	300	3.6				
	4							
TB 2	U2	2	80	1.1	200	16	100	Pocket
	U14							
	U4	4	230	1.1				
	U12							

TB1 board was designed to simulate a customer validation board during multi-level paste printing and the assembly of multiple components with various component to component spacing while TB2 design was based upon the JEDEC standard JESD22-B111 modified to accommodate cavities.
TB1 was a 0.7mm thick, 203mm X 127mm, 10 layer Any Layer uVia high density interconnect (HDI) PCB with an Electroless Nickel Immersion Gold (ENIG) surface finish.

TB2 was JEDEC type, 1mm thick, 140mm x 132mm (with assembly rails), 4-2-4 high density interconnect (HDI) PCB with an Organic Surface Preservative (OSP) surface finish

Both test boards, fabricated by the same supplier, were constructed with Low Halogen FR4 material, with a UL 94V-0 rating, and a 150°C glass transition temperature (Tg). TB2 utilized resin coated copper foil (RCC) for the outer layer prepreg with solder mask placed in the cavities while TB1 was built with FR4 and the cavities were free of solder mask. TB1 included passive component pads in the cavities and on the surface layer where TB2 did not.

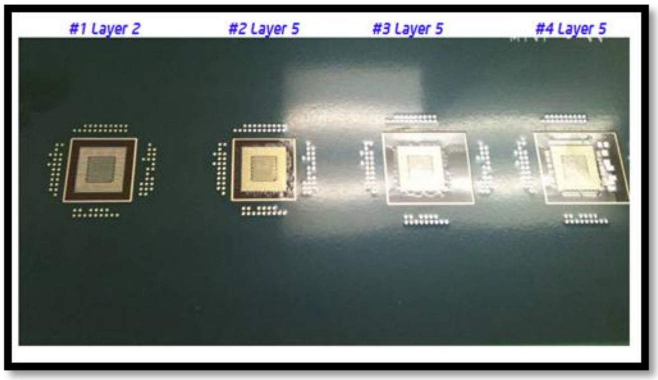


Figure 1. TB1 with cavity and layer

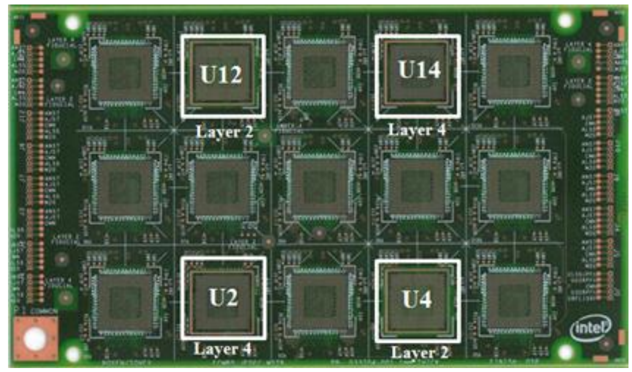


Figure 2. TB 2 with cavity locations and layer

The TB1 cavity location #1 (Figure 1) was recessed to layer 2 (82um deep), while other 3 cavity locations were recessed to layer 5 (300um deep). TB2 cavities U2 and U14 were terminated on layer 2 (170um deep) while the U4 and U12 cavities terminated on layer 4 (339um deep).

The 4 cavity locations on TB2 (Figure 2) were selected based upon historic reliability data which showed these locations were prone to fail first during drop testing. The 2 depths on TB2 represented the minimum depth (layer 2) and the maximum depth (layer 4) that could be attained on the 4-2-4 stack up. The other 11 BGA patterns remained on the surface layer. Packages were assembled during the same process on all 15 BGA patterns including the cavities (Figure 3).

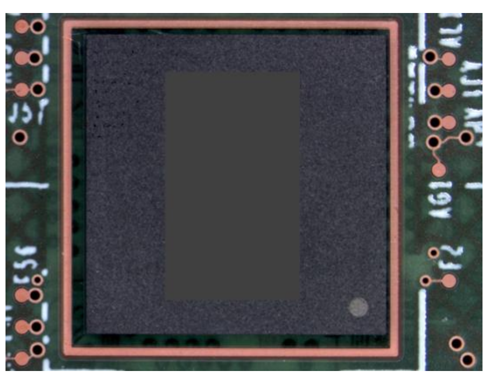


Figure 3. BGA package assembled in 1 of the TB2 cavities

The number #1 and #2 cavities, although recessed to different depths, maintained the same component to cavity wall air gap spacing of 2.0mm, while cavities #3 and #4 have a larger air gap of 3.6mm with the same cavity depth. Cavity #4 in addition to the BGA pattern had passive solder pads around the BGA perimeter.

Solder Paste Stencils

Both stencils were 4mils thick, full board 3 dimensional metal stencils with recessed pockets matching the cavity depth and locations on each test board. The stencils were manufactured by 2 separate stencil manufacturers from the test board Gerber files.

Squeegees

The squeegees were supplied by each of the stencil manufacturers and were manufactured with flaps created by slitting the blade to match the locations of the cavities on the test boards. Typically a squeegee blade is a single blade running the length of the squeegee.

The flaps were designed to follow the contour of the test board, dropping down into the cavities at the leading edge and retracting from the cavity at the trailing edge to provide pressure inside the stencil pockets while printing solder paste on the pads.

Three squeegees used to print TB1 were 300um thick and each of the 3 squeegees had a different flap length; 5mm, 8.9mm, and 12.7mm. TB2 was printed with 1 squeegee at 200um thick and a flap length of 16mm. (Table 2)

Printing

Single pass, multi-level paste printing proved to be the biggest challenge in the SMT assembly process for both test boards. Halogen-free SAC-305 solder paste. TB1 used a Type3/4 paste and TB2 used a Type 4 paste. Both test boards were printed with a commercially available printer.

Findings

Factors identified as critical to maintaining a consistent solder paste height across the printed BGA pattern were: 1.) the alignment of the squeegee flaps to the stencil pockets, 2.) the squeegee flap length, 3.) the width of the air gap between the nearest solder pad and the cavity wall, and 4.) proper board support under the cavity.

Alignment

Proper alignment (Figure 4) of the individual squeegee flaps to the stencil pockets to attain the proper solder paste volume over the entire board without defects proved to be very difficult. The alignment was accomplished by performing a test print; measuring the offset (Figure 5) of the paste to the stencil pocket with a micrometer then adjusting the squeegee blade position in the squeegee assembly (see Figure11). The procedure was repeated until the optimal squeegee blade alignment was achieved.

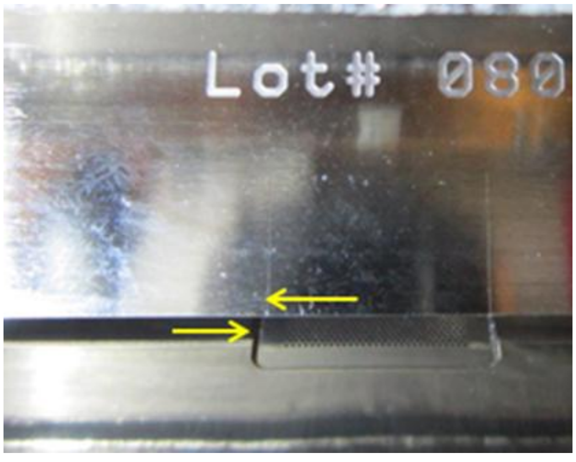


Figure 4. Squeegee flap misalignment to stencil pocket

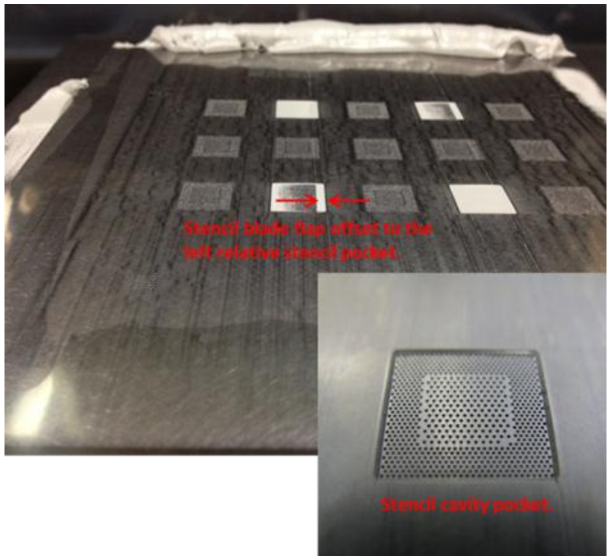


Figure 5. Cavity stencil showing squeegee blade offset

Adding orientation marks to the squeegee and a corresponding guide marks on the stencil would have facilitated the alignment and significantly reduced the alignment time (see Figure 6).

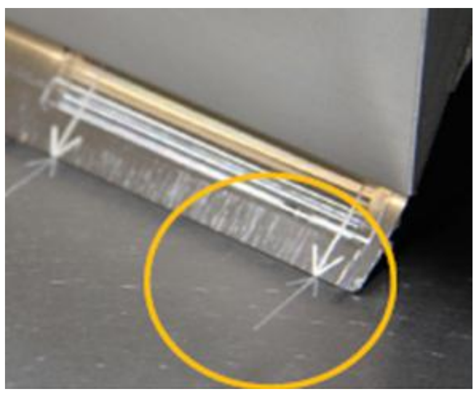


Figure 6. Squeegee and stencil with alignment marks

Flap Length

Determining the proper flap length that provides the correct amount of pressure on the paste is another factor critical to attaining correct amount of paste on the pads in the cavity and on the surface of the PCB with a single pass of the squeegee. Paste tests were performed on TB1 with the 3 different flap lengths. The 5mm flap proved to be too short to attain adequate pressure on the stencil in the cavity resulting in inconsistent paste volumes. The 12.7mm was too long and did not properly transition in and out of the cavity to produce a uniform paste height. The 8.9mm flap length (Figure 7) produced a uniform paste print on 3 of the 4 test cavities. Cavity #2 on TB1 had some additional challenges which will be discussed later.

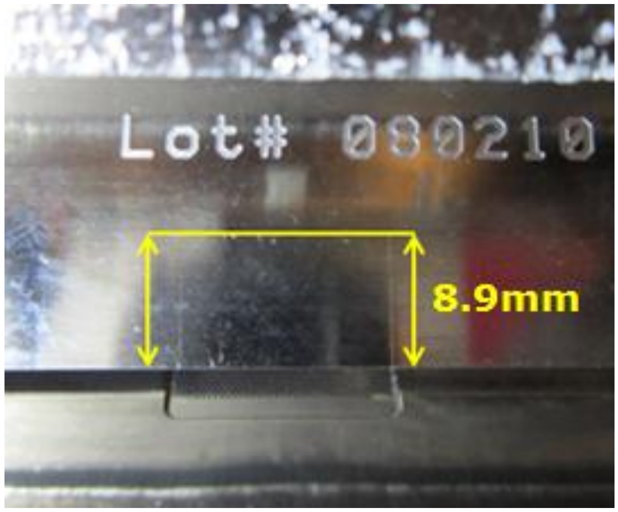
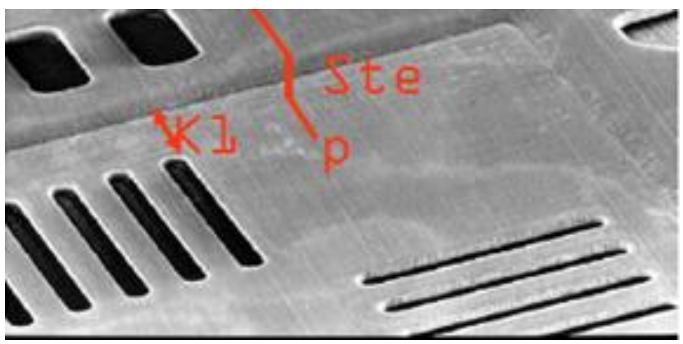


Figure 7. TB1 optimal Flap length.

Air Gap

The IPC 7525A "Stencil Design Guidelines" states that there is a relationship between the cavity or "step" depth relative to the width of the air gap measured from the wall of the cavity to the nearest feature to be printed. To summarize the guideline: the minimum air gap (cavity wall to the nearest printed feature) increases at a fixed rate of 900um for every 25um of step depth. Therefore the calculated gap "K1" (shown in Figure 8) for a 250um deep cavity would be 900um.



$$K1(Gap) = \frac{StepDist(um)}{25um}(900um)$$

Figure 8. K1 Air gap per IPC 7525 Guideline.

TB1 cavities 2, 3, and 4 were at a 300um depth. Cavity #2, although at the same depth as cavity 3 and 4, had the same 2mm wall to solder pad air gap as cavity #1 but the depth of cavity #1 was 82um depth.

Paste printing cavity #2 with an air gap of 2.0mm and depth of 82um resulted in wet bridging on several of the leading and trailing rows (Figure 9) of the BGA pads with all 3 squeegees. However, using the same print envelope, we were able to successfully produce level and defect free prints with an air gap width of 3.6mm on the 300um deep cavity with the 8.9mm flap on the squeegee blade.

Although TB2 was not designed to test the air gap, the TB2 cavities were successfully printed at 80um and 230um depth with an air gap of 1.1mm using a squeegee with a flap length of 16mm. Both conditions, the air gap and the flap length, contradicted the results of TB1 which showed the 8.9mm flap with a 3.6mm air gap as the parameters needed for consistent paste volume. Another critical parameter, squeegee thickness, not previously identified may have influenced the results of TB2. The squeegee flap was longer but the squeegee was also 100um thinner than those used on TB1. The thinner squeegee may have been more flexible allowing the flap to reach the bottom of the cavity closer to the wall of the cavity.

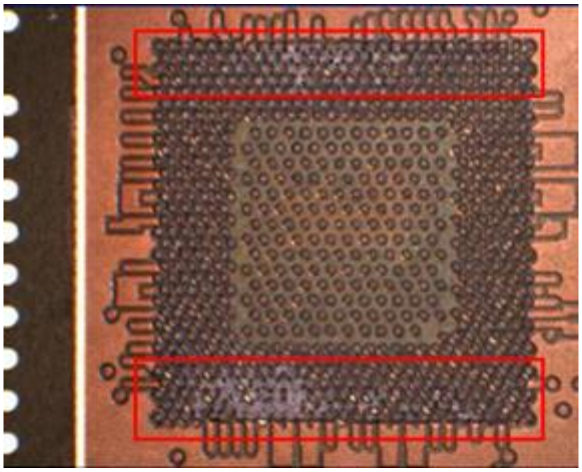


Figure 9. Wet Bridges on Cavity #2.

Cavity Support

As reported earlier in the paper, achieving a consistent paste volume print on TB1 cavity#2 was problematic. A review of the print process and fixture showed there was a difference between cavity 2 and the other 3 cavities. Cavity #2 was not supported as well by the print fixture as the other 3 cavities during the printing process, allowing the board to bend, resulting in an overprint on the first 2 rows of the leading and trailing edges. Modifying the support fixture resulted in improved support for cavity #2 and less wet bridging, but the modification did not eliminate the bridging (Figure 10).

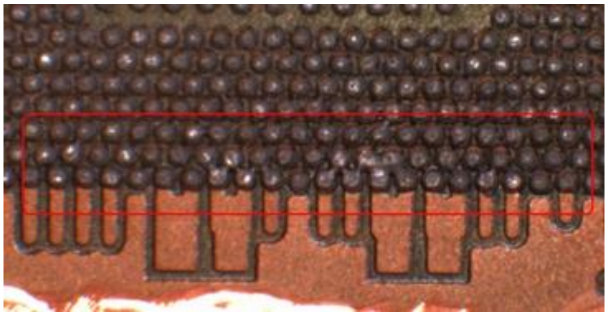
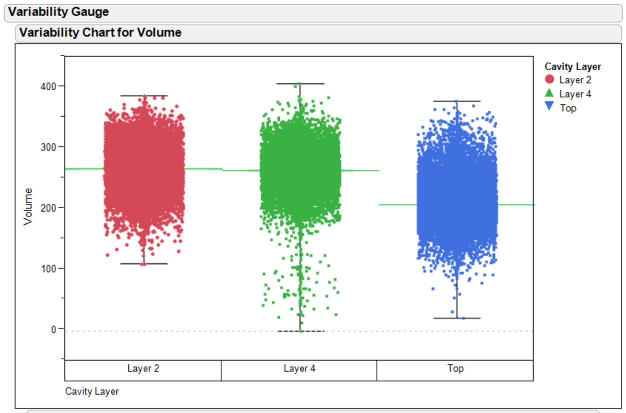


Figure 10. Wet Bridges on Cavity #2 after support adjustment.

The wet bridging persisted through several print attempts and became apparent that the squeegee flap was not transferring the pressure uniformly across the #2 cavity pattern. Cavity #2 with the 2mm gap and 300um depth would not yield a consistent defect free print. The wet bridging issue was solved by applying flux on the cavity #2 pads with a small brush, instead of printing solder paste.

Solder Paste Volume

After paste printing TB2, the solder paste volume was measured with a solder volume optical-laser metrology tool. Measurements were made at all 15 BGA locations on all BGA pads. The metrology tool was set up to detect the following solder paste defects: 1.) excessive volume, 2.) insufficient volume, 3.) paste bridging, and 4.) paste offset. The target solder paste volume was 250 cubic mils per pad in the BGA pattern. As Figure 12 illustrates, optimizing for the target paste volume at the cavity locations, the paste volume on non-cavity (top) locations fell below the target volume. Although the process provided adequate solder paste volume for this experiment, additional process optimization could reduce the variation of solder paste volume in the cavity locations.



Variability Summary for Volume

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Minimum	Maximum	Observations
Volume	223.1409	38.43536	0.111232	222.9229	223.3589	0	406	119400
Cavity Layer[Layer 2]	266.6293	36.74216	0.291201	266.0585	267.2001	110	387	15920
Cavity Layer[Layer 4]	263.8417	37.42924	0.296647	263.2602	264.4232	0	406	15920
Cavity Layer[Top]	207.8337	25.19836	0.085157	207.6668	208.0007	21	378	87560

Figure 12. Solder paste volume by board cavity location.

SMT Yield

A pick-and-place machine was used to place the components on the test boards. There were no defects or miss-pick errors associated with the process. TB 1 used a standard SAC-305 reflow process to solder the components to the board in a 10-zone reflow oven with a nitrogen atmosphere and TB2 used the same reflow process but with a 14 zone reflow oven with air.

Although TB1 and TB2 were assembled by 2 different companies, both test board designs yielded 100% on 400 and 150 packages respectively after SMT. A total of 440 packages were assembled in the cavities. One package on TB2 had an electrical failure which was determined not to be related to the cavity board or SMT process.

SMT yield was determined by: 1.) Electrical continuity testing of the package daisy chain, and 2.) Defect inspection with X-ray for solder bridging, missing solder, small balls, and solder voids.

TB2 had 5 packages in the 4-layer cavity locations that were identified during post SMT x-ray as having smaller solder balls in the corner or along the edge of the package. Although these solder joints were low in solder volume, they still passed post SMT electrical testing. Figure 13 shows an example of the small solder balls.

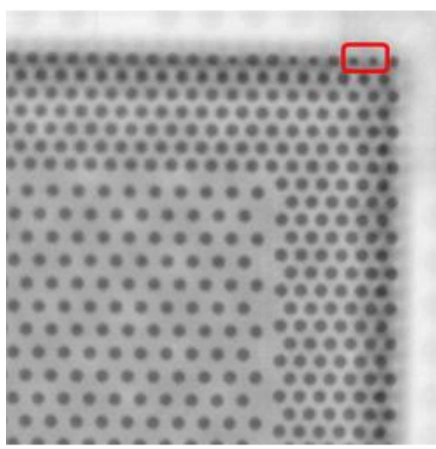


Figure 13. Small solder balls

Drop Test

The solder joint reliability was evaluated using a standard JEDEC drop test; 1500G, 0.5s half-sine pulse. The BGA cavity locations were chosen to coincide with the high risk locations for solder joint drop test failures. The 2-layer deep cavities were BGA locations U2 and U14 and the 4-layer deep cavities were BGA locations U4 and U12 which were the high risk locations. Selecting the high risk locations enabled the test results to be compared with historical data trends on test boards without cavities.

The cavity reliability drop test results for the critical to function (CTF) and the non-critical to function (NCTF) solder joints (see Figures 14 and 15) were statistically equivalent to the historical data of the non-cavity BGA packages at the same locations.

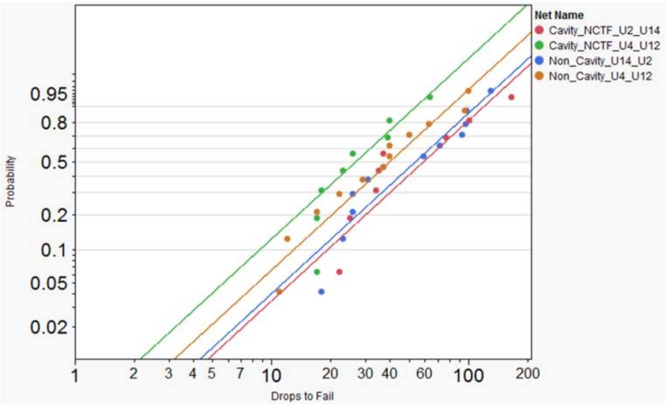


Figure 14. Cavity and Non-cavity solder joint joint reliability, NCTF locations

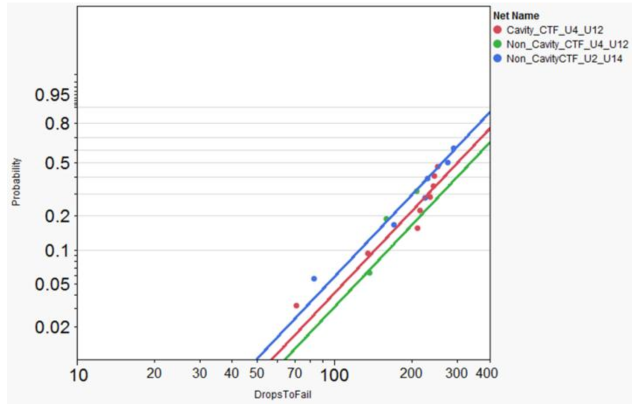


Figure 15. Cavity and Non-cavity CTF solder reliability

Note: No CTF failures observed at the U2 and U14 cavity locations.

TB1 2-layer cavity NCTF solder joints demonstrated better reliability than the 4-layer cavity NCTF solder joints (t-value <0.05) as shown in Figure 16.

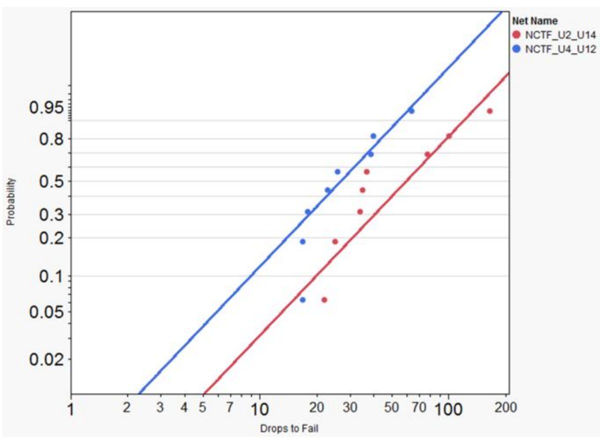


Figure 16. NCTF failures for 2 and 4 layer deep cavities

CONCLUSIONS

The use of cavities in a PCB as a method to reduce the component height or to increase component clearances is a viable technology. SMT testing of the cavity boards assembled with the 0.4mm pitch BGA packages at multiple cavity depths has demonstrated that PCBs can be successfully paste printed, assembled, and reflowed in the same multi-level processes with the existing equipment capability.

Single pass, multi-level solder paste printing is the most challenging aspect to implementing cavity technology into a high volume manufacturing environment. The key to a successful paste print is optimizing the critical print parameters; 1.) Solder pad to cavity wall air gap, 2.) Squeegee flap length and thickness, 3.) Print fixture support, and 4.) Pocket stencil alignment.

Optimizing the print parameters helps insure multi-level paste print quality but the parameters may need to change as the cavity design changes. The testing demonstrated a relationship between the cavity depth, air gap, and flap length and flap thickness that impacts the paste printing results. Test prints would be necessary to reset the critical parameters to accommodate the design differences. Other print parameters not mentioned in the paper that are also critical to achieving consistent solder paste volume with single level paste printing are important and also apply to multi-level printing.

The drop testing showed that the solder joints on the cavity components appear to be as reliable as the same components assembled to the surface of the PCB. The drop test results also showed a statistical reliability improvement for the 2-layer cavity over the 4-layer cavity.

An alternative methodology to paste printing the BGA style packages, is dipping of cavity components in paste or flux prior to placement. The dipping method does not require solder paste stencils to be pocketed. Flux dipping was not investigated during this study.

The conclusions are based upon a limited data set and additional testing is encouraged.

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