Early Design Review of Boundary Scan in Enhancing Testability and Optimization of Test Strategy

Sivakumar Vijayakumar
Keysight Technologies
Singapore

Abstract
With complexities of PCB design scaling and manufacturing processes adopting to environmentally friendly practices raise challenges in ensuring structural quality of PCBs. This makes it essential to have a good 'Design for Test' (DFT) to ensure a robust structural test.

A good structural test implementation starts right at the design of an ASIC wherein, the system application and, the ASIC design itself should be kept in mind for implementing the features to enable testability.

Answers to the below four questions are the essence of the first part of this paper.

- What are the aspects to be considered for enhancing 'DFT'?
- How effectively can the 'DFT' be reviewed?
- Is there an intelligent and automated way of doing this?
- At which phase of Product Life Cycle should the DFT review be done, to obtain best value for structural test?

During the course of the DFT review, can we realize a good test strategy for the PCBA? How can the test strategy of the PCBA be partitioned as to what portions of the design can be covered structurally and what is covered functionally, in a way that provides best diagnostics to discover faults? Answers to the above two questions will be addressed in the second part of this paper.

Introduction
Test strategies have not caught up with the speed of advancements in PCBA technologies and the design complexities that today's technologies demand. For the questions posed above, the answers have been implemented as case studies for different market segment designs. The results have been promising in enhancing the yield, meeting the time-to-market of the product, and in optimizing redundancies in test flow. This paper will present on how this is achieved and would make an attempt in generalization for a good DFT review and test strategy.

Device Level DFT
DFT is a concept that spans from the device level all the way to the system. To ensure a robust test to diagnose maximum defects, DFT becomes a critical piece. At a device level, the complexities are ever increasing. This increases the complexity of testing as well. In order to cater to developing an efficient test, addition of test circuitry and its design becomes paramount. Device being the foundational block for the test scheme of a system, a well thought out DFT architecture always pays off for enabling determinism of quality.

Several years ago, enabling Test Access Ports via IEEE Standard 1149.1 (Boundary Scan Standard) has predominantly been a major test circuit provided by device vendors. This enabled detecting structural defects on boards arising on the digital nodes that interfaced with other devices which are Boundary Scan enabled.

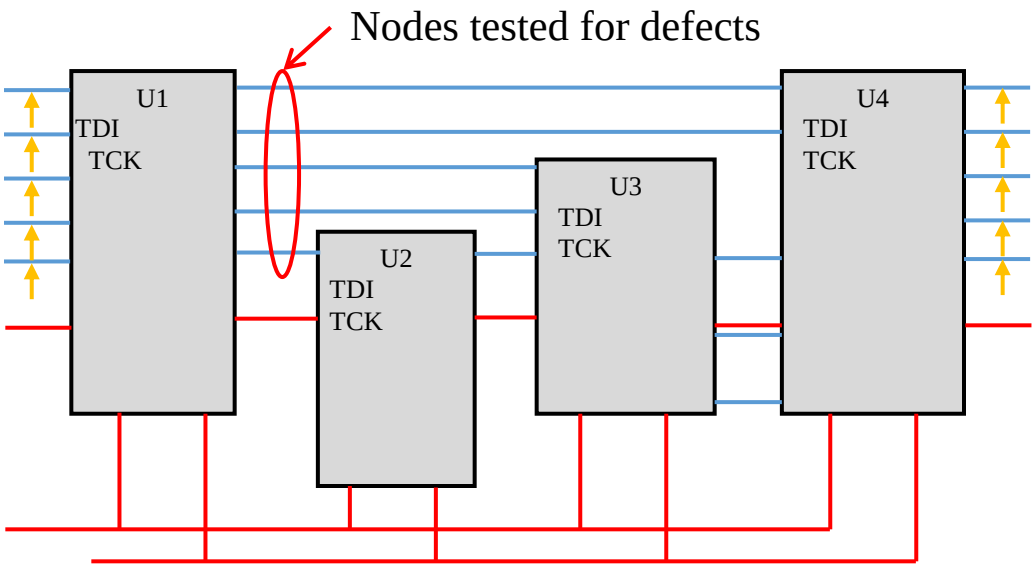


Figure 1 –Defect Detection On Digital Interconnects Between Devices Enabled with IEEE 1149.1

This limits the capability to only the IOs that had Boundary Scan cells on them and, the type of node interconnects on it. From a device perspective, it limits the test offerings for chip level fault detection at board or system level.

The question often posed would be- the devices are tested by the vendors. So, the parts are good. Hence, why is there a need to enable tests for internal modules of a chip? For complex ICs - functionality tests, parametric tests, memory tests, etc, would help classify the part as a good or bad part for the depths of tests written in the device test environment. But, once the part is assembled on a board, the characteristics of the neighboring circuitry around it may have an impact on the device's behavior. And, any stress tests at a system may result in any faults on the internal of a chip? This is where, DFT to detect faults inside a chip's logic becomes important.

With ICs getting more complex, the defects within the logic of the device is also a matter of concern.

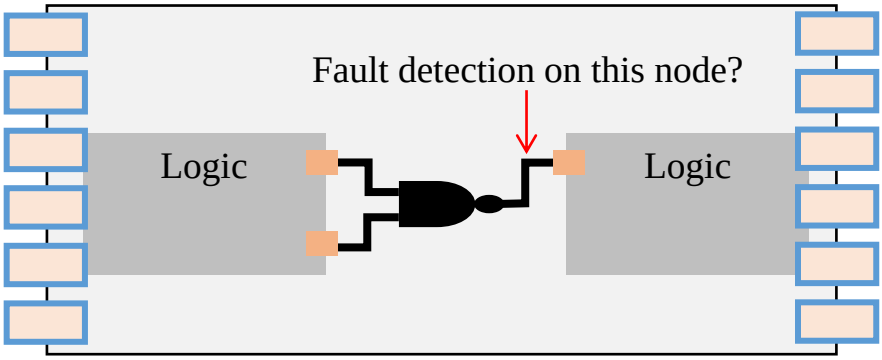


Figure 2 –Fault Detection On a Node Inside a Device

To identify these internal faults, pattern based and scan based test architectures have become predominant. This has enabled test for defects on the device effectively by emulating at-speed behavior of the test logic.

Scan based test logics in the form of BIST (Built-In Self-Test) has been expanded onto the Boundary Scan TAP. During the design of the chip, test modules are built to test the functionality using the Design for Test methodology for devices. This has made testing more effective and pervasive that can readily be used at any stage of the product life cycle.

BIST allows testing of entities of the chip that would be difficult to test. This makes the test generation and test application cost-effective. A good DFT results in increasing the test coverage and thus, enabling in identifying more defects.

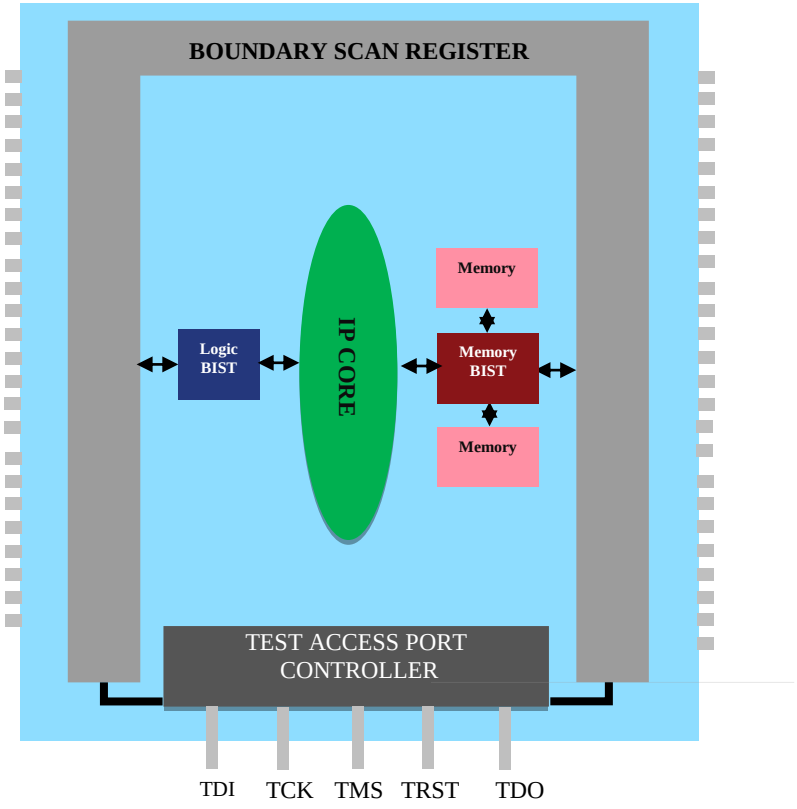


Figure 3 – Boundary Scan Device with Built-In Self-Test (BIST)

With the increase of SOC (System-On-Chip) and SIP (System-In-Package) designs with a mix of digital, radio frequency and mixed-signal today, the need for DFT has advanced to enable the devices to provide an architecture for a flexible test methodology that is cost effective and can be leveraged in multiple phases of the life cycle, ranging from Chip test to a system.

With the multiple IPs in a package, flexibility to test at different phases is crucial to validate the effects of other interfacing devices or systems. In addition, IPs can be re-used easily into different SOCs. The DFT for the IP core will enable BIST logic to integrate to the SOC module for tests. This will ensure faster time for SOC integrations by treating the IPs as black-box. Enabling DFT at a device will help in ensuring that the fundamental and critical block of the system – i.e. the Chip is defect free. New standards such as IEEE 1687 and ratification to IEEE 1149.1 standard approved in the year 2013 cater to increasing the test logic with the chips.

Board and System Level DFT

When it comes to the DFT at a board level, the first step is to choose a IEEE 1149.X enabled device for the required functionality, if available. This is the key to increase structural test coverage. The onus lies on the Design teams in qualifying JTAG enabled parts to supplement into their functional requirements and specifications. Streamlining component qualification and verifying new devices are compliant to IEEE 1149.1 Standard by the Product Procurement team facilitates an effective process for good DFT.

DFT guidelines is not the scope of this paper. However, a few good practices of DFT for a board will be highlighted to facilitate with the scope of this paper.

Chain the devices with similar logic voltage together by interfacing with the others appropriately with voltage translators.

In complex designs where certain programmable devices or custom ASICs are built purely for power management, it is preferred to not chain this device as it could affect the stability of the board during the test.

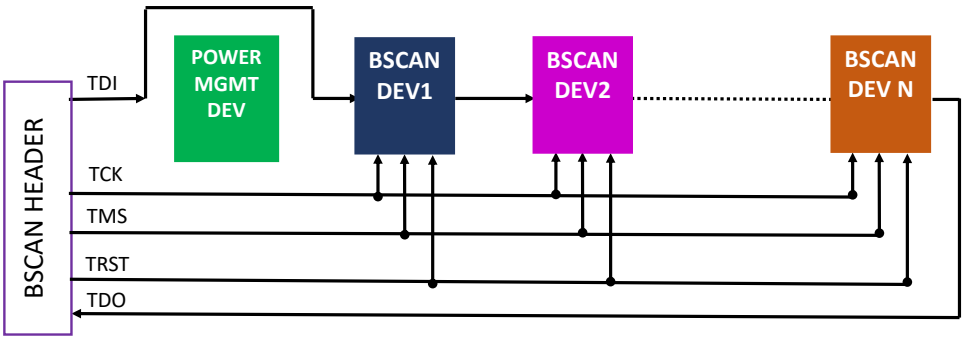


Figure 4 – Boundary Scan Topology Bypassing Sensitive Circuitry

Group the programmable devices together is one section and keep them at the beginning of the chain. This would facilitate using a common header for boundary scan and for device programming.

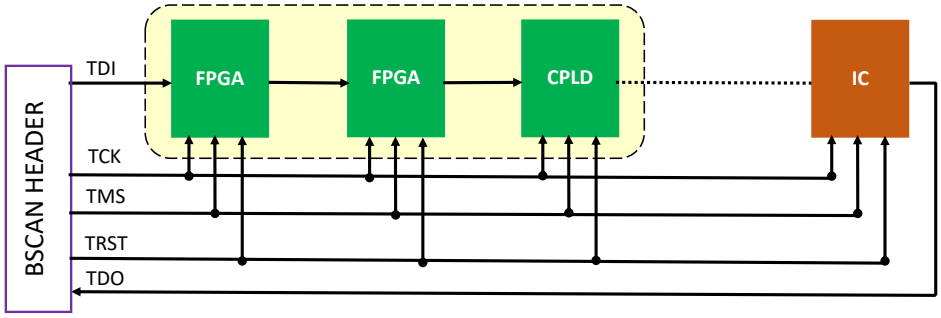


Figure 5 – Boundary Scan Topology with Programmable Devices

The FPGA on the chain can become the Boundary Scan master controller and run the test on the rest of the chain. This enables:

- the board to go into Boundary Scan mode when desired to test for Boundary Scan
- to run any BIST tests on ASICs that are part of the Boundary Scan chain to check for any faults when the characteristics are not as desired

On complex designs, when the board has 20 or more devices involving several logic levels, using a CPLD as a scan path linker, would reduce the real estate usage for boundary scan implementation and provides better management on boundary scan chain. When the designs involve several logical circuits in a chain - e.g. CPU block, Data Processing block, IO management, Memories, etc. a scan path for each circuit would help control all the TAP signals independently. If for example, the CPU block is desired to be kept out of testing for a debug, the appropriate port on the linker can be disabled thereby, ensuring that none of the TAP signals on that logic are toggled. This provides greater flexibility of test via software.

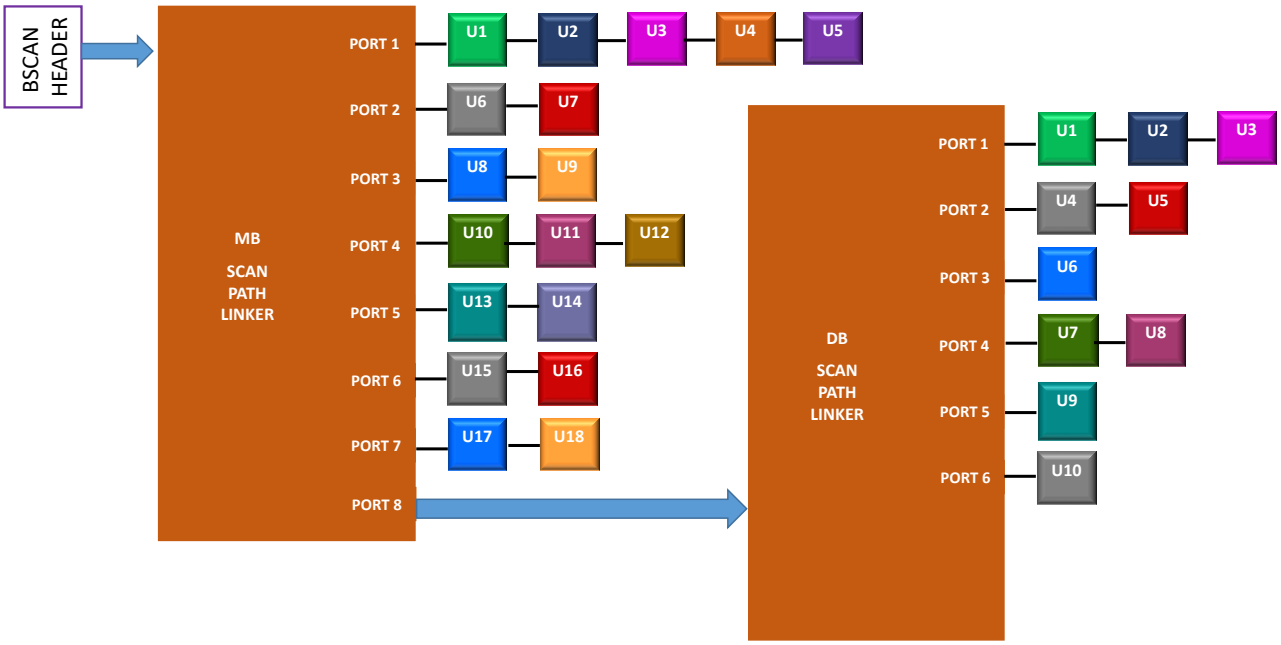


Figure 6 – Boundary Scan Topology with Scan Path Linkers

For system-level Boundary Scan implementation involving multiple board configurations, making the boundary scan chain to be dynamically configurable by the presence of the board in the system is of great value. This enable the chain to be tested as a system once all the boards are stacked. It is useful to ensure that when assembling the boards, if it results into any Board-to-Board connector issues, structural test via Boundary Scan would come in handy.

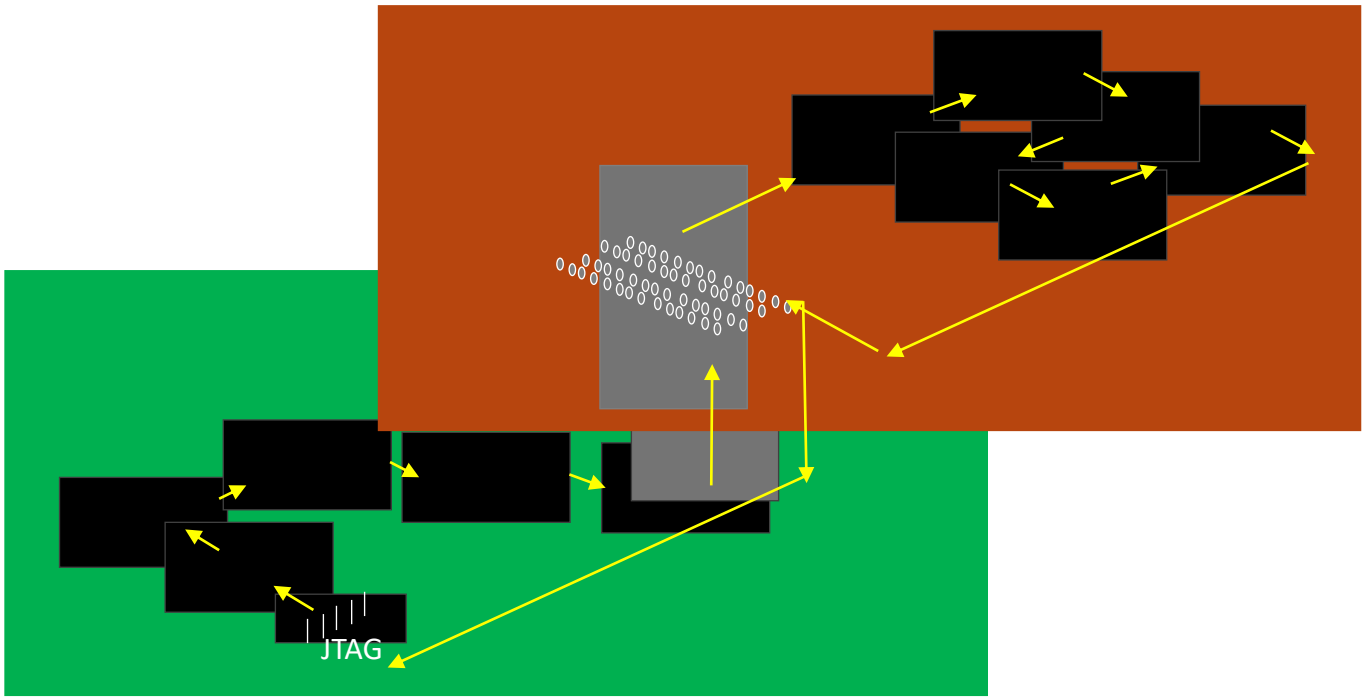


Figure 7 – Boundary Scan Topology for Multi-Board Configuration

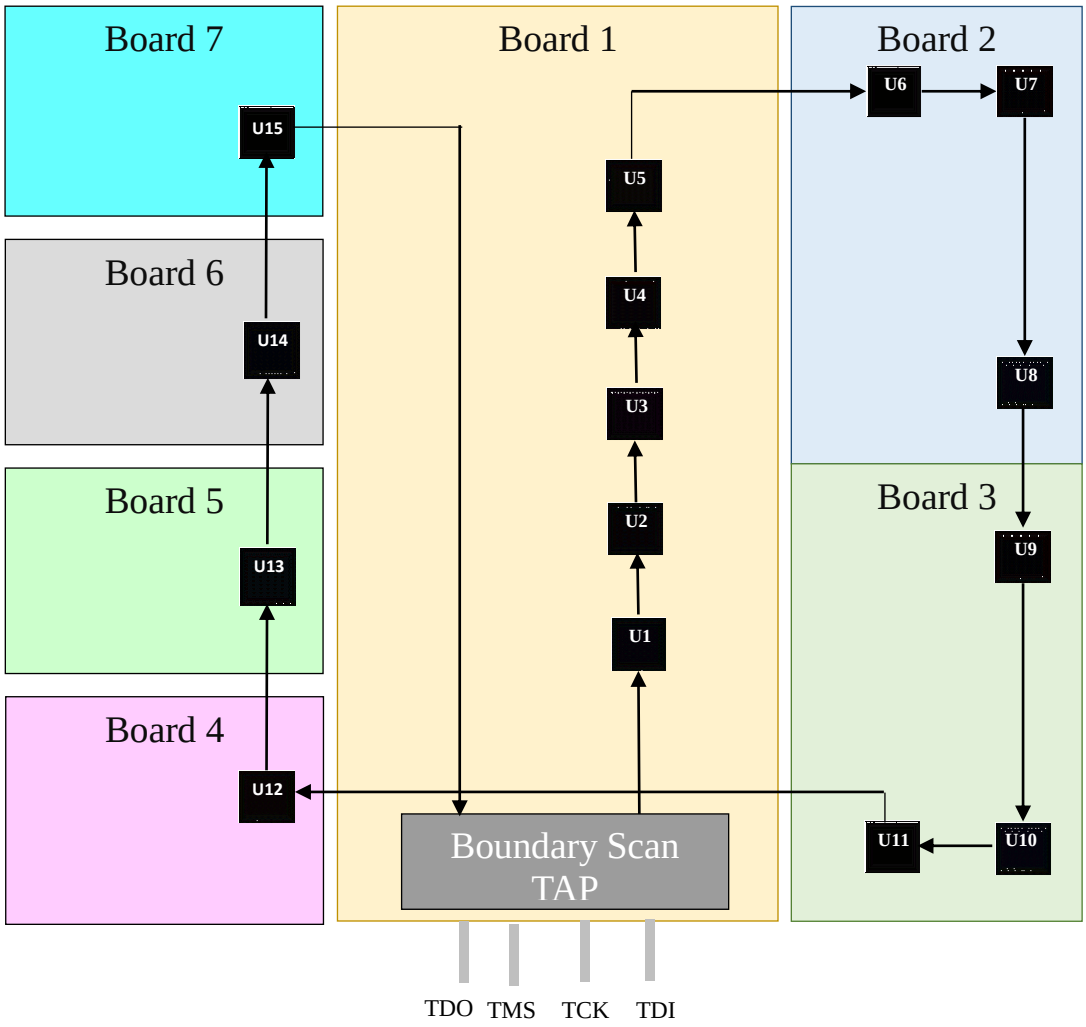


Figure 8 – Boundary Scan Topology for Multi-Board System

In case of multiple board configurations coupled with a programmable device capability to trigger the tests, it provides options to run the tests in any phase of the product life cycle. After assembly of the system, in Environmental Chamber test or in the Field after deployment.

Influence of DFT into Test Strategy

A good DFT from the device level up to a system level, provides flexibility of testing at any stage in the product life cycle.

Figure 9 – Product Test Life Cycle

Design Review

- Review the design right at start with the first cut of files.
- Assess structural testability and BISTs for the ASICs.
- Enables in planning the functional test and mitigation for structural coverage loss.

Prototype Testing

- Turn on maximum testability during the proto phase.
- Validating good DFT in the Design Review will cater for more test coverage.
- This will mitigate the turning-on of functional tests till ready.
- Enable BIST tests to monitor the yield of ASICs.

Mass Production Testing

- Quick turn-on for Mass Production with updates to Proto Test.
- If the yields from BIST tests during Proto Phase is good, it is up to the Program Management team to decide whether to it turn-off.

System Testing

- Once individual boards are assembled into the system and before moving onto Functional tests, the system can be tested to ensure there are no handling defects introduced. Also, the aspect of low level diagnostics ensures saving root causing issues later in the Product Life Cycle.

Environmental Chamber Testing

- If the DFT enables on board programmable device capable of being the Boundary Scan Master, then, running the structural tests can verify how good the structural stability for varying environmental parameters is.

Remote On-Field Testing

- Once the board is shipped, if the DFT has enabled for triggering the test remotely (via on board diags with programmable device as the Boundary Scan master), any issues on the system can be diagnosed before taking a call to RMA.

Benefits of DFT

A good overall DFT enables identifying defects early in the process. You do not want to find these defects to percolate into customer base. A good DFT equips for a comprehensive testability. This maximizes defect detection and in reducing NTF bone pile. The rework on the defects to fix happens in lesser strikes. All of these help in reducing the scrap cost which will add back to savings as an ROI. After adopting this scheme as a well-oiled machinery, the RMA logistics costs will come down. The brand equity will rise.

Early Design Review of Boundary Scan in Enhancing Testability and Optimization of Test Strategy

Sivakumar VijayaKumar
Keysight Technologies

How good is my product?

Is there a guiding principle to influence a good test?

YES

'Design For Test' in short... **DFT**

What is 'Design For Test' or 'DFT'?

It is a concept that influences the design of a component or a system to facilitate in maximizing tests to diagnose maximum defects.

- Involves additional test circuitry added to designs
- Based on Boundary Scan Standard - IEEE 1149.1
- Test tools and methodologies maximizing defect detection

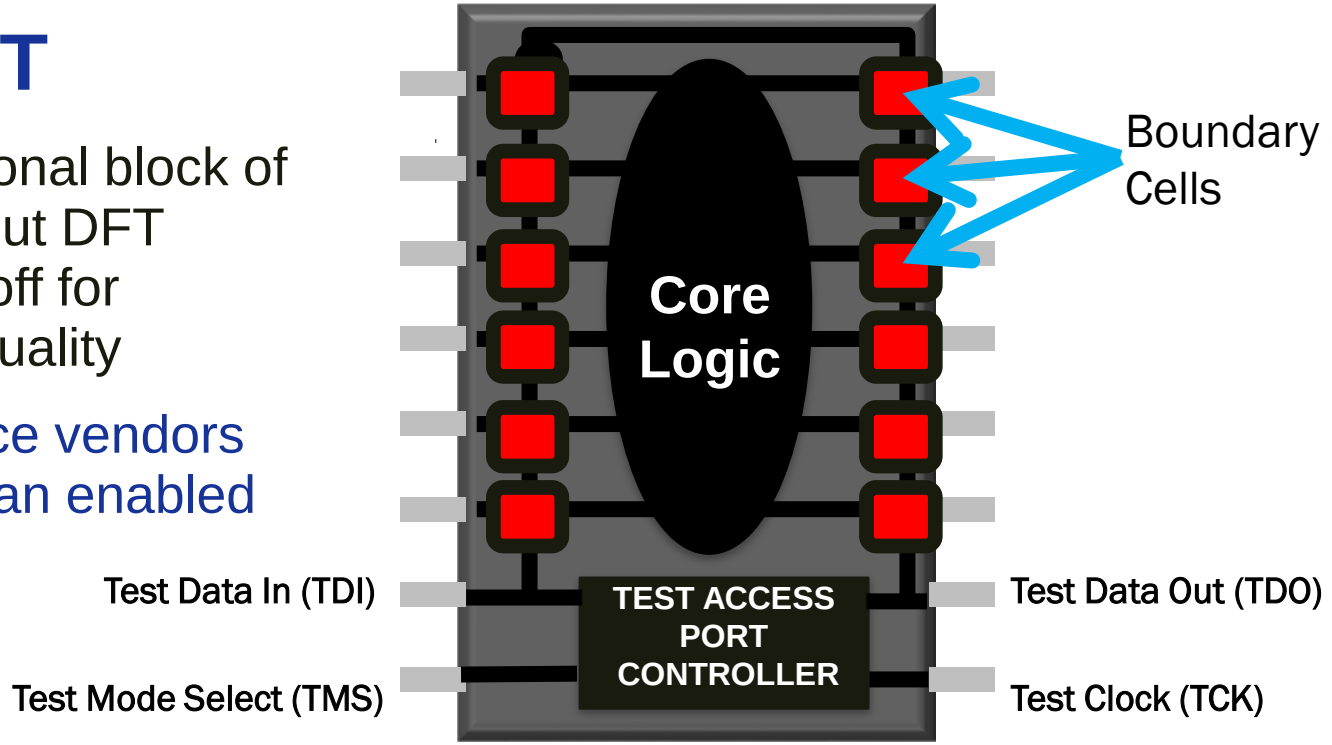
Where all can this concept of DFT span?

- Device level all the way to Systems

Device Level DFT

Device being the foundational block of a system, a well thought out DFT architecture always pays off for enabling determinism of quality

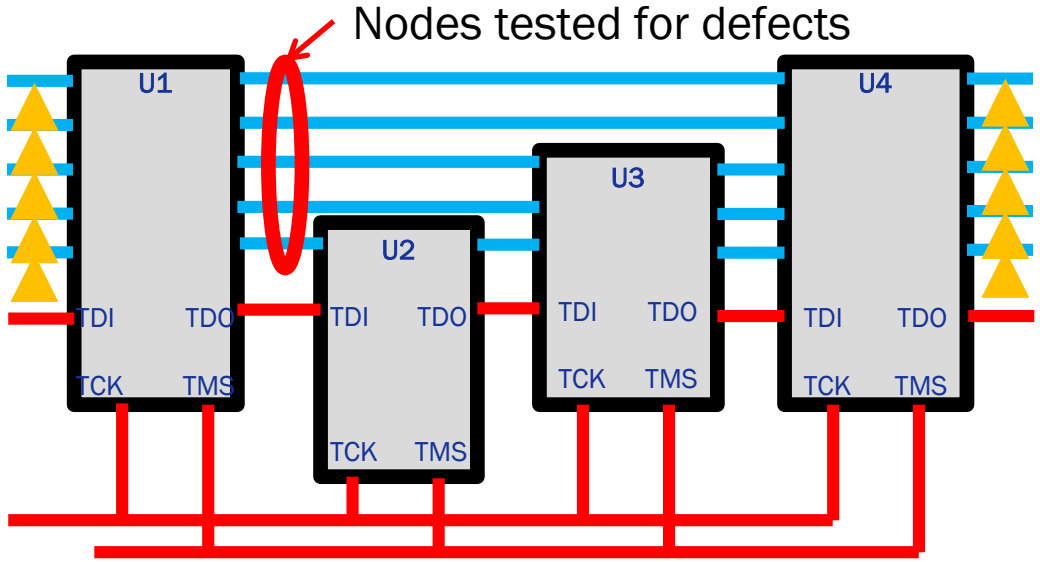
- Rising number of device vendors provided Boundary Scan enabled chip



Device Level DFT – Defect Detection Between Devices Enabled with IEEE 1149.1

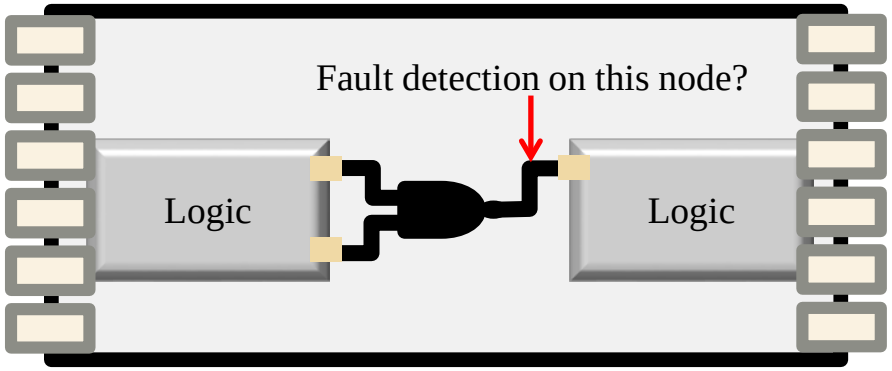
With basic implementation of IEEE 1149.1 enabled devices structural defects on boards arising on digital nodes interfacing with other devices can be detected

- Limits the defect detection to IOs on the devices
- Restricted to type of node interconnects on it



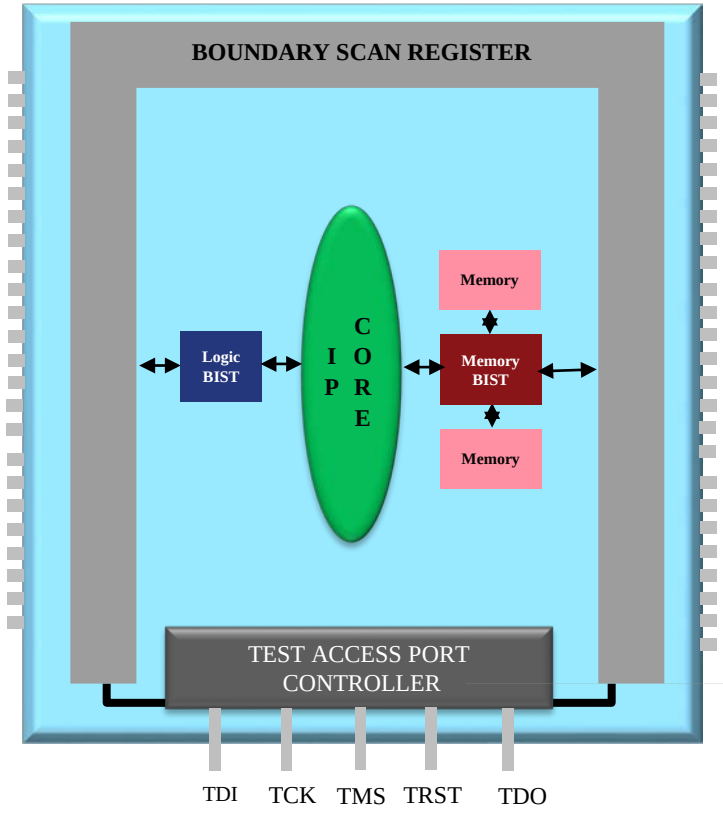
Device level DFT for defect detection inside the device?

- Basic implementation provides structural defect detection to IO interconnects on the devices
- What about defect detection inside the chip?



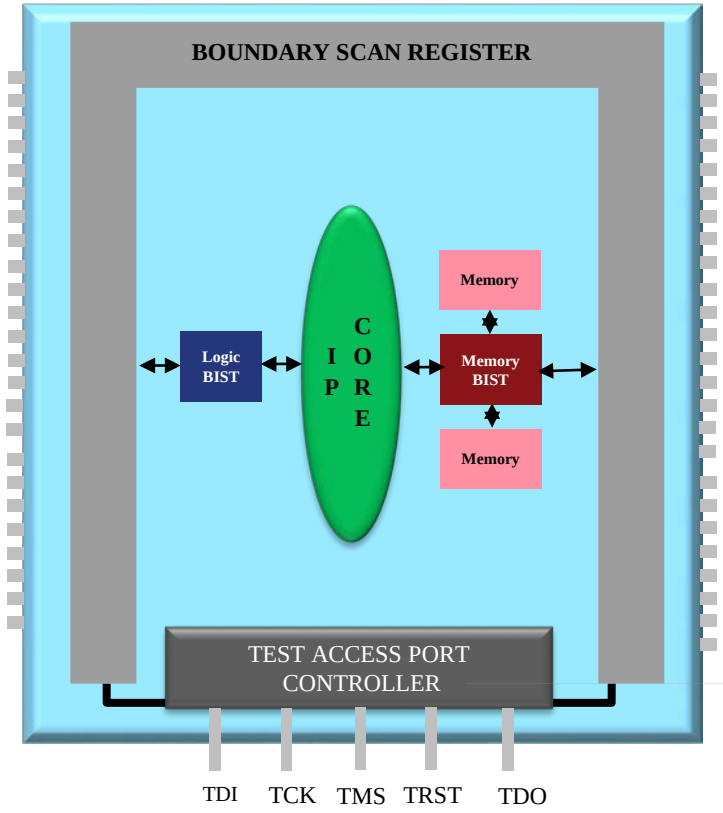
Basic Boundary Scan cells can be leveraged to enable fault detection on nodes inside the chips

Device level DFT for defect detection inside the device - BIST



- Pattern based and scan based test architectures for internal defect detection.
- Scan based test logic in the form of BIST (Built-In Self-Test) has made testing more effective and pervasive that can readily be used at any stage of the product life cycle.
- BIST has made test generation and test application cost-effective. This has enabled in increasing the test coverage to device internals.

Device level DFT for defect detection inside the device - BIST



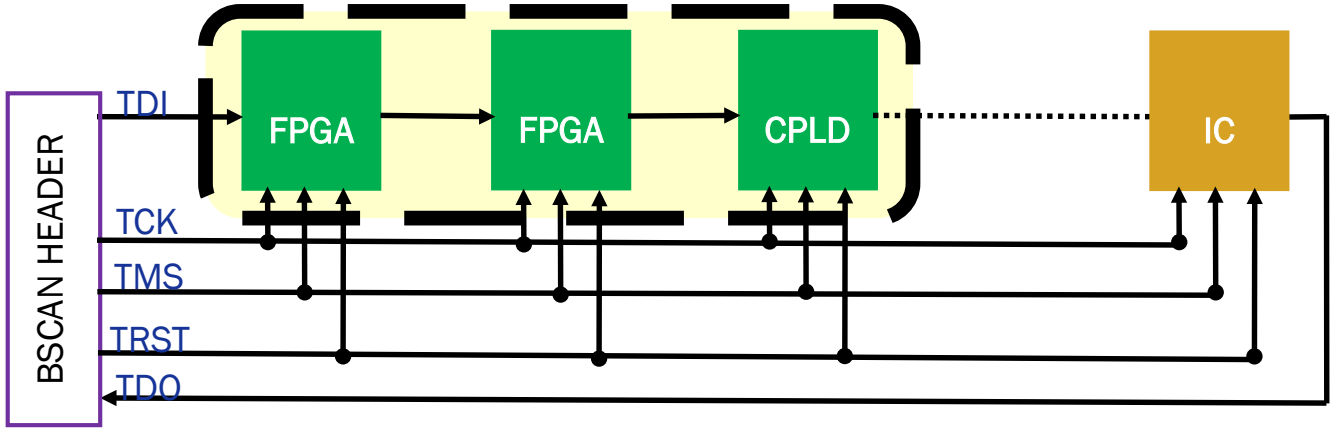
- Increase of System-On-Chip and System-In-Package designs necessitates an architecture for a flexible test methodology to be leveraged in multiple phases of the life cycle, ranging from chip test to system
- Provides flexibility to test at different phases and IPs can be re-used easily into different SOCs.
- Enabling DFT at a device will help in ensuring that the chips are defect free.
- New standards - IEEE 1687 and IEEE 1149.1-2013 standard cater to increasing the test logic within the chips.

What are the elements needed to ensure a good Board Level DFT?

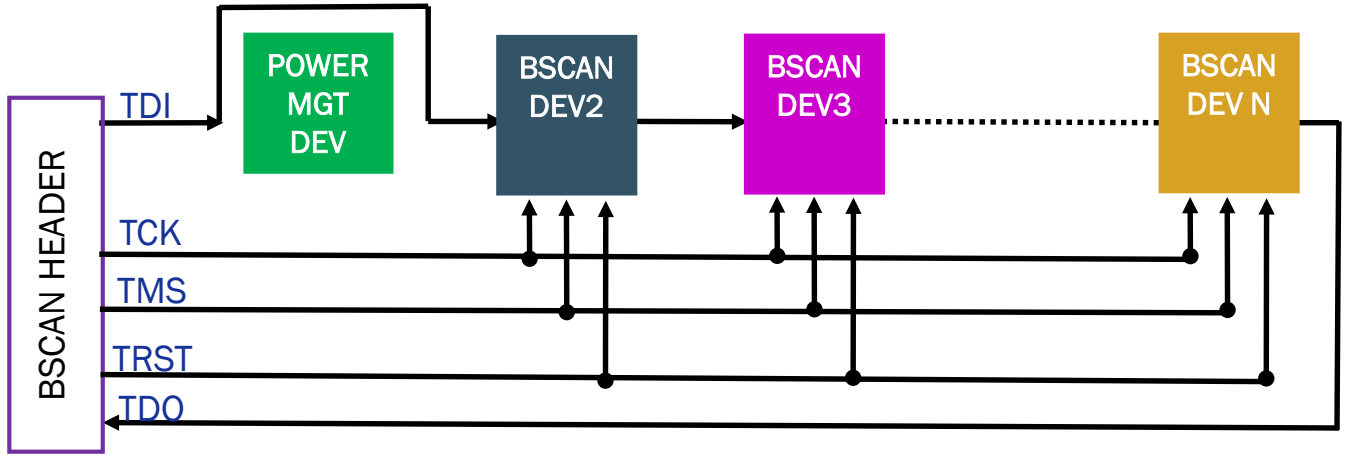
- First step is to choose IEEE 1149.X enabled device for the required functionality, if available.
- Design teams must qualify JTAG enabled parts to supplement into their functional requirements and specifications.
- Qualifying new devices compliant to IEEE 1149.1 standard by Procurement team facilitates an effective process for good DFT.
- Chain the devices with similar logic voltage together

Board Level DFT – Some Basic Good Practices

Devices of similar logic are chained together

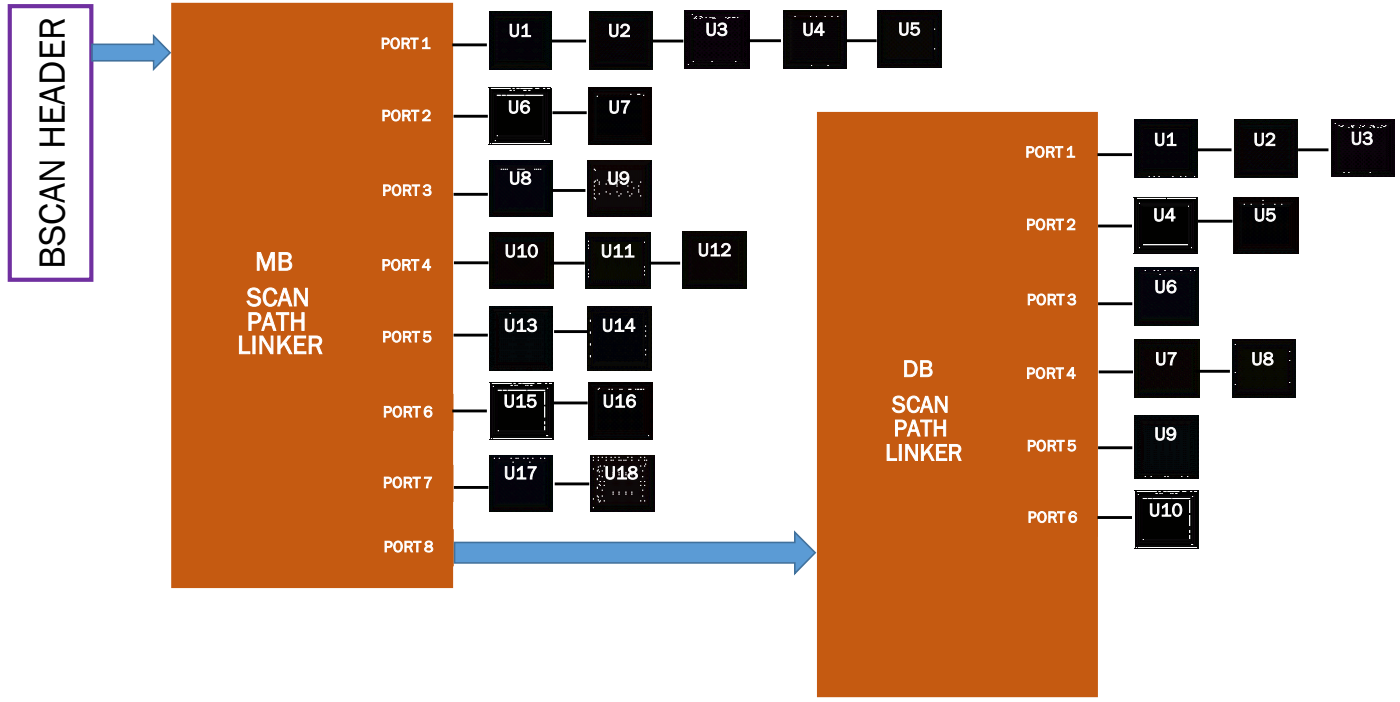


Better to keep Power management ICs, out of the chain as it may affect stability of the board during the test.



Board Level DFT – Good Practices

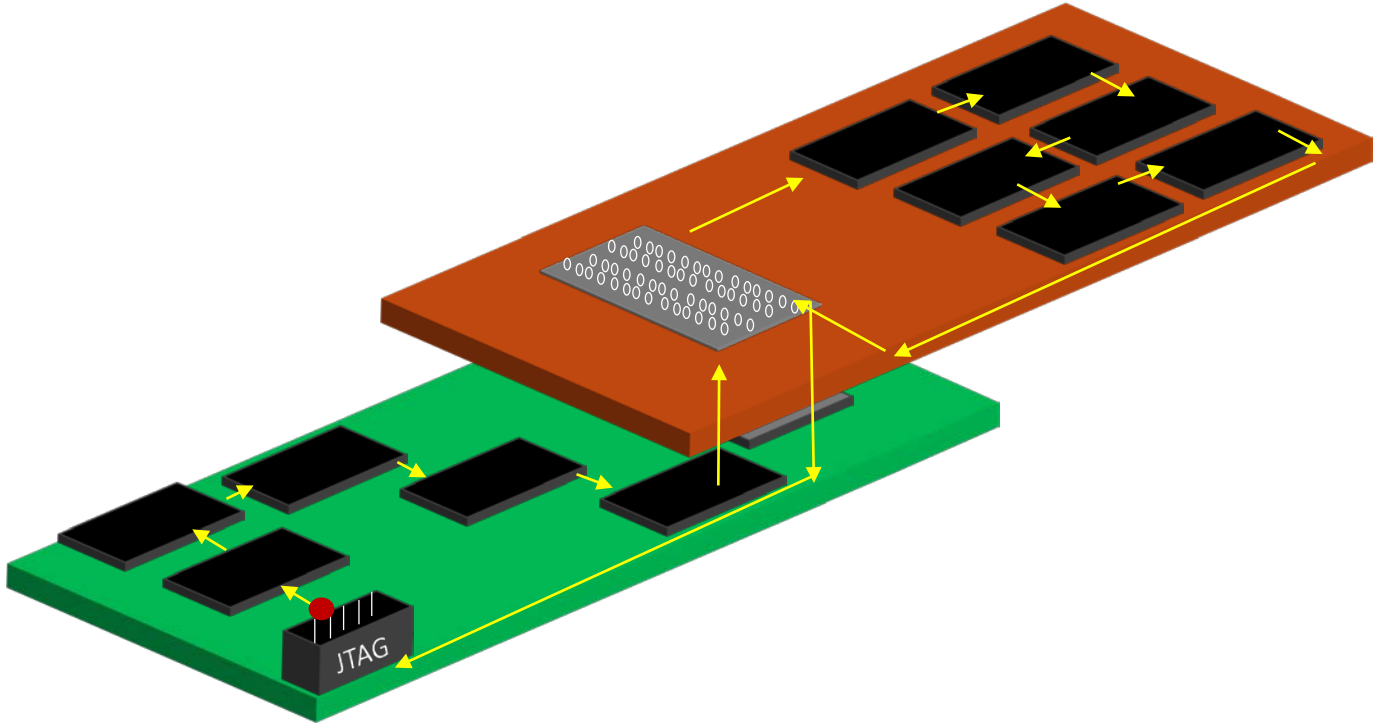
- On complex designs using a CPLD as a scan path linker, provides better management and flexibility of boundary scan chain in test.
- A scan path for each circuit (CPU block, Data Processing block, IO management, Memories, etc.) would help control the TAP signals independently.



Board Level DFT – Good Practices

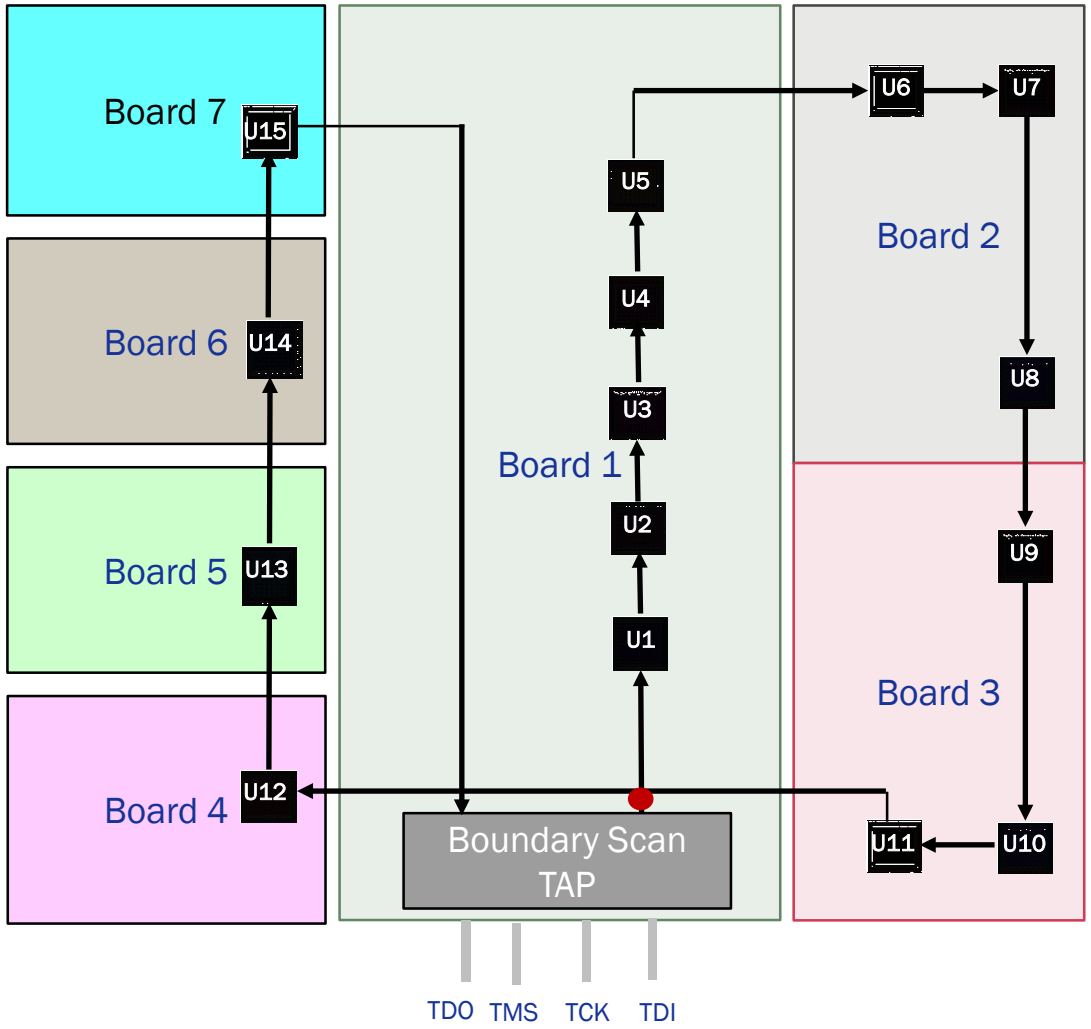
- Dynamic configuration of system constituting multiple boards enables the boundary scan chain to be tested as a system once all the boards are stacked.

- Detects any defects resulting from Board-to-Board connector issues



Board Level DFT – Good Practices

- For multi board configuration programmable device provides options to run the tests in any phase of the product life cycle
  - In Environmental Chamber test
  - In the Field after deployment



Influence of DFT into Test Strategy

A good DFT from the device level up to a system level, provides flexibility of testing at any stage in the product life cycle.

- Review the design right at start with the first cut of files.
- Assess structural testability and BISTs for the ASICs.
- Enables in planning the functional test and mitigation for structural coverage loss.

- Turn on maximum testability during the proto phase.
- Validating good DFT in the Design Review will cater for more test coverage.
- This will mitigate the turning-on of functional tests until ready.
- Enable BIST tests to monitor the yield of ASICs.

- Quick turn-on for Mass Production with updates to the Proto Test.
- If the yields from the BIST tests during Proto Phase is good, it is up to the Program Management team to decide whether to turn it off.

- Once individual boards are assembled into the system and before moving onto Functional tests, the system can be tested to ensure there are no handling defects introduced. Also, the aspect of low level diagnostics ensures saving root cause issues later in the Product Life Cycle.

- If the DFT enables on board programmable device capable of being the Boundary Scan Master, then, running the structural tests can verify how good the structural stability for varying environmental parameters is.

- Once the board is shipped, if the DFT has been enabled for triggering the test remotely (via on board diags with programmable device as the Boundary Scan master), any issues on the system can be diagnosed before making a call to RMA.

Conclusion

- A good overall DFT enables identifying defects early in the process.
- A good DFT helps equip for comprehensive testability. This maximizes defect detection and in reducing NTF bone pile.
- The rework on the defects to fix happens in lesser events.
- All of these help in reducing the scrap cost which will add back to savings as an ROI.
- RMA logistics costs will come down.
- The brand equity will rise.

All of this starts with an early design review of the Boundary Scan circuit, during the design stage of board or system.

Q & A