A System-Level Electrostatic-Discharge-Protection Modeling Methodology for Time-Domain Analysis

Nicolas Monnereau, Fabrice Caignet, David Trémouilles, Member, IEEE, Nicolas Nolhier, and Marise Bafleur

Abstract—**A system level modeling methodology is presented and validated on a simple case. It allows precise simulations of electrostatic discharge (ESD) stress propagation on a printed circuit board (PCB). The proposed model includes the integrated circuit (IC) ESD protection network, IC package, PCB lines, passives components, and externals elements. The impact of an external component on the ESD propagation paths into an IC is demonstrated. Resulting current and voltage waveforms are analyzed to highlight the interactions between all the elements of an operating PCB. A precise measurement technique was designed and used to compare with the simulation results. The model proposed in this paper is able to predict, with good accuracy, the propagation of currents and voltages into the whole system during ESD stress. It might be used to understand why failures occur and how to fix them with the most suitable solution.**

Index Terms—**Electromagnetic compatibility (EMC), electrostatic discharge (ESD), modeling, system level, time-domain simulation.**

During their manufacturing and use phases, electronic products are subject to electrostatic discharges (ESD) disturbances.
In the case of stand-alone circuits, a dedicated ESD protection strategy is implemented inside the silicon chip using protection elements like diodes, silicon-controlled rectifier (SCR), MOSFET etc. The main goal of this strategy is to evacuate the high ESD current from one port to the other, whatever the possible connections exposed to the stress. The first step, to design efficency IC ESD protection is the development of stand-alone protection devices. Semiconductor designers can use various tools to help them in the design and characterization of ICs. Physical modeling tools provide a good estimation of the performance of on-chip protections. These models are validated by a set of measurement methods like transmission line pulsing (TLP) [1], very fast TLP (VF-TLP) [2].

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To ensure that the product is sufficiently robust regarding ESD events, which can occur during the manufacturing process, the very well-known standards like the human body model [3] and charge device model [4] are required.
The ESD protection problem is specific when the ICs are mounted on a printed circuit board (PCB). Electronic equipment operating in real world is subject to more severe ESD stress than in manufacturing ESD-controlled environment. Moreover, complex interactions between passive and active components (ICs, PCB lines geometry, passives. . .) and the environment significantly impact the ESD waveform.
The IEC 61000-4-2 standard test [5] is widely used to evaluate system robustness against ESD. Up to now this standard is the only one available that can be applied on final products like multimedia ones. It does exist another standard called ISO10605, but it is dedicated for automotive applications [6], [7]. The IEC 61000-4-2 standard has been developed twenty years ago for electromagnetic compatibility (EMC) in order to evaluate the ESD susceptibility of systems. It is intended to emulate real world events such as human body discharge into a system. When ESD issues are revealed, there is a lack of investigation's method, which can lead to many unsuccesful system redesigns. Moreover, there are not enough design tools that allow an accurate prediction of the possible ESD propagation paths and events. Designers need modeling methodologies able to simulate the design before prototyping to anticipate ESD failures and provide the most suitable solutions to protect the product combining efficiency and low cost.
In this paper, a methodology to build a behavioral and accurate model of a system is proposed and evaluated to predict current paths during ESD events. A simple system, made up of an inverter and its passive components required for its proper operation, is used to illustrate the proposed modeling methodology. Each part of this system is modeled separately using very-high-speed integrated circuit Hardware Description Language—Analog and Mixed Signals (VHDL-AMS) [8]. The main advantage of using such behavioral description language is to build the complete system level simulation using building blocks that can be assembled hierarchically to model the whole system as represented in Fig. 1.

We will describe how to build each block and to achieve full system modeling. A dedicated PCB including specific measurement methods has been designed to validate the approach and to demonstrate that it is possible to obtain accurate results within a high level of abstraction.

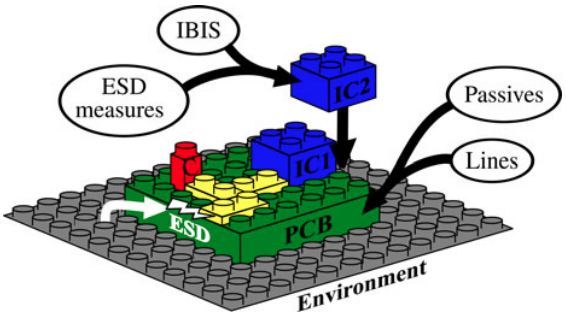


Fig. 1. Schematic representation to build system level generic block's simulation.

This paper is organized in six sections. After this brief introduction, the system, and test methods used to compare the developed simulation methods and measurement methods are presented in Section II. Section III describes how IBIS models are improved for system level simulation. Section IV details the implementation of each block for system modeling. Section V presents analysis of some cases study in which the complex current shape is thoroughly analyzed and explained. Section VI reports comparisons between measurement and simulation.

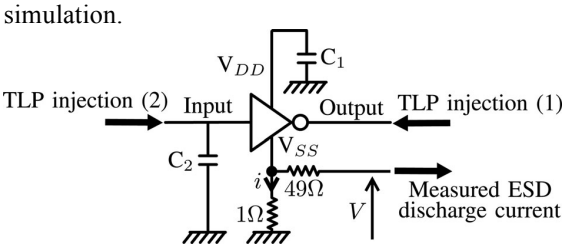


Fig. 2. Studied case schematic with case 1 and 2 injection and "one-ohm measurement" method.

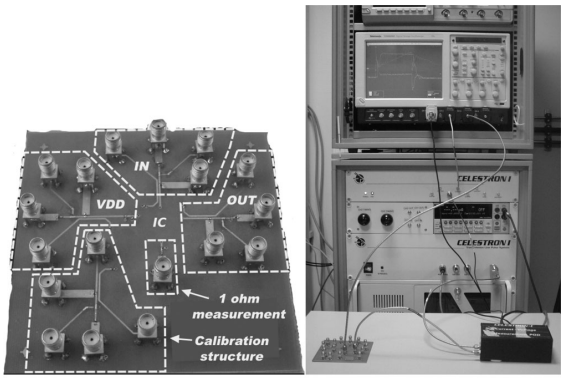
II. PCB AND TESTS METHODS

The studied system is built around a commercial inverter integrated in 0.25-**µ** m CMOS technology. The system is composed of the IC, a few passive components and PCB lines as shown on Fig. 2. Two cases are investigated in this paper.

1) Case 1 : Study of the impact of an external capacitance C1 used for IC power-supply decoupling (between **V**DD and **V**GND) when an ESD event occurs on the output to ground.

2) Case 2 : Study of the impact of an external capacitance connected between the input and ground plane C2. ESD injection is performed on the input to ground.

A dedicated PCB, shown in Fig. 3(a), was realized to perform measurements and ESD injections. All IC pins are connected to SMA connectors through the same PCB layout structure. Depending on the passive components mounted on this dedicated structure, various ways of measurements and injections can be performed. Measurement techniques included on this structure are mainly extracted from EMC standards, which allow measuring the conducted emissions of an IC [9]. To measure the current, which flows into the circuit, a measurement method called "one-ohm measurement" issued from the EMC standard IEC61967 [9] is used. Initially, intended to measure the IC power supply conducted emissions, this technique was used to measure the current that circulate into the circuit during an ESD stress. A 1Ω resistance is inserted into the ground path. The 50Ω impedance adaptation is obtained with a 49Ω resistance.



(a) (b)

Fig. 3. (a) Picture of the test board. The IC is soldered on the bottom layer of the PCB. (b) Picture of the test setup.

Testing at system level is usually done using an IEC 61000-4-2 generator (ESD gun). However, the interpretation of gun, generated complex waveforms, is not straightforward. Moreover, guns can generate perturbations that disturb the measurement [10] and the reproducibility of the pulse is very poor [11]–[13]. Instead, we used a transmission line pulse (TLP) generator.

The TLP setup, shown in the test bench of Fig. 3(b), uses a 1-ns rise time and 100-ns width rectangular pulse. The analysis of the measurement resulting from this TLP waveform allows understanding the impact of each component on the ESD system current propagation. The analysis of the current waveform shape, obtained with the one-ohm measurement, is performed with the help of the simulation.

III. MODELING METHODOLOGY

This section presents the modeling of each system part. To keep a behavioral approach, VHDL-AMS is selected as the description language. The description of the system is split into three blocks: the IC, the PCB, and the external test bench. Parts A, B, and C detail each of these blocks and how to interconnect them.

A. *Circuit Modeling Methodology*

The integrated circuit model is composed of three parts: the package, the ESD protection structures, and the IC core. The interaction between the ESD

protections and the core are not taken into account in this study. The core functionality can be described in VHDL. A previous paper has already presented the ESD susceptibility of the core [14].

1) Integrated Circuit Model From IBIS File: The circuit modeling is based on standardized models called Input Output Buffer Information Specification (IBIS) and also known as ANSI/EIA-656 [15]. This standard allows reproducing the electrical behavioral of input/output buffers of digital circuits in order to predict signal integrity (SI) at system level [16]–[18].

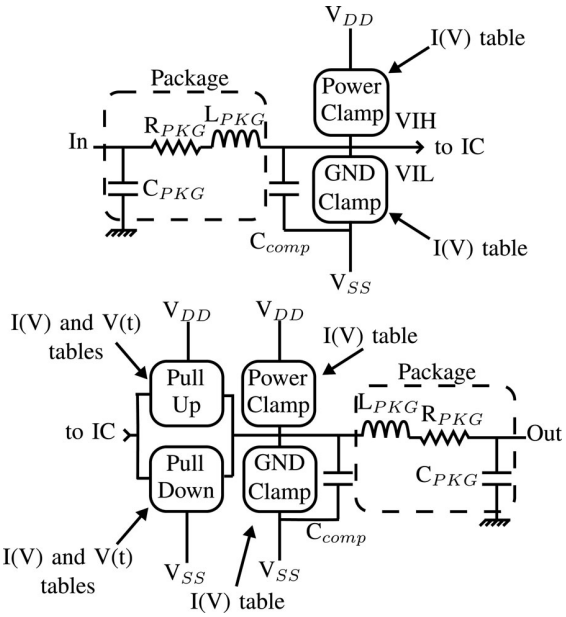


Fig. 4. Typical schematic of IBIS model of (a) input and (b) output.

IBIS models, provided to designers, are a file that contains information for each pin of an integrated circuit. This file format is ASCII text. It contains **I** (**V**) IC buffers and ESD clamps tables, **V** (**t**) tables for the dynamic output buffers, passive elements of the package pins, input and output equivalent capacitances (**C**comp), and others. The schematics of Fig. 4 report a typical IBIS model for (a) input pins and (b) output pins. All data included in IBIS file are obtained from measurements and/or from SPICE simulations in precise configurations defined by the standard depending on the application of the final product. One of the main advantages is that it does not reveal any information about architectural or process, which can compromise the intellectual property of semiconductor manufacturers.

Although IBIS files are very useful for SI simulations, there is no information about ESD protection and, so, is still incomplete for system level ESD simulation. The **I** (**V**) characteristic of ESD clamps (between inputs and output to ground or **V**DD (see Fig. 4) is only given for − 1 **x V**DD to 2 **x V**DD which is not sufficient to cover the full ESD protection responses. Moreover, the ESD current paths are not all considered—for example, the IBIS file does not include the power supply protection between **V**DD and **V**SS pins, or the protections between the various power supplies.

It means that IBIS is not able to reproduce all the current paths that can occur during an ESD event. For all these reasons, IBIS model extension is required to fulfill high current level ESD simulation for all possible ESD paths. In the IC model proposed by us, ESD protections are replaced by other models described in the next two sections.

Moreover, the IC model should take into account the parasitics of the IC to ensure that the dynamic aspects of the ESD impact will be reproduced by simulation. This is performed by reusing the values of passive elements of the packages pins and input/output on-chip equivalent capacitances given by IBIS models as shown in Fig. 5. Finally, the I/O buffer models are kept so that the simulation works even if the IC is powered up or not, in order to reproduce failures into normal operating conditions.

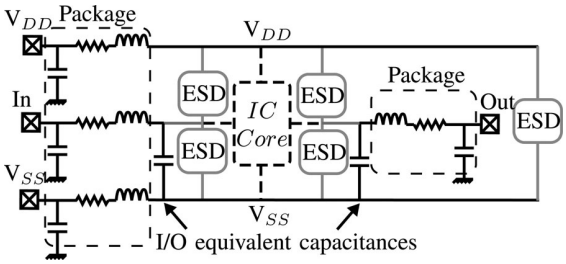


Fig. 5. Typical schematic of model IBIS without the output buffer.

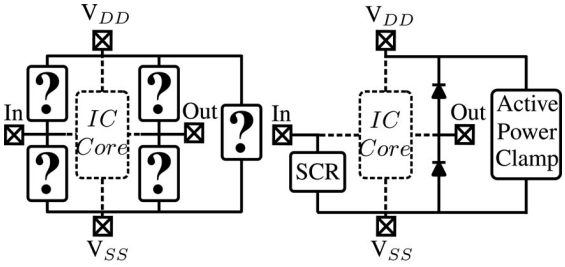


Fig. 6. (a) Typical ESD protection network. (b) Identified protection elements after TLP measurement.

2) Extract Information About ESD Protection: The IC used to validate our ESD modeling approach is a commercial integrated inverter. From the system designer's point of view, no information about its internal structure is available. The manufacturer provides only the data sheet (functionality and electrical characteristics) and IBIS model, but no information that could help for ESD simulation [see Fig. 6(a)].

To extract information from the ESD protections of the circuit, static, and quasi-static (TLP) measurements are performed. An experimented engineer aware of state-of-the-art integrated ESD protection can, however, quite easily identify the

type of protection devices associated with each pin [19], [20]. From the simple circuit studied here, three types of devices were identified: several diodes, an RC triggered power clamp (PC) and an SCR, with a dedicated strategy protection as shown in Fig. 6(b).

The next section will describe how to build the ESD models from TLP and static measurements.

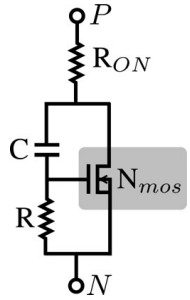


Fig. 7. Power clamp model.

3) Modeling of ESD Protection Based Only on Measurements:

Models of IC-internal protections need to be simple enough to allowfast calculation and good convergence. Acoarse behavioral model can easily introduce many discontinuities either on the signal or its derivatives and then induce serious convergence issues. Here, our basic idea consists in using equations known to represent correctly the device behavior and known to offer good simulation convergence. As will be shown, these physically based equations are simplified as much as possible to reach a minimum set of parameters. Strictly speaking, these model parameters are not physical anymore. The proposed model type is thus somewhere in between physical and behavioral.We only consider the quasi-static protection devices behavior. Notice that most ESD protection dynamic effects are already taken into account by the input/output equivalent capacitances provided in the circuit IBIS file.

The diode model is built upon the very classical diode current equation including a serial resistance:

$$i_d = i_s \times \left[\exp\left(\frac{v_d - R_{\text{on}} \times i_d}{N_f \times U_t}\right) - 1\right] \quad (1)$$

with $\mathbf{U_t}$ being the thermodynamic voltage.

The diode model has three parameters: $\mathbf{i_s}$, $\mathbf{N_f}$, and $\mathbf{R_{on}}$ that are, respectively, the reverse-bias saturation current, nonideality coefficient, and serial resistance of the diode. $\mathbf{i_d}$ is the current through the diode and $\mathbf{v_d}$ is the voltage across the diode.

Equation (1) is directly implemented into the VHDL-AMS as this type of language allows the use of implicit equation, which often eases the modeling work. To build the model, each diode parameters are extracted by fitting the measurement data.

The RC triggered clamp model is based on the schematic proposed in Fig. 7. Three parameters allow defining the power clamp model: the serial resistance $\mathbf{R_{on}}$, **R,** and **C** ,which together are the triggering elements that control the gate of an NMOS transistor. For the MOS transistor, we use classical level-one MOS equations composed of three regions: no current below the threshold voltage (2), a linear region (3), and a saturation region (4). We also have to define an additional "Size" parameter that actually corresponds to the transconductance and W/L product

1) When $\mathbf{V_{gs}} \leq \mathbf{V_t}$

$$i_{ds} = 0 \quad (2)$$

2) When $\mathbf{V_{gs}} \geq \mathbf{V_t}$ and $\mathbf{V_{ds}} < (\mathbf{V_{gs}} - \mathbf{V_t})$

$$i_{ds} = \text{Size}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (3)$$

3) When $\mathbf{V_{gs}} \geq \mathbf{V_t}$ and $\mathbf{V_{ds}} \geq (\mathbf{V_{gs}} - \mathbf{V_t})$

$$i_{ds} = \frac{\text{Size}}{2}(V_{gs} - V_t)^2. \quad (4)$$

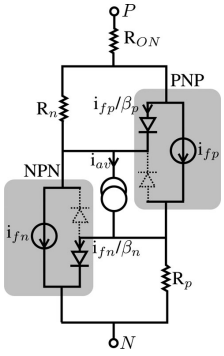


Fig. 8. SCR model, forward bias diode model are not represented.

The RC triggering element's values and the MOS size is adjusted by fitting both the TLP I (V) curve and the transient behavior of the device during TLP pulses. The reverse operation, which involves the drain-substrate diode, is modeled by a diode connected in parallel using the previously described diode model.

SCR reverse-operation model is based upon the most simple bipolar transistor transport model (simplified Gummel and Poon [21]) as represented in Fig. 8. The current $\mathbf{i_f}$ is thus represented by a simple diode-like exponential as follows:

$$i_f(n/p) = i_{\text{sat}} \times \left[\exp\left(\frac{V_{\text{BE}}^{\text{NPN/PNP}}}{N_f \times U_t}\right) - 1\right] \quad (5)$$

with $\mathbf{i_{sat}}$ being the diode's reverse-bias saturation current, $\mathbf{N_f}$ being the diodes nonideality coefficient, and $\mathbf{U_t}$ being the classical thermodynamic voltage.

For the SCR forward operation, the collector-base diodes of both npn and pnp bipolar transistors are not even included in the model and replaced by a dedicated diode model, described earlier.

An avalanche current source $\mathbf{i_{av}}$ is added for the

triggering. The avalanche current is computed in the function of the collector current of NPN transistor from the following expression:

$$i_{\mathrm{av}} = (M-1) \times ic_{\mathrm{NPN}} \tag{6}$$

where **M** is the avalanche multiplication factor of the junction collector/base of NPN, given by the Miller expression [22]:

$$M = \frac{1}{1-\left(\frac{V_{\mathrm{CB}}}{V_{\mathrm{BV}}}\right)^{m}} \tag{7}$$

with **VCB** being the voltage across the junction collector base, **VBV** being the breakdown voltage, and 2 < **m** < 6 being an arbitrary factor depending on junction characteristics.

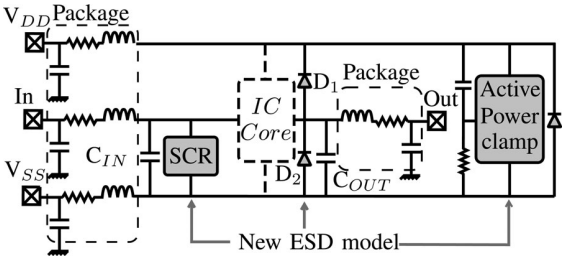


Fig. 9. Simplified ESD integrated circuit model.

When the voltage **VCB** reaches the breakdown voltage value **VBV**, the **iav** source provides the necessary current to trigger and hold the SCR. Modeling the avalanche source from (6) and (7) is critical regarding convergence issues. Indeed, the multiplication factor expressions suffer from a sudden change of sign near the breakdown. In order to avoid the change of sign, the Miller expression is derived from the Taylor series:

$$M \approx \sum_{j=0}^{Nb} \left(\frac{V_{\mathrm{CB}}}{V_{\mathrm{BV}}}\right)^{j} \tag{8}$$

with Nb , the number of terms. This development corresponds to a geometric sequence and thus

$$M \approx \frac{1-\left(\frac{V_{\mathrm{CB}}}{V_{\mathrm{BV}}}\right)^{Nb+1}}{1-\left(\frac{V_{\mathrm{CB}}}{V_{\mathrm{BV}}}\right)}. \tag{9}$$

This last expression is used as the multiplication factor M in the model (6). The parameter Nb is the number of terms of the mathematical series. It can be adjusted to high value for better accuracy. A lower value reduces the accuracy but leads to a smoother variation that helps convergence. We found Nb = 100 as a good compromise. Note that this expression of M is not defined for a voltage exactly equal to the breakdown voltage. However, the expression is continuous around this point, and its value can be calculated at this point.

We finally obtain a five-parameter model with Beta (β_p /β_n) being the bipolar transistor current gain, **isat** and N_f being the diodes nonideality coefficient and saturation current, respectively, **VBV** being the breakdown voltage, and **Ron** being the serial resistance of the SCR.

Diodes RC triggered PC and SCR protection models are combined with the previously described IBIS elements to model the whole ESD circuit. Fig. 9 shows the simplified schematic of the IC model obtained by this methodology. The conduction of the PC is modeled by a diode for its reverse-biased operation.

4) Model Verification and Discussion:

The validity of the model is checked on the discharge paths that involve more than one protection element. In all cases, we observed a discrepancy lower than 20%. The largest discrepancy results are shown in Fig. 10 for a stress injected between Out and Vss pins.

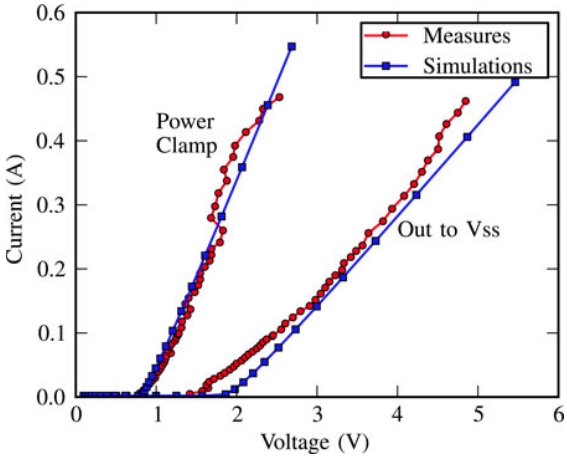


Fig. 10. TLP measurements and simulations of the power clamp (**VDD** to **Vss**) and of Out to **Vss** stress that combines two protection elements (diode + PC).

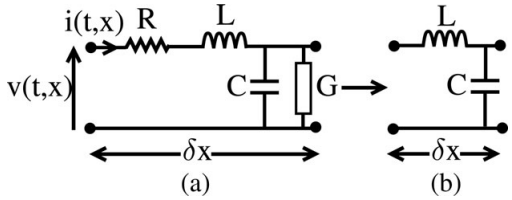


Fig. 11. (a) Elementary length transmission lines and (b) simplification for ESD propagation into PCB.

B. Print Circuit Board Modeling Methodology

Two kinds of generic PCB line models have been developed to take into account propagation effect and crosstalk phenomena. The simple line, modeling the propagation, consists in the distribution of an elementary length of a transmission line. Generally, the elementary transmission line elements are modeled with four parasitics elements [23] as shown in Fig. 11(a): R (serial resistance in ohms), L (serial inductance in Henry), C (parallel capacitance in farads), and G (parallel conductance in Siemens). According to these parameters, the expression of the line impedance can be established as follows:

$$Z_C = \sqrt{\frac{R + jL\omega}{G + jC\omega}}. \quad (10)$$

In most general cases, the line impedance is complex. However, the good quality of the conductors used in PCB (copper) as well as the good quality of the substrate dielectric generally result in the "weak losses" condition that implies: $R << jL\omega$ and $G << jC\omega$. The characteristic impedance is then purely real

$$Z_C = \sqrt{\frac{L}{C}}. \quad (11)$$

Fig. 11(b) shows the simplified elementary length where only the L and C effects are taken into account. These simplifications have been validated in a previous work done by Lacrampe [24] using a TDR-like method based on a VF-TLP tester. The line parameters depend on geometric dimensions (length L , width W , thickness t, and substrate height H) and on the dielectric constant εr of the material used for the PCB (FR-4 epoxy for the studied case). The inductance and capacitance per unit length are computed from these parameters and equations given by Bakoglu [25].

PCB lines are discretized in n portions by taking as an assumption the quasi-transverse electromagnetic (TEM) approximation [26]. To carry out this serialization of the various line portions, we programmed a generic code module having as inputs the values of the capacitance and the inductance per unit length and the number of lumped elements. An example of the VHDL-AMS code is given bellow (see Fig. 12) showing the advantage of using a behavioral description.

```
ENTITY LC_line IS
  generic ( L_val : real; C_val : real ; n :
      natural);
    -- L_val: inductance per unit length
    -- C_val: capacitance per unit length
    -- n: number of LC module
  port (terminal a,b,c : electrical);
END ENTITY module_line;

ARCHITECTURE behavioral OF LC_line IS
terminal T : electrical_vector (1 to n-1);
BEGIN
  fst  : entity module_LC generic map (L_val,
      C_val) port map (a,T(1),c);
  loop : for i in 1 to n-2 generate
    LC : entity module_LC generic map (L_val,
        C_val) port map (T(i),T(i+1),c);
  end generate loop;
  lst  : entity module_LC generic map ( L_val,
      C_val) port map (T(n-1),b,c);
end ARCHITECTURE behavioral;
```

Fig. 12. VHDL-AMS code to model PCB line using LC module.

Another model has been built to take into account crosstalk phenomena between several lines. The coupling effect is modeled by inserting a mutual inductance and capacitance per unit length on elementary length as shown on Fig. 13. These elements are computed from geometry with the equations proposed by Sohn et al. [27]. The generic model, described in VHDL-AMS, allows the prediction of the noise coupled between lines. This model has been validated for ESD in [14].

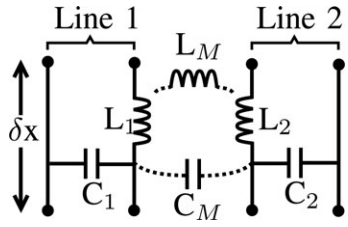


Fig. 13. Methodology of PCB lines connections.

Two generic modules have been developed to model the whole PCB: one module named "LC line" for propagation and a second module named "LC line coupled" to take into account coupling effect between several lines. The methodology of the generic model's connections is illustrated in Fig. 14. Depending on the interaction between the lines, each segment is modeled by a module, which takes into account the impedance, length, and optionally the coupling effect. In the portion III and I, there is no coupling effect between lines. So, the module "LC line," without coupling effect, is appropriate. In portion II, where lines are close, the "LC line coupled" module is used to take into account crosstalk between lines.

Following the assembly methodology presented, it could be easy to extract an equivalent Hardware Description Language (HDL) from PCB layout by automatic extraction's software.

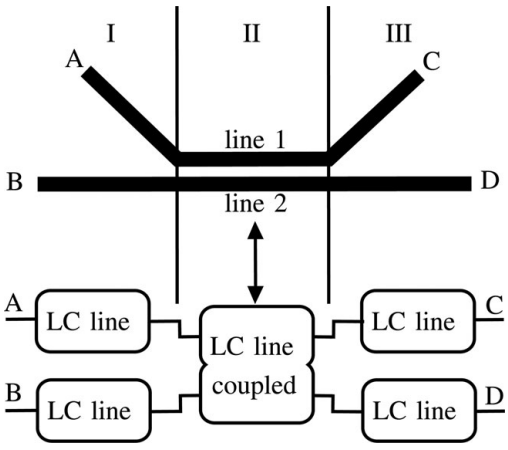


Fig. 14. Methodology of PCB line connections.

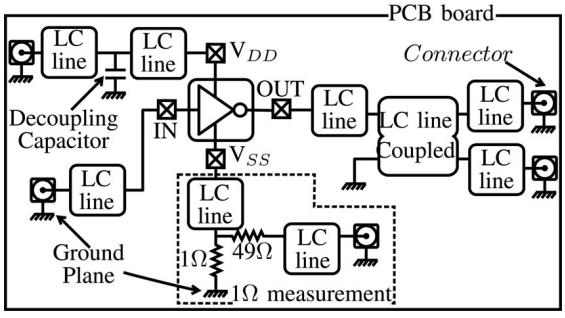


Fig. 15. Simplified PCB model.

C. Full System

This section presents the modeling of case 1 discharge configuration, between output and ground plane. All the other configurations of ESD discharge stress are modeled and can then be analyzed in a similar way.

The integrated circuit elements, such as package, I/O capacitances from IBIS and ESD protections modeled from measurements, are assembled with the generic blocks previously described. The methodology of PCB lines connections, described in the previous section, is applied to form the PCB block. IC and PCB block are assembled hierarchically as shown in Fig. 15. It has to be noticed that only the main PCB lines are reported on the schematic, but the whole PCB lines are modeled. The PCB block includes the line injection connected to the pin "OUT," the one-ohm measurement technique connected to the **V**SS pin, and the decoupling capacitance connected to the **V**DD pin.

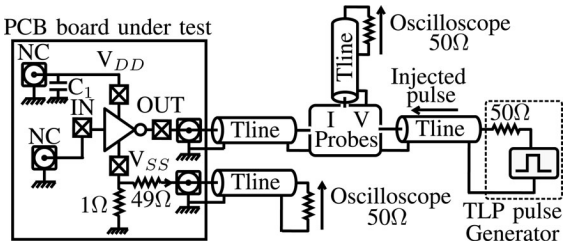


Fig. 16. Simplified system model for ESD discharge between output and ground plane.

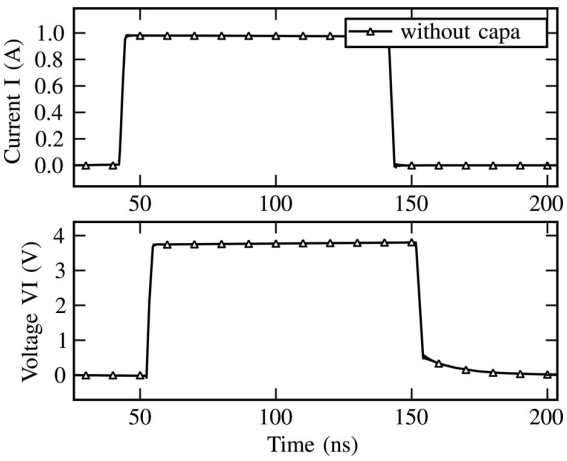


Fig. 17. Simulations of the current I in the 1-Ω ground resistance and internal voltage VI across the power clamp for 1-A TLP pulse injected from output to ground, without IC decoupling capacitance.

To model the whole system, it is necessary to consider all the external elements including generator and cables. The discharge configuration between output and ground plane takes into account the test bench as shown in Fig. 16. A pulse voltage source in series with a 50-Ω resistance is used to represent the TLP generator. Connections between the oscilloscope, the TLP generator, and the PCB board are modeled by simple transmissions lines (Tline) with 50-Ω impedance whose delay is adjusted to match with the cable delay. Current and voltage probes, represented in Fig. 16, correspond to the probe of the TLP tester. This allows measuring the injected and reflected waveforms.

To summarize the methodology to build the full simulation scheme, the device model (including package protection strategy and IC core), PCB, cables, measurement test bench, and generator are clearly separated. It will be shown in the following paragraphs that simulations reveal the interactions between each of these model elements.

IV. Simulation of the Whole System

A. Case 1: Decoupling Capacitance Connected Between VDD and Vss

In this section, the simulation of the whole system is analyzed for various IC's decoupling capacitance values (50 nF, 14 nF, and no capacitance). The TLP pulse has the following characteristics: amplitude : 1 A; pulsewidth : 100 ns; and rise time: 1 ns.

Fig. 17 shows the simulation results when the decoupling capacitance is not connected. The current I corresponds to the current that circulates through the 1-Ω resistance. VI is the internal voltage of the IC between **V**DD and **V**ss pins, across the power clamp. The whole injected current flows through the 1Ω resistance. As expected by the protection strategy of the IC, the discharge current flows through the output diode D1 and the power clamp.

If a 50nF decoupling capacitance is connected between **V**DD pin and the ground plane, the shape of the current I through the 1Ω resistance is significantly different as shown in Fig. 18.

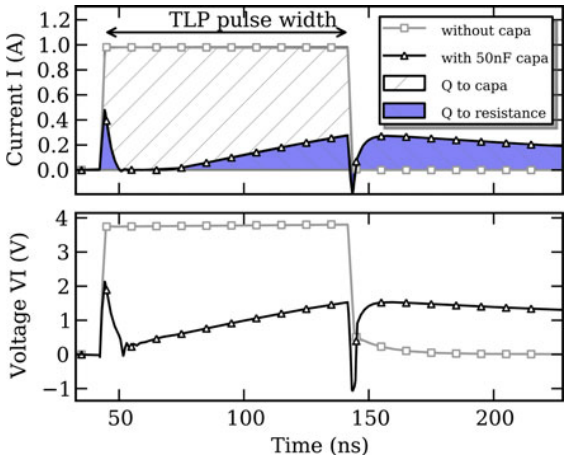


Fig. 18. Simulations of the current I in the 1-Ω ground resistance and internal voltage VI across the power clamp for 1-A TLP pulse injected from output to ground, without IC decoupling capacitance.

Complex interactions between the chip, its package, the PCB lines, and the decoupling capacitance are observed.

Simulations of the current I in the 1-Ω resistance and internal voltage VI across the power clamp for one ampere TLP pulse injected between output and ground were carried out to compare the two

configurations: with and without 50-nF decoupling capacitance.

The external decoupling capacitance defines the internal potential between $\mathbf{V}_{DD}$ and $\mathbf{V}_{SS}$ (VI). Initially, there is no charge on the decoupling capacitance, voltage VI is equal to zero, and the power clamp is closed. When an ESD stress occurs on the output pin, the current goes through the diode D1. Because the capacitance is directly connected to the ground, the current path can flow either through the PC or through the capacitance. In this case, the decoupling capacitance offers a lower impedance than the power clamp, creating a preferential path for the ESD discharge current from the $\mathbf{V}_{DD}$ pin to ground.

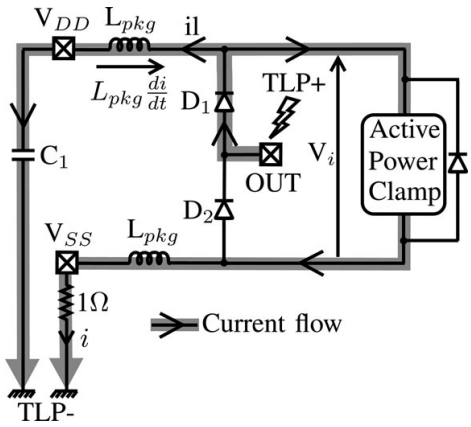


Fig. 19. Simplified schematic showing the ESD current path into the circuit over fast TLP rising edge with 50-nF decoupling capacitance at $\mathbf{t}_0 + \boldsymbol{\varepsilon}$.

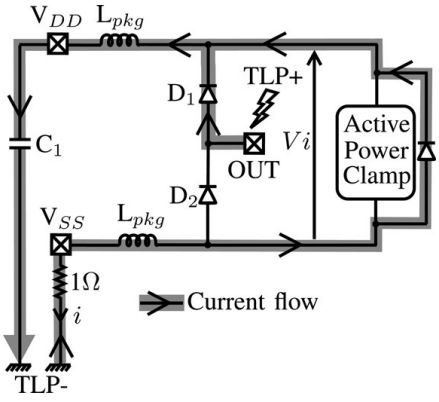


Fig. 20. Simplified schematic showing the ESD current path into the circuit on fast TLP falling edge, with 50-nF decoupling capacitance at $\mathbf{t}_4$.

The current peak observed on the resistance needs explanation. During the fast TLP rising edge, between $\mathbf{t}_0$ and $\mathbf{t}_1$ (see Fig. 18) the inductive effect of the package allows the PC to conduct some current for a very short time. This is because the package inductance is not able to drive current instantaneously respecting the basic equation $\mathbf{V} = \mathbf{L}_{pkg}\,(\mathbf{di/dt})$. So, the voltage across the $\mathbf{V}_{DD}$ package inductance increases strongly. The threshold voltage of the PC is reached allowing the conduction of the current. Fig. 19 shows the current path into the circuit during TLP rising edge.

Just after the TLP rising edge at $\mathbf{t}_1 + \boldsymbol{\varepsilon}$, the inductive effect decreases, voltage VI decreases and the power clamp switches OFF.

During the following interval time, $\mathbf{t}_2$ to $\mathbf{t}_3$, all the current directly goes out of the chip and the external capacitance begins to charge up. No current circulates through the 1-Ω resistance.

When the charge voltage of the capacitance reaches the triggering voltage of the PC, at $\mathbf{t}_3$, the PC conducts more and more current as the capacitance still charges up gradually. When the TLP pulse begins to fall, at $\mathbf{t}_4$ (returns to zero), a negative peak current is visible on the simulation. It can be explained by what we could call "the package inductance balance effect." Just before the TLP pulse end at $\mathbf{t}_4 - \boldsymbol{\varepsilon}$, the current circulates mainly in the package $\mathbf{V}_{DD}$ inductance (about 700 mA/1-A injected) to charge the external capacitance. When the ESD-pulse currentflow stops, the current continues to circulate through the $\mathbf{V}_{DD}$ package inductance forcing the PC to conduct a reverse current to fulfill the "inductance balance effect." The current path into the circuit during TLP falling edge is presented in Fig. 20.

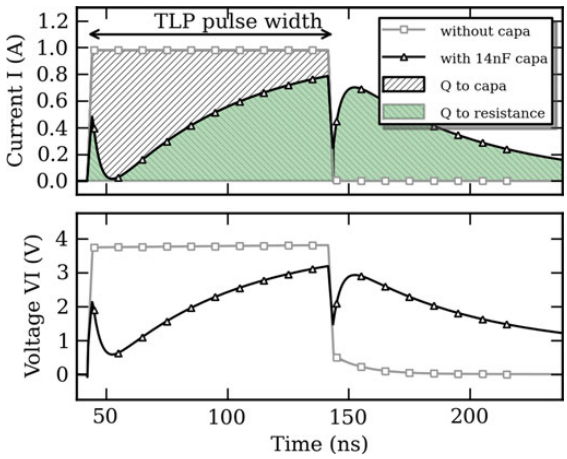


Fig. 21. Simulations of the current I in the 1-Ω ground resistance and internal voltage VI across the power clamp for 1-A TLP pulse injected from output to ground, with 14-nF decoupling capacitance.

After the TLP pulse ends at $\mathbf{t}_5 + \boldsymbol{\varepsilon}$ (returns to zero), the decoupling capacitance discharges through the PC until the RC triggering circuitry turns it OFF. It is noted that even if the external capacitance absorbs a great part of the energy stress corresponding to the white hatched area in Fig. 18, the PC must conduct within a time delay considerably longer than the stress duration to evacuate the charge accumulated inside the capacitance.

Even if the current through the PC during the TLP pulse (gray on Fig. 18) is smaller than the whole current injected, the PC continues to discharge current. It implies that the decoupling capacitance increases the time required by the PC to shunt the current.

When the PC stops conducting (i.e., the sustaining voltage goes below the transistor holding voltage), the remaining charges in the capacitance are then locked and the capacitance maintains a high voltage between $\mathbf{V}_{DD}$ and **Vss**. This could have a crucial impact on the susceptibility when the system is powered-up.

Results with a 14 nF decoupling capacitance are shown in Fig. 21. The capacitance charges up more rapidly during the TLP pulse. At $\mathbf{t}_3$, the voltage capacitance increases more rapidly, and results in a shift of the PC triggering.

The current path is the same except at $\mathbf{t}_4$ when the TLP pulse begins to return to zero. At $\mathbf{t}_5 - \boldsymbol{\varepsilon}$, the current circulates mainly in the package **Vss** inductance (about 700 mA) to the 1-Ω resistance. The current that circulates through the capacitance is only 300 mA. When the ESD-pulse stops, the current continues to circulate through the **Vss** package inductance forcing the PC to conduct the current in a same way to fulfill the "inductance balance effect." This explains why the peak on the one-ohm measurement at $\mathbf{t}_4$ is not negative. Depending on the decoupling capacitance value (14 and 50 nF), the current path varies when TLP pulse end, and the PC can switch from direct to reverse mode very quickly.

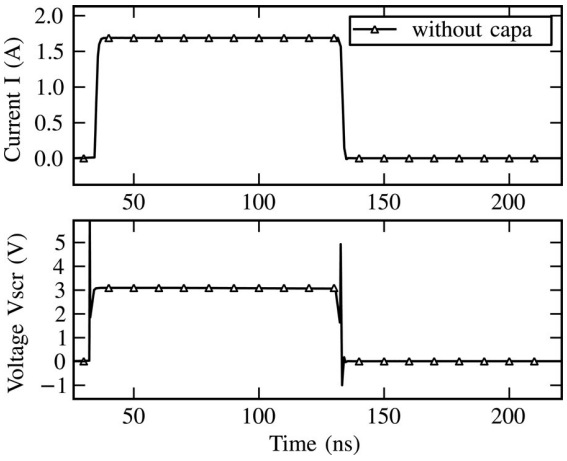


Fig. 22. Simulations of the current I in the 1-Ω ground resistance and internal voltage $\mathbf{V}_{scr}$ across the SCR for 1-A TLP pulse injected from input to ground, without capacitance.

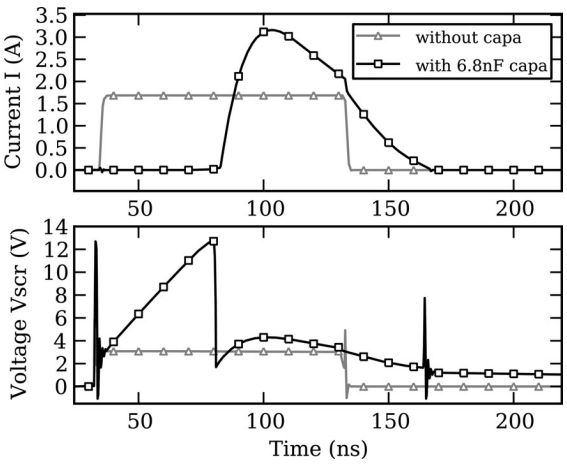


Fig. 23. Simulations of the current I in the 1-Ω resistance and internal voltage $\mathbf{V}_{scr}$ across the SCR for 2-A TLP pulse injected between input and ground plane, comparison with and without 6.8-nF capacitance.

B. Case 2: Capacitance Connected Between the Input and Ground Plane

The TLP generator is connected between the input and ground plane and has the following characteristics: amplitude : 2 A; pulsewidth : 100 ns; and rise time : 1 ns. The impact of an external capacitance connected in parallel with an SCR internal-IC protection is analyzed.

Fig. 22 shows the simulation results when the capacitance is not connected. The current I corresponds to the current that circulates through the 1-Ω resistance. $\mathbf{V}_{scr}$ is the internal voltage of the IC across the SCR. Due to impedance discontinuities between TLP generator, 50-Ω cable and 110-Ω PCB lines, the injected current level is about 1.7 A. The whole injected current flows through the 1-Ω resistance. As expected by the protection strategy of the IC, the discharge current is sunk by the SCR in forward mode.

When a 6.8-nF decoupling capacitance isconnected betweeninput pin and the ground plane, the shape of the current I is strictly different as shown in Fig. 23.

The external capacitance actually defines the internal potential between the Input and **Vss** ($\mathbf{V}_{scr} = \mathbf{V}_{c2} - \mathbf{V}_{R1\Omega}$). Initially, there is no charge on the capacitance and no current circulates through the 1Ω resistance. Voltage $\mathbf{V}_{scr}$ is equal to zero and the SCR is OFF.

When an ESD stress occurs on the input pin, at $\mathbf{t} = \mathbf{t}_0$, the discharge current is absorbed by the capacitance, the SCR does not trigger. From $\mathbf{t}_0$ to $\mathbf{t}_1$, the ESD current charges up the decoupling capacitance. The voltage $\mathbf{V}_{scr}$ increases gradually and the capacitance charges up.

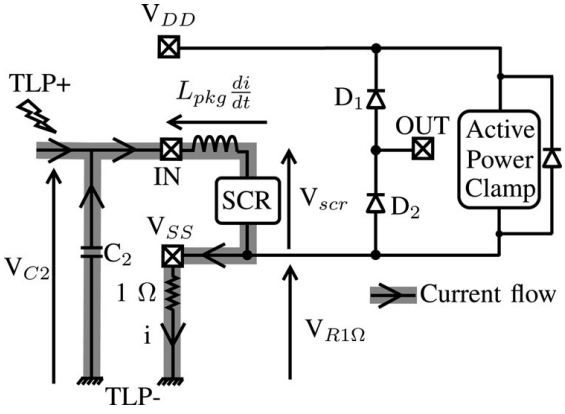


Fig. 24. Simplified schematic showing the ESD current path into the circuit from $\mathbf{t}_1$ to $\mathbf{t}_2$, when the SCR deviate the TLP current and current capacitance.

When the capacitance charge voltage reaches the triggering voltage of SCR (about 13 V), at $\mathbf{t} = \mathbf{t}_1$, it turns ON and goes to snap-back state. The voltage across the SCR drops to 2 V, the holding voltage,

and its on-state resistance becomes very low. The SCR then conducts the current from the generator TLP and cumulates the discharge current of the capacitance creating a very strong current peak as shown on the simulation results of Fig. 23. The voltage difference between the SCR and capacitance is balanced by the inductive effect of the input package to match with Kirchhoff's voltage law: ($V_{C2} - L_{in} \times di/dt - V_{scr} - V_{R1\Omega} = 0$). Fig. 24 shows the current path into the circuit during this phase.

When the TLP pulse ends, at $t = t_2$, the ESD current flow stops that creates an abrupt change on the current simulation results. The charge voltage of capacitance is still higher than the holding voltage of the SCR. The capacitance continues to discharge through the SCR. At $t = t_3$, as the current becomes lower than the holding current, the SCR switches OFF. This leads to a shift of the current, from about 200 mA to 0, on the current simulation result of Fig. 23. After the SCR stops, no more current circulates through the circuit.

This capacitance's charge and discharge effects during an ESD stress has been highlighted by P. Besse in [28] for an automotive device and an external capacitance used as an electromagnetic interference (EMI) filter. The same effect could occur for an integrated capacitance and power clamp as shown in [29].

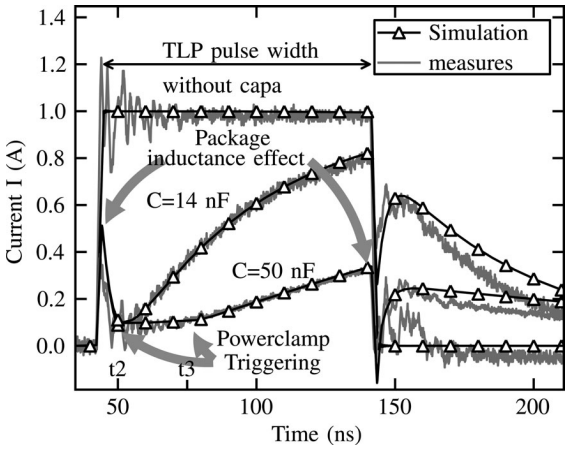


Fig. 25. Measurements and simulations of the current in the 1-Ω ground resistance for 1-A TLP pulse injected from output to ground, with 14 nF, 50 nF, and without IC decoupling capacitance.

V. Comparison Between Measurement and Simulation

A. Case 1: Decoupling Capacitance Connected Between V_{DD} and Vss

The simulation results and measurements comparison are shown in Fig. 25. For various decoupling capacitance values (50 nF, 14 nF, no capacitance) the simulations perfectly match with the 1-Ω resistance measurements. As can be noticed, from t_2 to t_3, a small current circulates through the 1Ω resistance.

This current corresponds to the conduction of the NMOS transistor of the output buffer due to the polarization of the gate-drain coupling capacitance charging up rapidly during the transition of injected TLP pulse. This current is 100 mA for 1-A stress. This was not predicted by only taking into account the protection devices in the simulation.

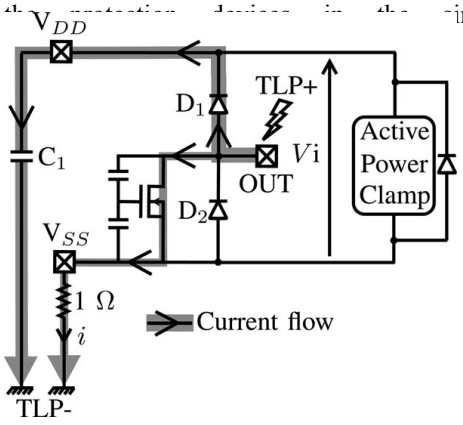


Fig. 26. Connection of the pulldown output transistor to take into account the gate coupling effect.

Consequently, a more complex model for system level ESD prediction must include the pull-down transistor, which is given into the IBIS description. The gate coupling capacitance (Cgd) of the output buffers that control the current flowing through the drivers must also be included. We solved this mismatch by using a Spice level 1 MOS structure fitted from the data given in IBIS files as shown in Fig. 26. The exposed experience considered an injection of only 1 A. For higher stress level, the gate coupling effect can lead to a very high gate polarization that can drive the transistor into avalanche mode and then it can be destroyed. To estimate the ESD robustness, the breakdown voltage of the output drivers should be known to predict the failure of the device.

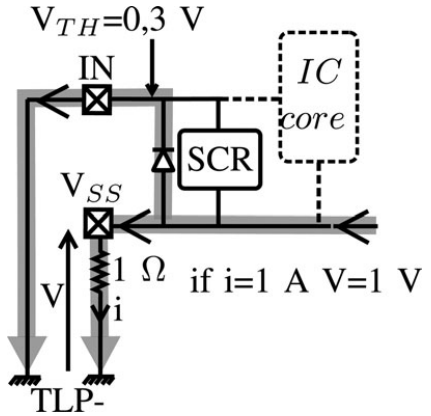


Fig. 27. New path created by the one-ohm measurement technique when the input is connected to the ground.

The 1-Ω resistance allows the measurement of the current going out of the circuit through the ground pin. But, this method has to be used cautiously. For example, when we study the impact of the external

decoupling capacitance, the inverter input was not connected and the current could not be discharged through this input pin. However, if the input is connected to the ground plane, new paths could be created as shown in Fig. 27.
The ESD discharge current that circulates through the 1-Ω resistance increases the internal **Vss** potential allowing the SCR conduction in reverse mode.

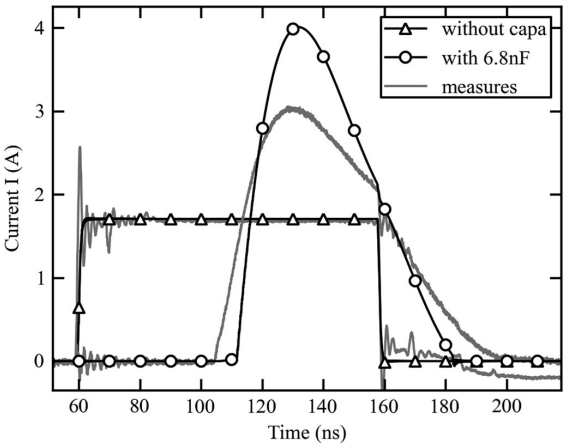


Fig. 28. Measurements and simulations of the current in the 1-Ω ground resistance for 2-A TLP pulse injected from input to ground, with 6.8 nF and without capacitance.

B. Case 2: Capacitance Connected Between the Input and Ground Plane

The simulation results are compared with measurements and shown in Fig. 28. The simulation without capacitance matches perfectly with the measurement. With 6.8 nF capacitance, a difference of about 20% is observed between simulation and measurement. When the SRC turns ON, it conducts the current derived from the TLP generator plus the discharge of the capacitance. This observed mismatch could be attributed to several reasons: First, the TLP generator model is a perfect current source forcing the current whatever the system load. Second, the discharge time constant of the capacitance could be more complex than a perfect one.
First, the model validity of TLP generator is checked. Simulations and measurements of incident and reflected current waveforms from TLP probe are performed with and without capacitance and are shown in Fig. 29. The first and last parts of the curve are, respectively, the incident and reflected current pulses. The superposition of the two waveforms (center part) corresponds to the transmitted current. Without decoupling capacitance, the polarization point of the SCR does not vary during the pulse, the transmitted current is constant.
When a capacitance is connected, the impedance viewed by the TLP generator changes during the pulse due to the charge and discharge of the capacitance and the variation of SCR polarization point. It shows that the transmitted current is not constant as depicted in Fig. 29. In both cases, the current waveform simulation matches with the measurement thus indicating that the TLP generator model is not the origin of the discrepancy.

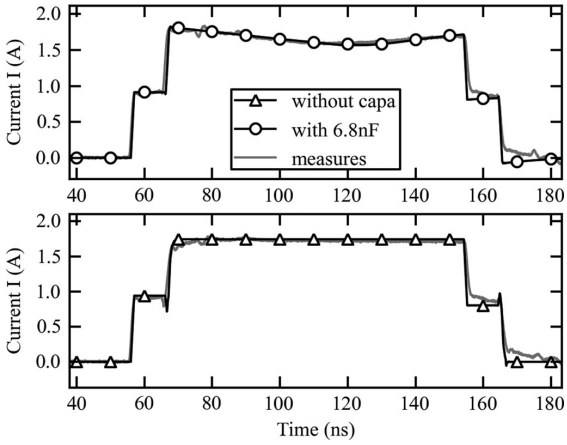


Fig. 29. Measurements and simulations of the current in the 1-Ω ground resistance for 2-A TLP pulse injected from input to ground, with 6.8 nF and without capacitance.

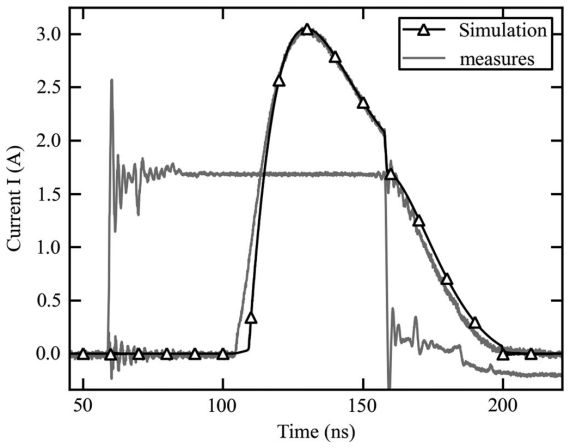


Fig. 30. Measurements and optimized simulations of the current in the 1-Ω ground resistance for 2-A TLP pulse injected from input to ground, with 6.8 nF and without capacitance.

The discrepancy is mainly due to the discharge constant of the capacitance. It is possible to adjust the simulation result by increasing the total resistance of the discharge branches. This has been done by inserting the equivalent high-frequency model of the capacitance on one part, and by introducing some access resistance to the SRC of 1Ω. The comparison of measurement and adjusted simulation is given in Fig. 30.

VI. Conclusion

In this paper, we proposed a methodology to build a complete system level ESD simulation taking into account the IC, the PCB, and the test bench. This methodology based on the principle of standalone blocks provides system level designers the possibility of simulating their electronic systems and analyzing their behavior during ESD test.
Each block of the system is independent and can be reused in any other configuration. The various

elements of the system: ESD generator, PCB, package, and IC have been presented and described separately.

We have demonstrated that it is possible to build IC ESD behavioral models without knowing in detail the internal IC ESD protection by using a combination of informations from IBIS files and TLP measurements. Based on existing model (IBIS) and from dedicated ESD measurements, the modeling approach of an IC has been presented. We demonstrated that IBIS model gives a lot of very useful information like buffers, on-chip capacitances, and passive elements of the package, but it has to be improved regarding the ESD strategy and high power **I** (**V**) curves to perform ESD simulations. The ESD protection models added are extracted from TLP measurements and fitted with classical diodes, SCR or MOS models. Even if our ESD protection's behavioral models introduce an error (lower than 20%), the comparison of theoretical and experimental results shows that it is possible to perform predictive simulation with good correlation to measured data. This could be explained by the fact that the 20% of mismatch on the models of the protections only introduces a small variation on the equivalent resistance. For a fixed current, it results in a small variation of the voltage across the protection device, and due to the number of elements in the current path, the cumulative impedance is higher than the one of the protections.

To summarize, the simulation and measurement results, for the simple case considered here, show that even when using these simple semiempirical models to perform the simulation, complex interactions can be identified which involve the IC ESD protection network and the other components of the system like the IC external decoupling capacitance. This paper shows that it is necessary to identify relevant system level and component circuit parameters to be able to simulate the ESD behavior at the system level.

Apossible solution to allowfast system level ESD verification and simulation would be is to add improved ESD protection network description and parameters in conventional IBIS files.

In addition, other parameters such as the amount of energy supported by IC internal ESD protection elements can give an estimate of the ESD robustness at system level.

Future work will focus on the robustness and susceptibility investigations and how to implement it at simulation level.

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