Design and Construction Affects on PWB Reliability

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The reliability, as tested by thermal cycling, of printed wire boards (PWB) are established by three variables; copper quality, material robustness and design. The copper quality was most influential and could be evaluated pretty accurately by microsectioning methods to determine the general quality of the board. Next in the hierarchy of influence came the robustness of material, and the tertiary influence was design. With the advent of Removal of Hazardous Substances (RoHS) causing lead to be removed from solder and the increase in thermal excursions for assembly and rework to 260C, materials tend to be as much a problem as copper quality in the robustness of PWBs. At the new lead free assembly temperatures the materials tend to break down adding to the failure modes caused by lead free assembly. Both the copper quality and material robustness are improving and now PWB designs are beginning to become more influential in the ability to provide a robust board in a lead-free environment. In this paper we will review the general trends in design like the use of non-functional pads, or nickel as part of the surface finish and rank the overall robustness of each.

It must be pointed out from the start that effect of the three major influences in PWB reliability is a product of all three influences and how they interact with each other. In a given application the copper, material and design are working in concert where the three are producing an overall, combined influence. Really good copper plating (or material) may overcome a weakness in design, or, a really robust design may overcome copper plating that is marginally applied. In high density PWBs all three influences have to be in line to be able to produce reliable product through assembly and in the end use environment.

It should be observed that the major cause of thermal cycling reliability degradation is due to the z-axis expansion of the dielectric material. Most dielectric is a composite of fiber glass weave in a matrix of epoxy. The expansion of the dielectric is constrained in the x and y axis due to the warp and weft of the fiber glass. There is no constraint in the z-axis. Figure 1 is of a cross section showing the z-axis expansion that would be typical when the circuit board is heated to 260C. The z-axis expansion of the dielectric is usually two orders of magnitude higher than the copper expansion. This z-axis expansion is the major contributor to breaks in the copper interconnections in the PWB.

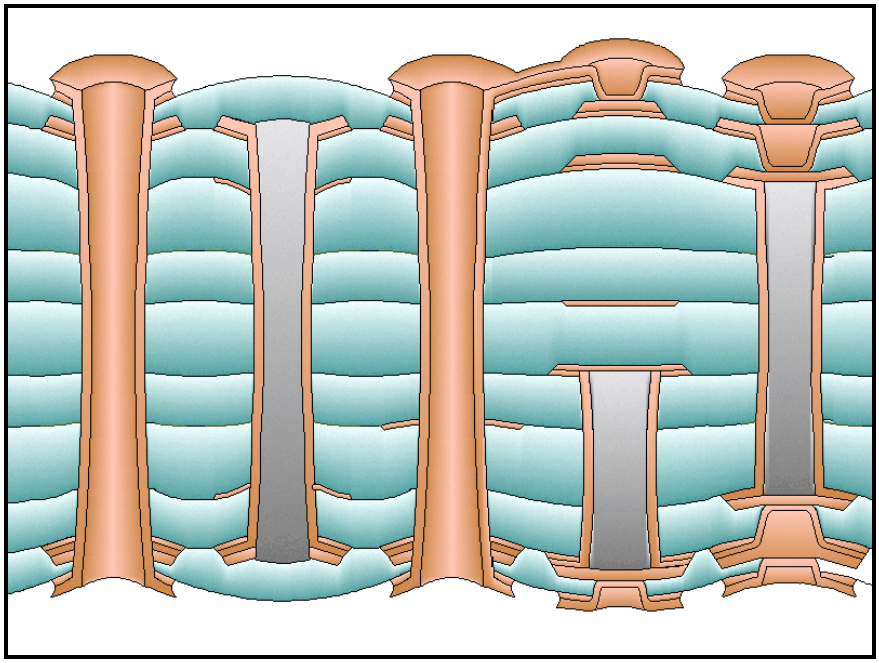

Figure 1 – Cross Section of Typical Interconnections at 260C

Quality is the assurance that the circuit board meets requirements. That the board has the specified copper thickness, the correct size, the correct solder mask etc. Quality is concerned with the board having been through the correct steps and that the paper work is filled out. Quality if based on conformance to specifications while reliability is the proof that the board works. Reliability is the proof that in spite of meeting quality requirements the product will work and survive assembly and in the end use environment. Quality is the talk; reliability is the walk.

One definition of reliability is when the strength of an object is stronger than the physical forces that act on the object. When the object is stronger than the forces that act upon it, the object will not break and therefore be considered reliable. Another definition of reliability is when a person gets to work on time every day so they are reliable due to meeting a perceived requirement, or duty. In this case they are always there, on time doing a job and are therefore, considered reliable. In this paper we are addressing much more to the former method. We are measuring the reliability of a representative coupon that is fabricated to withstand a number of thermal cycles without increasing the circuitry resistance by 10%; or have a material degradation. The 10% increase in resistance is principally due to cracks in the copper of conductor structures used in the fabrication process.

By material degradation we mean that the material does not change capacitance between ground planes, on coupons designed to measure capacitance change, by greater that 4%. The 4% change in capacitance this is not an approved number but usually provides visible damage in microscopic evaluations. Greater than a 4% change in capacitance reflects material degradation of adhesive delamination, cohesive failure and crazing. Both types of defects, the copper cracks and material degradation, are visible by microscopic examination of failed coupons and in the corresponding or associated circuit boards.

Based on those definitions of what reliability is, and under standing that this is reliability that is tested until a representative coupon fails, we can test until failure and determine relative reliability. If for example tested as received a coupon achieves a mean of 500 cycles to failure and one with a different design achieves 250 cycles to failure we consider the second design to be half as robust, half as able to meet the needs of the application. That does not automatically imply that the second design will not work. The first design, maybe, reliable for 10 years in the field, and the second design may be good for five years in the field but if the product is warranted for three years in the field then both are reliable enough to meet the design requirement. We can rank the two variables; the first configuration being twice as reliable as the second.

These ranking of the designs are from the reliability tests that are generated, in most cases, from tests on the same production run. The data comes from relative coupons which have been normalized to be the same copper thickness and of the same material. Some of the tests have the two designs in the same coupon while other are from two different coupons but both are on the same production panels. As a point of disclosure this ranking is based on Interconnect Stress Testing (IST) using IPC methods from TM 650, IPC procedure 2.6.26 DC Current Inducted Thermal Cycling.

Figure 2 is the latest IST tester which automatically sets up and thermal cycles individual IST coupons to specific temperatures, monitoring the coupons for changes in resistance. The equipment can precondition to simulate assembly and rework and then proceed with thermal cycles to failure. The equipment monitors and records the cycles to failure data for review.

Figure 2 –IST Tester, Eight Head with Coupons, Three Screen Shots

In order to measure the reliability we use representative coupons. These coupons are the same as the production panel and are fabricated with the same process steps with which the board was fabricated. There fore the coupon is a testable version of the PWB. The typical coupon has been through every process step as the PWB including the same material, lamination, drilling, hole preparation, surface finish and routing. The typical design has all the types of interconnections as the board, has on the tightest grid, heating circuits, DELAM circuits, registration circuits and other specialized circuits. The coupon usually has hundreds of interconnects of a given type so the sample is statistically valid when compared to the PWB.

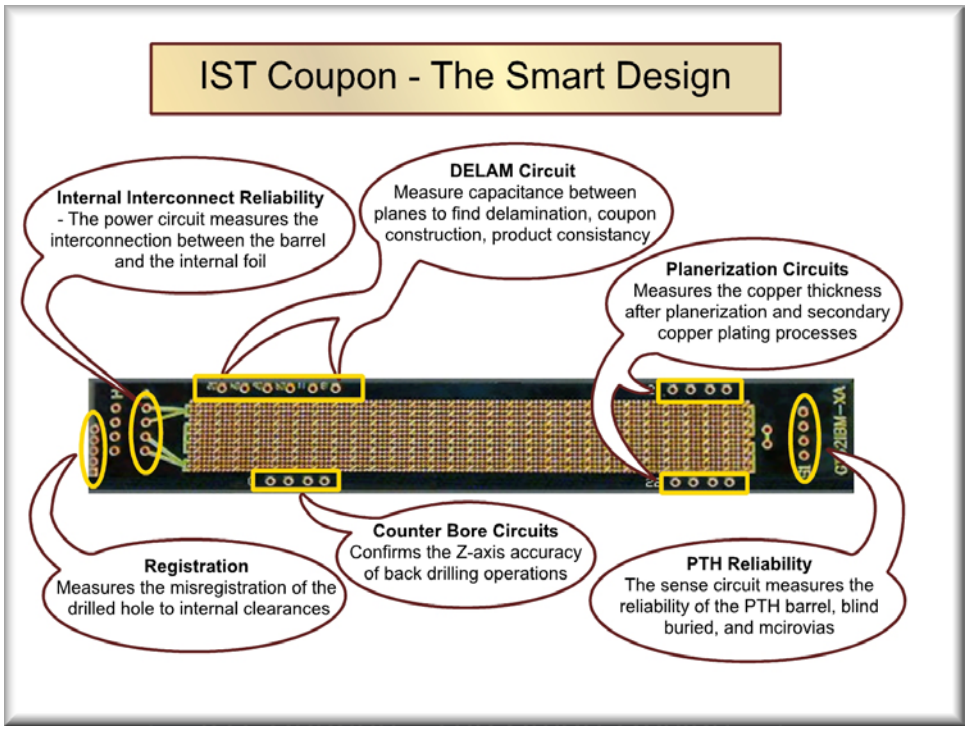

Figure 3 – IST Coupon

IST testing continues until a circuit reaches a 10% increase in resistance. The heating of the coupons stops within seconds of reaching the 10% increase. This means the coupon is not catastrophically destroyed but is in the process of failing. This allows us to place the coupon under a thermal camera and apply a small current to the failing circuit. This small current, typically between .5 and 2 amps, allows us to heat the most damaged circuit and find the one most damaged interconnection. This allows us to microsection the most damaged interconnection and observe the failure as it is happening. This gives us a great advantage in being able to see the failure mode, be it a barrel crack, corner crack or interconnect failure and under stand how the failure occurred.

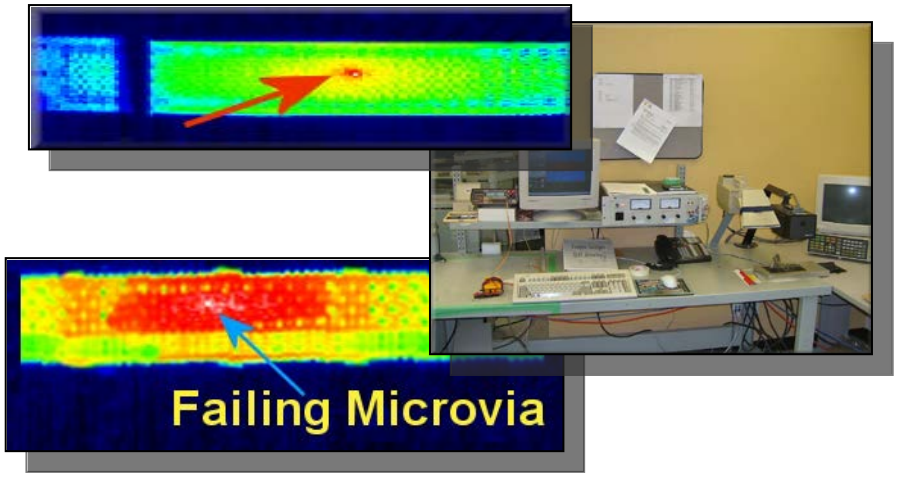

Figure 4 – Photos of Hot Interconnect Structures and Equipment

There are a number of failure modes that are seen. We understand that these failures were not visible before thermal cycling but are found after the circuits failed. These include failures that are obvious on microsection evaluation. The cause of the weakness may not be easily observed based on microscopic examination even though the failure is observed. Figure 5 shows to most observed failure modes based on interconnect structure (with the exception of microvias). These failures include corner cracks, two types of barrel cracks, interconnect failures on PTHs blind and buried vias and butt joint failure and lifted pad on capped buried via. Please note that the lifted cap on a capped buried via without an accompanying corner crack is not an electrical failure. The cap, once it is lifted, is not an integral part of the circuit.

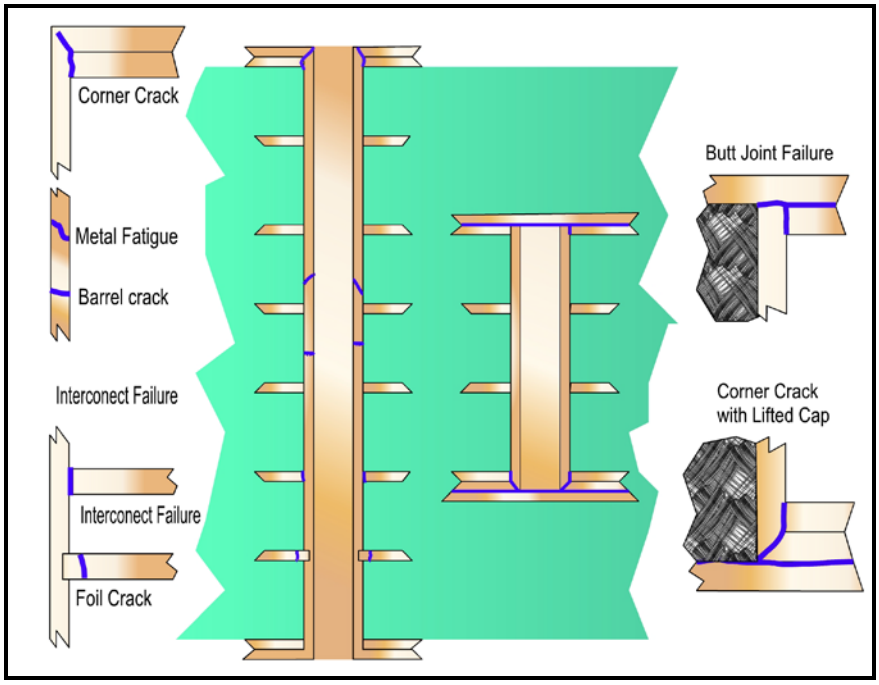

Figure 5 – Some Typical Failure Modes

In microvias failure modes most common is a separation between the base of the microvia and the target pad, followed by a microvia barrel crack corner crack and, rarely, a pull out type failure that is a circumferential crack around the base of the microvia (figure 6). There other failure modes that will be addressed later on compound interconnect structures; that is structures were the microvias are stacked on other microvias and stacked on buried vias.

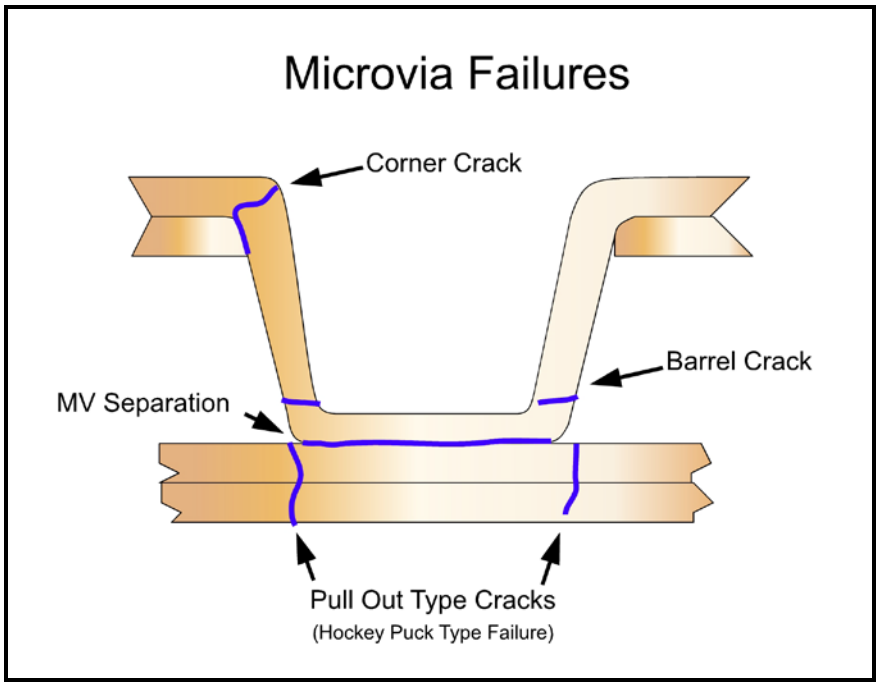

Figure 6 – Some Typical Microvia Failure Modes

Given this overview of how we test the relative reliability one can see how easy it is to evaluate design influences in reliability particularly after lead-free assembly and rework simulation. What we are concerned with includes the interconnect structure and material robustness for given layer counts, processing (like hole fill), the presence of non-functional pads, holes sizes, surface finishes, grid sizes and stacked and staggered microvias. Our goal on this paper is to rank these influences as to which are the most robust to the least robust in a given design variable.

Ranking of Interconnection Types

We will start with the interconnection type. This is the ranking of structures that are well made without quality issues like copper thickness or copper distribution. If we rank them from most robust to least, we would rank interconnections robustness as microvia, staggered microvias, plated through hole (PTH), stacked microvias, blind vias, and buried vias. We will consider the stacked and staggered microvias as compound structures later in this paper.

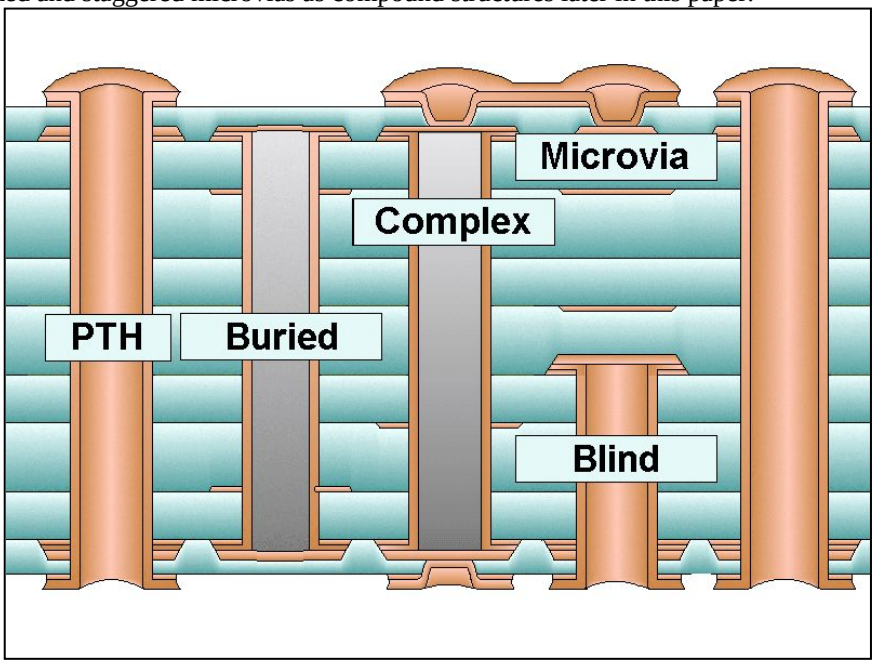

Figure 7 – Some Typical Interconnect Structures

Surface Finish as a Reliability Influence

Surface finish has a thermal cycling reliability component from two sources. Nickel in electroless nickel gold electroless (ENiG) or nickel in electrolytic nickel gold surface finish and fused solder in the form of hot air solder leveling (HASL), hot air leveling (HAL) and fusing both have a significant reliability impact. Most other types of surface finishes like tin, silver and OSP do not have a direct affect on reliability based on thermal cycle testing.

Nickel as one of the layers of a surface finish is either good, or, detrimental in PCB reliability. Normally well applied nickel extends the life of circuit boards by a factor of three or more. The same coupons fabricated with and without nickel will have the nickel boards out perform the coupon with other types of finishes. We call this nickel protection where nickel significantly extends the cycles to failure frequently by a factor of three. Usually we can not break interconnections in 1000 cycles with nickel through out the interconnect structure. The nickel stops the crack and performs well in thermal cycle testing. Figure 8 shows nickel as the protector. The crack forms after many thermal excursions but stops when it hits the nickel.

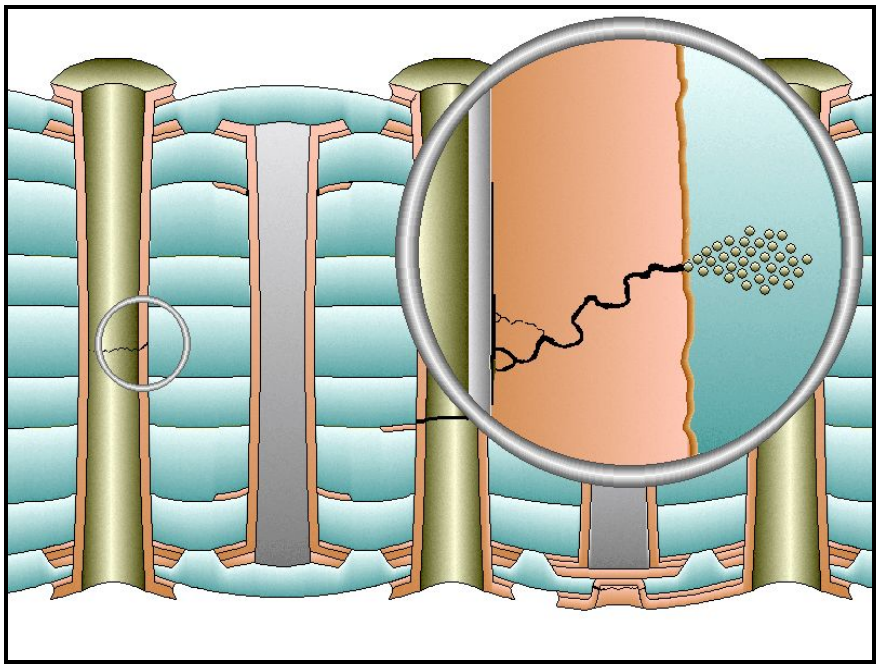

Figure 8 – Nickel Protection

Nickel is a protector of interconnections that is unless there is a problem with the application of the nickel. Usually coupons with nicks, bubbles, or breaks in the nickel finish will fail early. They tend to fail in a third the time of the same coupons without nickel. It appears that a defect in the nickel will force a crack that will crack from the nickel layer into the hole. This is called nickel acceleration. It is a rare condition but is common enough that it should be taken seriously.

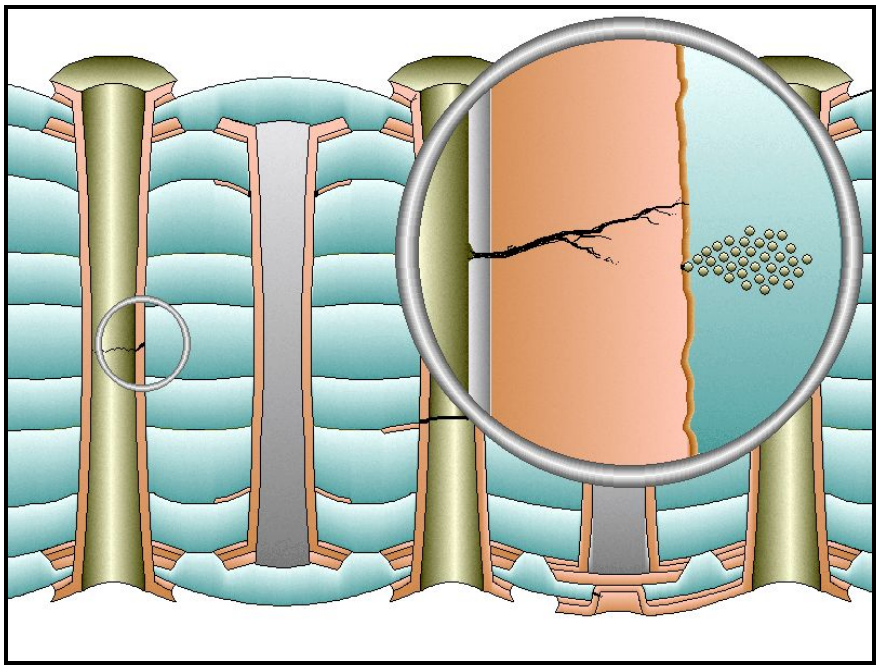

Figure 9 – Nickel Acceleration

The concept of HASL and solder fusing makes a lot of sense with eutectic solder but not so much sense in lead free applications. It appears that the amount of damage to materials is significant in applications 260°C or higher. There is a problem expressed as barrel cracks in PTHs that are solder filled. So there is a tendency to have reduced thermal cycling reliability using fused surface finishes. The other surface finishes do not tend to produce reductions in PWB reliability. That is not to say that a fused surface finish cannot be robust but great effort must be taken to make this a robust process step. There are two problems with these molten solder applications, barrel cracks which are solder filled and copper dissolution.

The filled crack is hard to measure because the solder is conductive and does not show as a significant change in resistance so the damage is invisible. If the crack occurred during the application of the solder it would not be found during the prescreening process. Also the copper interconnections in the surrounding area would be stress relieved by the crack.

Lead free solder tends to dissolve copper. The copper dissolution is obvious in the crack as the two sides of the crack do not match. The normal crack, one without copper dissolution has two sides that fit like jig saw puzzle pieces. In the case of copper dissolution the edges do not fit. Copper dissolution may be serious enough to violate copper thickness requirements.

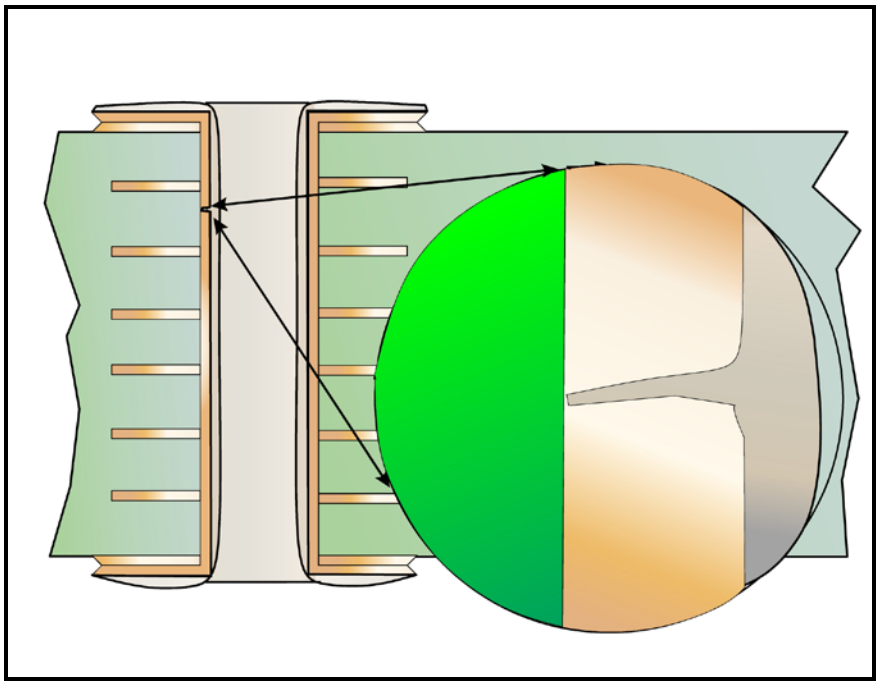

Figure 10 - Barrel Crack with Solder and Copper Dissolution

With surface finishes the most robust, based on thermal cycle testing, is a finish with well applied nickel, all other surface finishes, finishes with fused solder and the least reliable is finishes with nickel poorly applied.

The Reliability of Hole Size

Hole size plays a role in the ranking of design robustness. Again given a well made and well electroplated hole the larger hole sizes are more robust. The smaller the hole size the less robust the hole will be. When it comes to hole size large heavily plated holes tend to have interconnection problems while small holes fail for barrel cracks. The smallest hole size we have tested, some down as small as .11 mm (.0045") are surprisingly robust.

The problem with very small holes, .11 mm (.0045") in a grid size of .5 mm (.020") is there is tendency for material damage in the form of crazing. Crazing tends to be a path for conductive anodic filament (CAF) growth. So the application for the small hole and grid size must be one that had a controlled, not humid, environment.

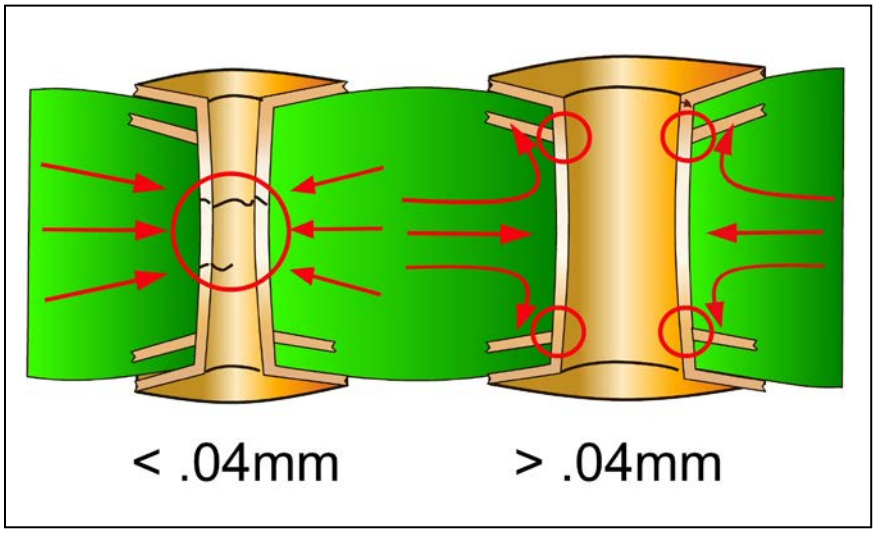

Figure 11 – The Effect of Hole Size on Failure Modes

The Effect of Grid Size on Reliability

The influence of grid size is based on failure of the laminate. Grid sizes greater than 1.3mm (.050”) will have less delamination and more often they will exhibit material degradation. With 1mm (.040”) we see delamination as the major material failure mode. Grid sizes of .8mm (.032”) tend to have cohesive failures and grid sizes of .7mm (.020”) tend to have material failure due to crazing.

It should be noted that all types of material break down can cause a path that is part of the five parts (path, electrical potential, moisture, ionic contamination and adjacent circuits) that are required for conductive anodic filament (CAF) growth. Having any sort of material breakdown is bad for circuits in that it could compromise dielectric constant, provide a path for CAF or artificially strain relieve the other circuits.

Large grid circuits, 2 mm to 2.5 mm (.080” or .100”), tend to stress relief material preventing delamination in the material itself. Large grids are spaced so far apart that they tend to be able to stress relieve them selves with out incurring material damage. The visco-elastic property of most PWB materials can easily expand between holes at 2 mm (.080”) allowing a degree of stress relief.

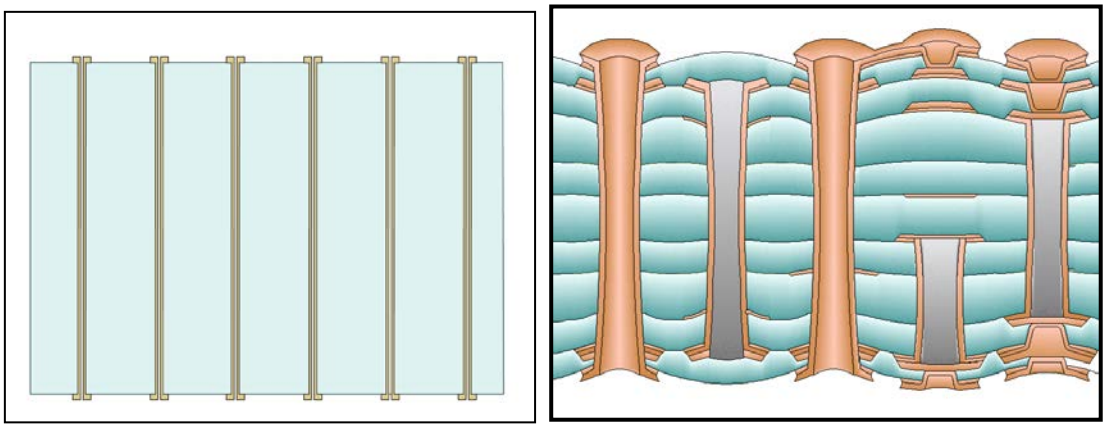

Figure 12 – Grid Size .100” and Image of Cross Section without Material Damage

Adhesive delamination is the breakdown of the material adhesion between laminated surfaces like the “a-stage” and “b-stage” material, “b-stage” and copper and epoxy to glass bundles packages. This is most prevalent in 1 mm and 1.2 mm (.040” and .05”) grid sizes. This is the type of delamination that is made worse by humidity entrapped in the dielectric prior to assembly and rework.

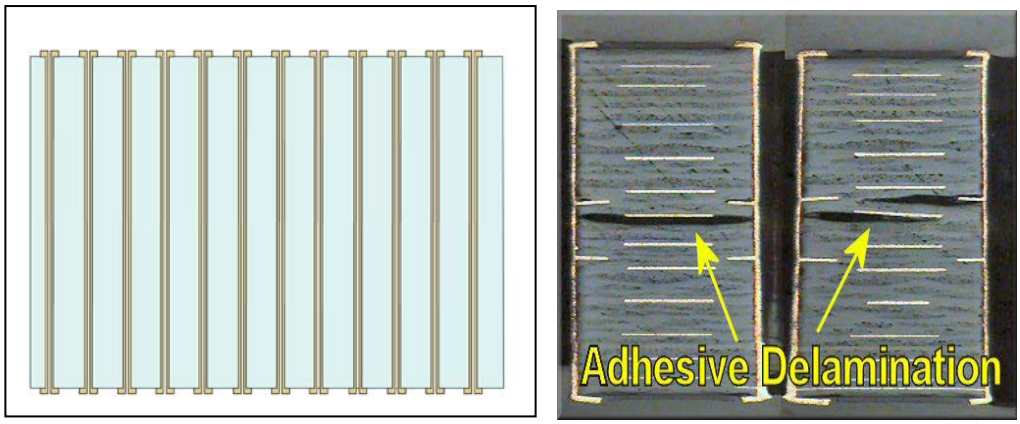

Figure 13 – Grid Size .040” and Photo of Adhesive Delamination

Cohesive breakdown is within the resin system itself. The breakdown is not particularly limited to the “a –stage” or “b-stage”. It will cross the “a-stage” and ``b-stage” boundary. It is most often found in .8mm (.032”) grid sizes. This type of material degradation is not so dependent on moisture in the dielectric but is most often associated with material failure due to temperature degradation.

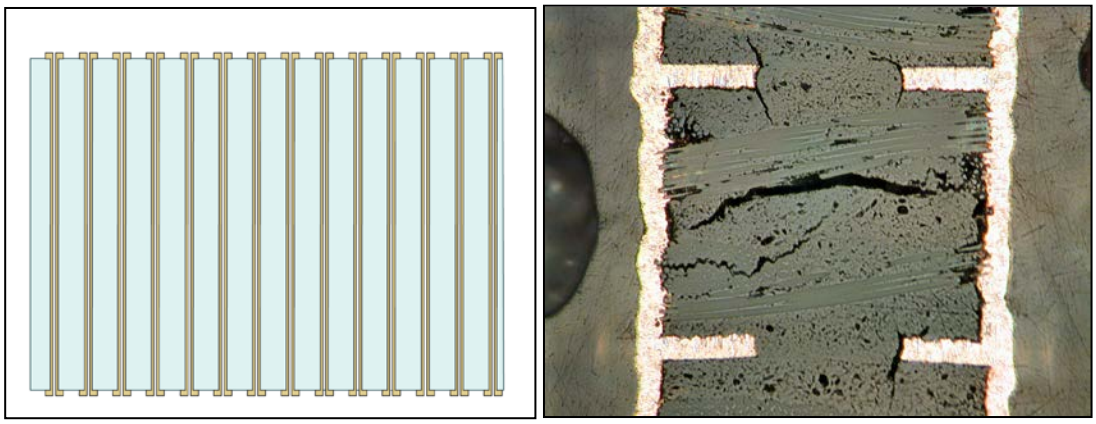

Figure 14 – Grid Size .032" and Photo of Cohesive Failure

There are a number of companies that are producing .11mm (.0045") holes on boards up to 6.4mm (.250") thick. The holes tend to be drilled on a .5mm (.020") grid. The holes are robust for thermal cycle testing but the material appears frequently compromised. Boards with these dimensions appear to have crazing. Crazing is the separation between the epoxy and glass fibers and is seen frequently in .5mm (.020") grid sizes. Crazing is a concern for CAF type failures.

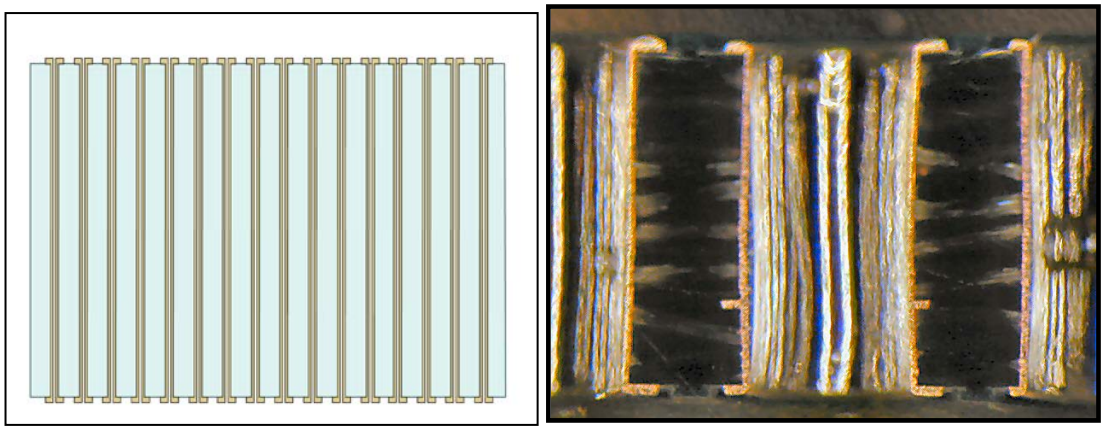

Figure 15 – Grid Size .020" and Photo of Crazing (not .11mm hole)

Material breakdown, or decomposition, due to using a basic, low Tg, material in a lead-free environment where the PWB is exposed to lead-free temperatures of 260°C can cause the material to turn black and apparently boil. The result is gross material breakdown without damage to circuits. It should be noted that this type of gross material degradation does not damage copper interconnections.

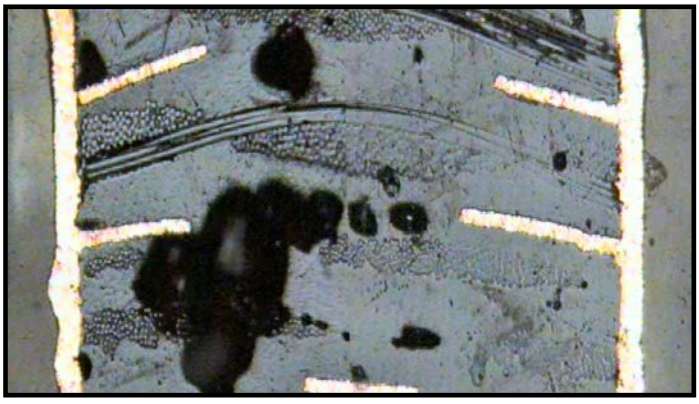

Figure 16 – Photo of Material Decomposition

The Reliability Effect of Nonfunctional Pads

Nonfunctional pads are pads that have no electrical connection, pads that have no circuit connected to any active part of the circuit board. They are used as dummy connections in order to keep the interconnection layout consistent and to help drilling. The problem is that this type of construction produces areas where the resin is thin. Having non-functional pads at every layer produces areas where the non-functional pads produce what is described as telegraphing. Telegraphing is where the stack of non-functional pads produces an image of the stack through the full thickness of the board producing high spots where ever there is a PTH. These high spots are due to the epoxy being squeezed so thin that there is glass lock between each layer. These area cause a pancake layer of non-functional pads with very little epoxy between each pad. Generally speaking the presents of non-functional pads is a determent to the reliability of PWBs.

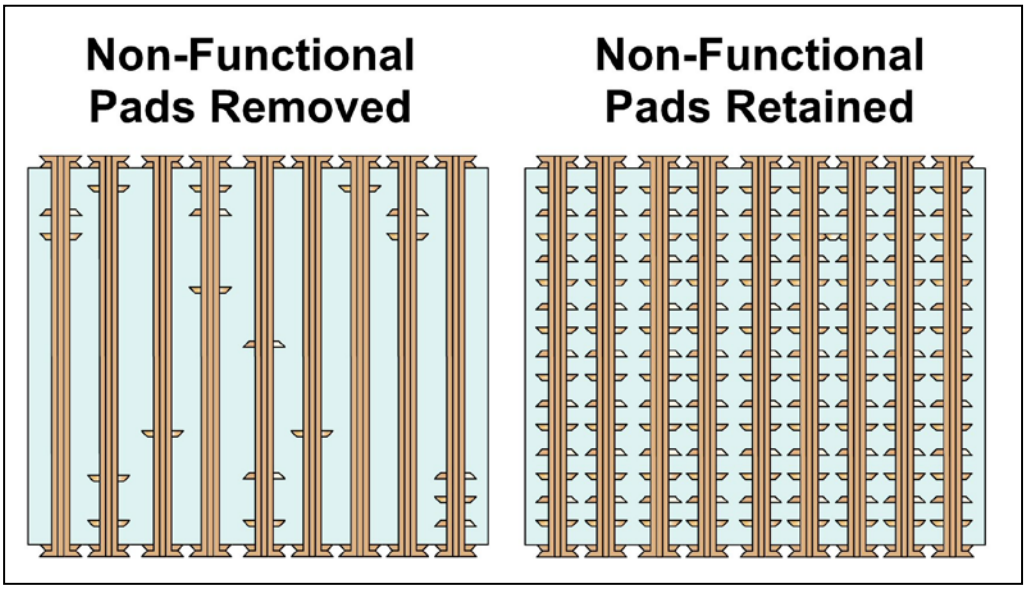

Figure 17 – Non-functional Pad In and Removed

The Effect of Types of Internal Interconnections on PWB Reliability

The influences of types of internal interconnections must be taken into account. Basically there are three types of internal interconnection formats that can be fabricated, flush interconnections, interconnections that have etch back and interconnections that have "three point" contact (figure 18).

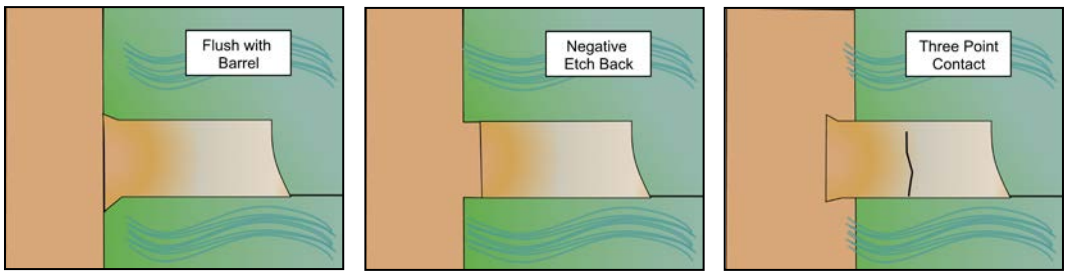

Figure 18 – Three Types of Internal Interconnections

Although negative etchback is about as robust as flush it appears that the three point contact has a tendency to cause foil cracks. It is counter intuitive but three point contact is the least reliable of the interconnections. This is due to foil cracks of the copper at the internal layer. Thus the ranking would be; flush, negative etch back and the least reliable would be three point contact.

The Influence on Reliability of Buried Via Fills and Caps

There are two types of buried vias; opened and capped. The open buried via may be filled with the "b-stage" resin, with a third party resin or electrolytic copper. The capped buried via may have a butt joint, or have copper wrap, and a cap. So that gives us a possibility of four constructions for buried vias.

Generally speaking the simple buried via with no third party fill is most robust. The epoxy filling is from the b-stage from the layers above and below the buried via. This type of buried via has the same z-axis expansion and glass transition temperature (Tg) as the board. Eye brow delamination may occur but that mostly is a condition of concern rather than a rejection point.

Then next most robust is a buried via where the buried via is filled with a third party epoxy. The third party fill may have copper and silver particles or be just epoxy. The third party filler has a different CTE and Tg than the dielectric materials and this sometimes causes barrel cracks in the buried via. This change in CTE and Tg tends to expand equally in x, y and z-axis producing significant problems in expansion mismatches resulting in barrel cracks.

The least robust type of buried via fill is a copper via fill where the via is filled by electroplating the hole closed. This fill is relatively new and is very susceptible to corner cracks due to over skiving and planerization.

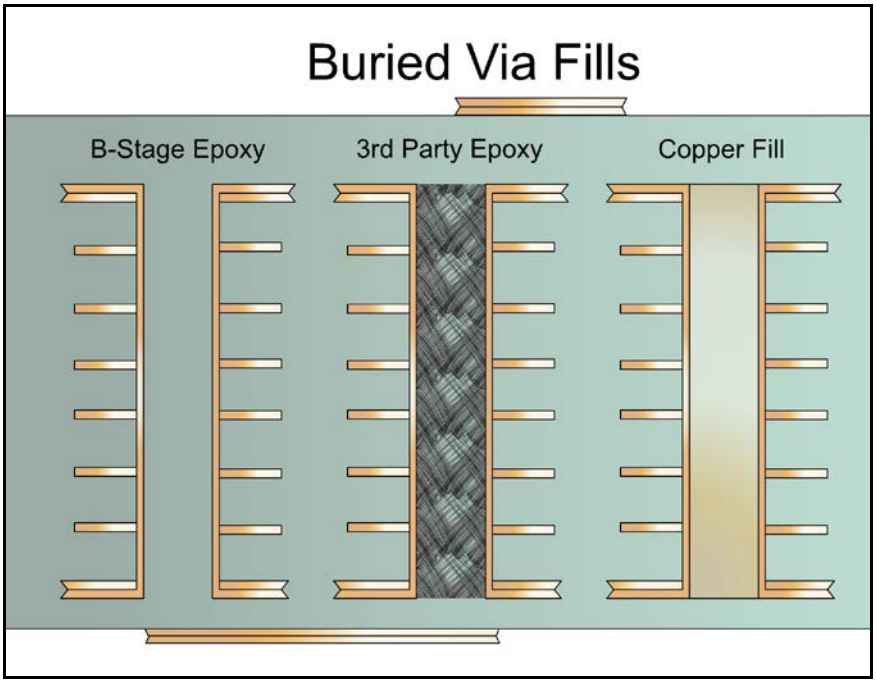

Figure 19 – Three Types of Buried Via Fills

Capped buried vias have additional process steps that can complicate the fabrication and produce product that is vulnerable to other problems. If in the process of skiving the buried via the skiving is too aggressive the thin copper wrap can cause corner cracks in the buried via. It should be noted that the cap is not part of the electrical circuit, can be completely separated from the buried via, without an electrical degradation of the interconnection.

There are two types of capped vias, butt joint vias and buried vias with a copper wrap. Buried with a copper wrap of .002” or greater tend to be robust. Butt joints tend to fail in just a few thermal excursions.

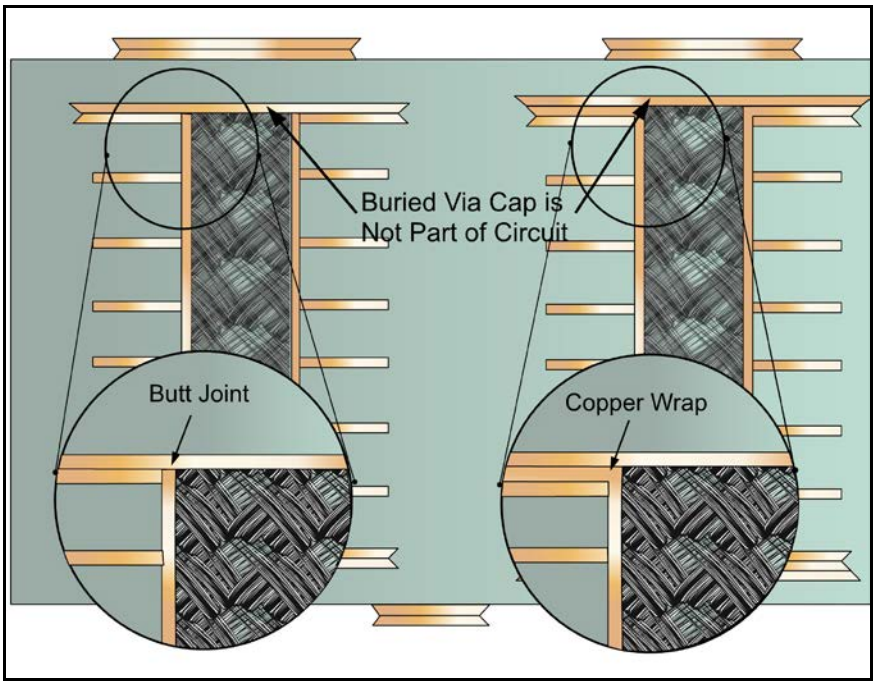

Figure 20 – Two Types of Capped Buried Via Constructions

The Influence of Via Fills and Caps on Microvias

Microvias are usually the most robust, interconnections when considered on their own. There are three types of microvias those that are surface mounted, buried and buried and stacked on other microvias and buried vias. We will address stacked microvias presently.

The most robust microvia is that surface microvia without a fill followed by microvias hat are buried and filled with "b-stage", next microvias with a third party fill and copper fill microvias are the least robust. It appears that copper filled microvias are just too new and have a tendency to have corner cracks. It should be noted that stand alone microvias with caps or without caps have no advantage, or detrimental effect, if the process is robust.

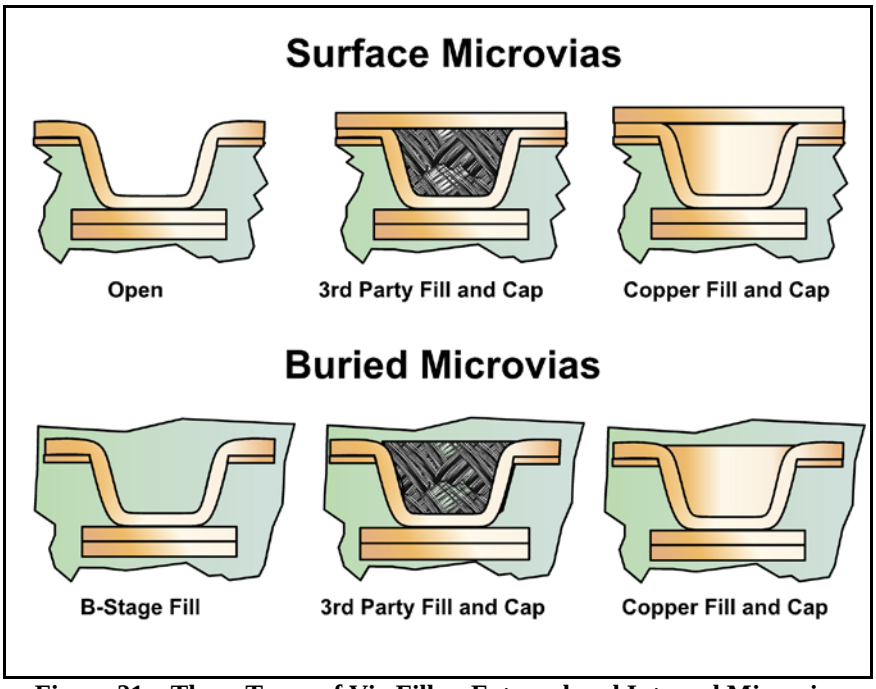

Figure 21 – Three Types of Via Fills – External and Internal Microvias

The Reliability of Stacked and Staggered Microvias

Now we will address the concept of compound interconnections involving stacked microvias where microvias are stacked on top of one and other and microvias stacked on top of buried vias. In both cases the microvias must have copper caps that are part of the electronic circuit. It is important to note that the microvia pad rotation is reversed on stacks of three or more microvias.

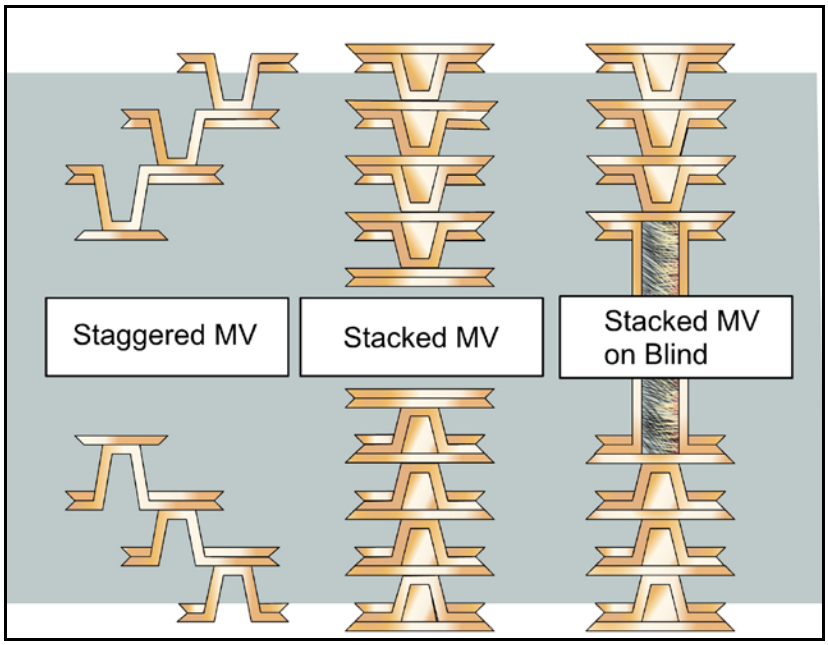

Figure 22 – Two Types of Compound Constructions –Stacked and Staggered

This pad rotation has a major effect on the failure modes of microvias. When we look at individual or staggered microvias we notice the pad rotation is down. In stacked microvia the pad rotation is up. There appears to be a greater tendency for corner cracks, particularly with copper filled microvias in stacked type of configurations.

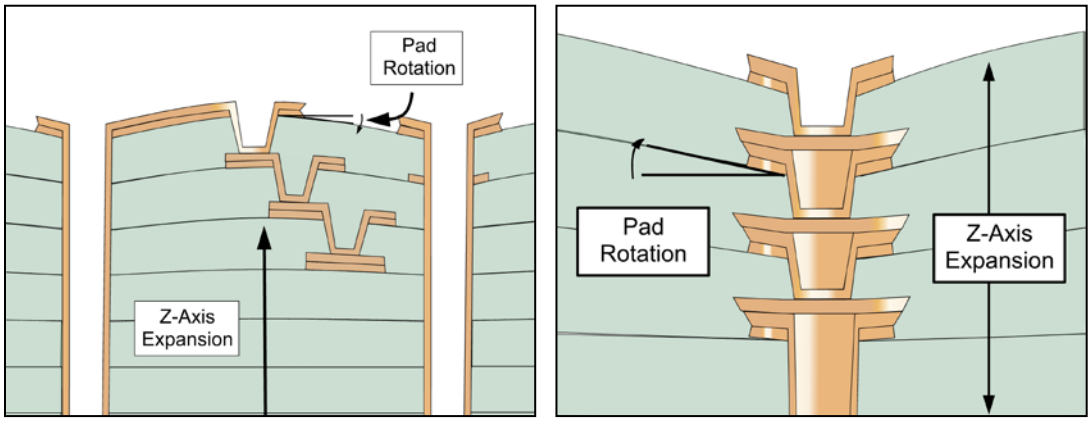

Figure 23 – Pad Rotation in Stacked vs. Staggered Microvias

The number of ways microvias may fail when stacked on the top of each other or a buried via has increased. We have at least eight types of failures that may occur when a microvia is stacked on another microvia or on top of a buried via. These extra failure modes require a mature process that is in balance in order to produce robust compound structures.

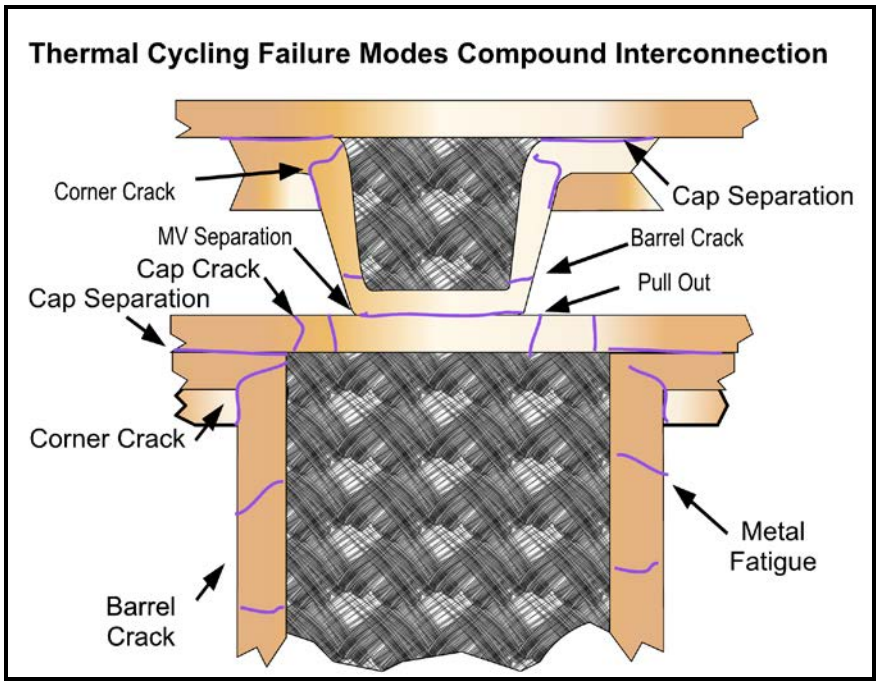

Figure 24- Failure Modes of Compound Interconnect Structures

One of the recent studies show that there is a problem with microvia stacked four high as compared to three high. It may be that the forces change on microvia stacks greater than three high. Stacking microvias four high or greater is a challenge.

The Reliability of Stacked verses Staggered Microvias

Stacked and staggered microvias were recently tested. Fortunately the staggered and stacked microvias were in the same coupon and both were tested together, using dual sense testing. The failure mode in both configurations was pad separation. The staggered microvias were two orders of magnitude more robust than the stacked microvias. Although stacked microvias can be robust there are so many failure modes that it is a challenge to produce stacked microvia greater than three high while staggered microvias present no immediate problems.

IST Cycles to Failure - Tested at 190°C						
Precon	As Received			Predoncitioning 6X260°C		
Type	Buried	Microvia		Buried	Microvia	
Circuit	Power	Staggered	Stacked	Power	Staggered	Stacked
Mean	1000	1000	79	1000	887	3
StDev	0	0	32	0	182	0
Min	1000	1000	52	1000	582	3
Max	1000	1000	138	1000	1000	3
Range	0	0	86	0	418	0
Coef Var	0%	0%	41%	0.0	0.2	0.0

Figure 25 - Recent Results of Microvia Testing – Stacked verse Staggered

Conditions that Do Not Produce Reliability Concerns

There are some design and configuration that are, counter intuitively, not as influential as determined by reliability testing. Pad to hole registration is not particularly influential in PWB reliability. As long as the hole hits the pad there is a tendency for a reliable circuit based on thermal cycle testing. There is one exception, when the hole has broken out of a pad and into the trace, particularly when the trace is part of a heating circuit, there can be a reduction of thermal cycles to failure. Other than that there is no real reliability concern based on hole to pad registration.

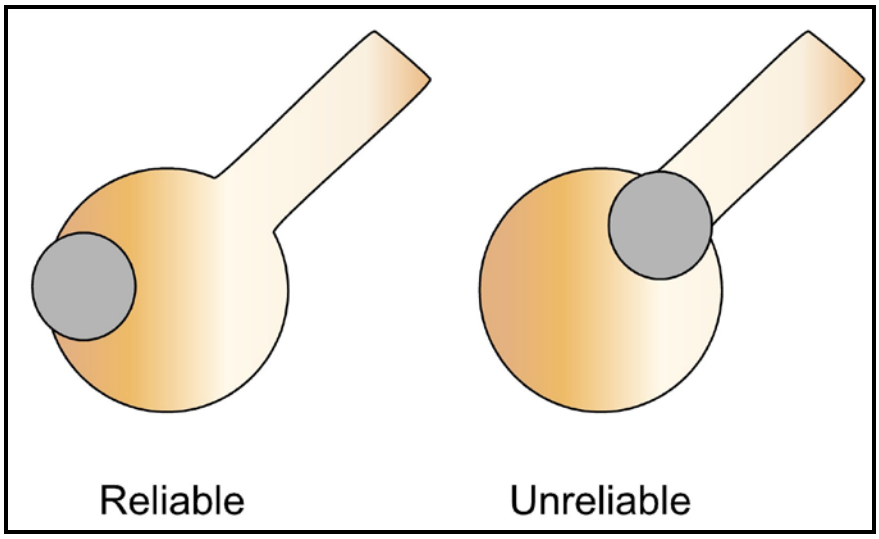

Figure 26 - Two Types of Hole Misregistration – `Break In`

One of the less influential factors is line width. It appears that fabricators are not very influenced by line width. Line width does not seem to be a factor, or, if it is a factor, line width anomalies are remove from the test samples before they are subjected to reliability testing. With automated optical inspection (AOI) and electrical test (ET) it may be that product that has line width anomalies are removed from the test sample. There was a line thickness issue on surface mounted filled microvias that were processed by a third party were line thickness was reduced on the exposed trace going to the microvia. This was the only case we ran into over the years where line anomaly was a problem. It must be that on HDI product line width and neck down issues produce opens which are found before reliability testing.

Baking is not very influential in reliability results. Usually if there is a material defect a pre-bake does not make a difference. If we find that adhesive delamination is affecting the coupon a pre-bake of the balance of the coupons does not dramatically reduce the material failure rates. This is counter intuitive but it is rare that baking makes a difference in reliability results. We would typically bake 8 hours or greater at 150C without significant reduction in the number of coupons that would pass the capacitance test. It may be that boards that are going to delaminate will do so with or without the bake. It may also be that we have a better means of finding delamination with the DELAM circuits. Since internal material damage is usually not visible in the board, and the number of boards with material damage is usually in the neighborhood of 10% to 20%, it may be that baking boards is not effective at reducing material damage. It is hard to find boards with random delamination, using random microsectioning as the method of proving an improvement.

It must be pointed out that anything can go wrong with fabricating circuit boards producing discrepant product. It must also be pointed out that anything may go correctly producing a synergy that may add up to overcoming a problem. Let us say groups of boards have been under plated violating the plating specification. It may be that high reliability material and an accommodating design may compensate for the thin plating. Thermal cycle testing of that discrepant product may show that the reliability if fine even though the product violates the minimum copper thickness requirement. The material, design and copper thickness in this example work in synergy to produce product that is strong and capable in a given application.

Design is the variable that is most covert of the three; copper quality, material robustness and design. Design makes or breaks a board in a subtle way, making one manufacturer capable, while another is not capable of making reliable boards using the same or similar material, and the same process steps. Design has been given a free reign based on what a board needs to do electrically, not what is reliable in reality. The limits of fabrication are beginning to encroach on this “free reign” and now designers need to understand what is the capability of their design, will they have fabricators that can build the design, and what is the reliability of that design through assembly and in the end use environment.