

Fill the Void V - Mitigation of Voiding for Bottom Terminated Components

Tony Lentz
FCT Assembly
Greeley, CO, USA

Greg Smith
BlueRing Stencils
Lumberton, NJ, USA

ABSTRACT

Voiding in solder joints has been studied extensively, and the effects of many variables compared and contrasted with respect to voiding performance. Solder paste flux, solder powder size, stencil design, circuit board design, via-in-pad design, surface finish, component size, reflow profile, vacuum reflow, nitrogen reflow and other parameters have been varied and voiding quantified for each. The results show some differences in voiding performance with respect to most of these variables but these variables are not independent of each other. Voiding in solder joints is a complex issue that often requires multiple approaches to reduce voiding below required limits. This paper focuses on solutions to voiding for commonly used bottom terminated components (BTCs).

When voiding is an issue, it is often not possible to change the solder paste or circuit board design due to end user requirements and time constraints. It is much easier to change the stencil design and the reflow profile in an effort to reduce voiding, and this can be done in a timely manner. Stencil design and reflow profile can be used to minimize voiding for BTCs like Quad Flat No Lead (QFN) components. Optimization of the window pane size and web width can help with voiding. Changing the volume of solder paste on the I/O perimeter pads of QFNs also has an effect on voiding. Use of linear ramp-to-spike (RTS) reflow profiles reduces voiding with some solder pastes, while ramp-soak-spike (RSS) profiles work better for other solder pastes. Stencil design and reflow profile were optimized for a variety of QFN components in order to minimize voiding. The results of this testing were quantified, summarized and recommendations given for ideal voiding performance.

Key words: voiding, bottom terminated components, stencil design, reflow profile, window pane

INTRODUCTION

Voids in solder joints are a commonplace occurrence and can lead to issues with solder joint quality and integrity. Voids can interfere with electrical signal quality which may create noise in the signal and can cause issues with component functionality. Voids in solder joints may increase resistance which can lead to improper heat transfer and potential overheating of the components. This is especially a problem for BTCs like light emitting diodes (LEDs) and QFNs. Voids can cause mechanical weakness in solder joints which may lead to joint cracking. This is mainly an issue when the void area is exceptionally large, or the voids are concentrated on a plane like the board pad interface or the component lead interface. Regardless of the effects of voids, they are always present and the total void area must fall below maximum acceptable limits.

Many studies have been published which investigate factors that influence voiding and suggest methods of mitigating voids in solder joints. In Fill the Void [1] stencil design, solder paste, reflow profile were studied with regards to their effects on voiding. Fill the Void II - An Investigation into Methods of Reducing Voiding [2] investigates the effects of solder paste, solder powder size, solder powder manufacturer, stencil design, surface finish, reflow profile, reflow method, and vacuum during reflow on voiding. In Fill the Void III [3] solder powder size, solder alloy, surface finish, low voiding solder paste, and stencil designs were tested with respect to voiding. Fill the Void IV - Elimination of Inter-Via Voiding [4] focused on voiding in QFN thermal pads with via holes and various hole plugging options, along with various stencil designs. In How Does Surface Finish Affect Solder Paste Performance [5] voiding was studied for a combination of circuit board surface finishes along with a variety of solder pastes. Size Matters - The Effects of Solder Powder Size on Solder Paste Performance [6] examined the effects of solder powder size on voiding in two different solder pastes. In The Effects of Surface Finish on Solder Paste Performance - the Sequel [7] surface finish, solder pastes, and reflow profiles were all varied with respect to voiding. Finally, in Root Cause Stencil Design for SMT Component Thermal Lands [8] the effects of stencil design on voiding was studied for a variety of BTCs. This paper is a continuation of work on stencil designs for BTCs, and includes variation of reflow profiles and different sizes of QFN's.

Voiding in solder joints can be caused by many things (Figure 1).

Originally presented at IPC APEX 2020

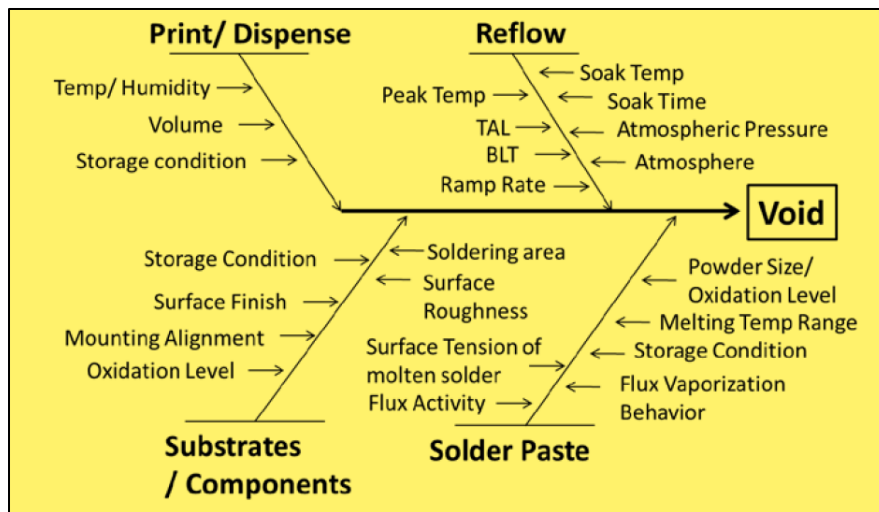


Figure 1 – Cause and Effect Diagram for Voids in Solder Joints

In most cases voiding is the result of a combination of factors that interact together. However, in some cases, voiding is caused mainly by one factor that can over-ride the effects of other factors. When this occurs, attempts to change voiding behavior may fail due to the strong influence of that specific factor. In the world of contract manufacturing, it is not easy to change a specific factor, like circuit board design, surface finish, or component style. In the end, reducing voiding is often challenging but is possible through changes in factors that can be controlled such as solder paste, stencil design and reflow profile. It is the intent of this work to optimize the combination of stencil design, solder paste and reflow profile in order to minimize voiding in QFN component thermal pads.

METHODOLOGY

Thermal Circuit Board

The thermal circuit board used for this experimentation is shown below (Figure 2). This circuit board is made of FR4 material that is 0.062 inches thick, with 1 oz etched copper pads and electroless nickel immersion gold (ENIG) surface finish.

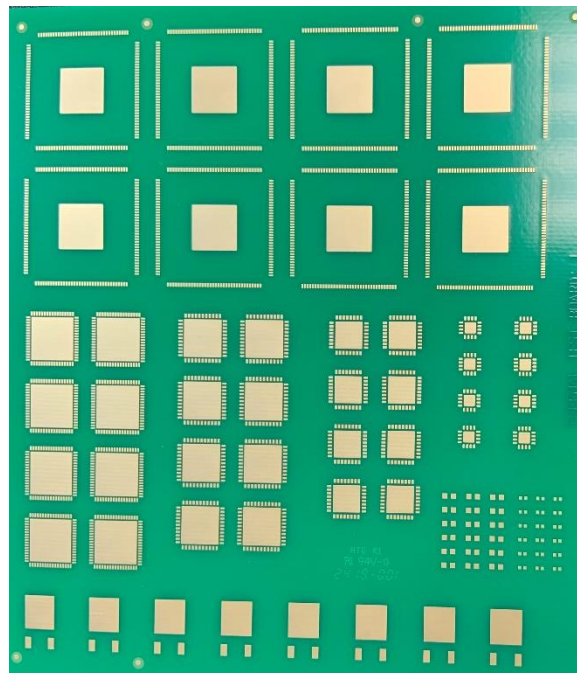


Figure 2 – Thermal Circuit Board

Solder Paste

Originally presented at IPC APEX 2020

A low voiding no clean SAC305 type 4 solder paste was used for this work. This solder paste was chosen because it is known to minimize potential voiding in a range of process conditions.

Stencil Design

Two laser cut stencils were made with the same aperture patterns but on different thickness of stainless-steel foil. One stencil was made on 102 μm (4 mil) thick foil and the other was made on 127 μm (5 mil) thick foil. Nano-coatings were not used on these stencils. The stencil aperture design is shown below (Figure 3).

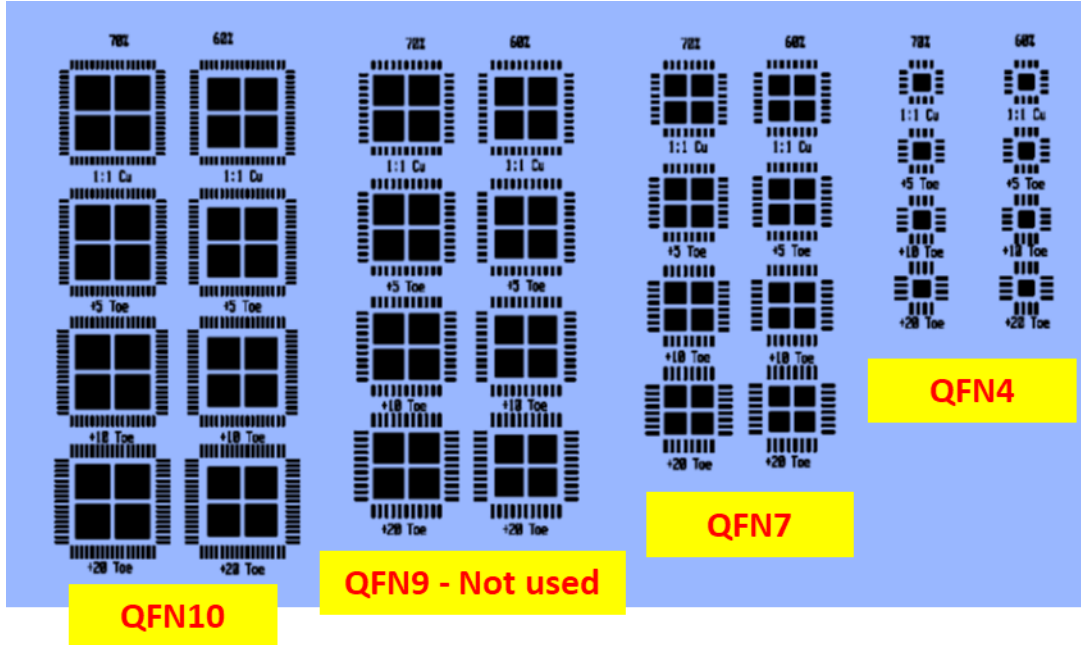


Figure 3 – Stencil Aperture Design

The area of solder paste coverage was varied between 70% and 60% for each size of QFN. The stencil designs for the perimeter (I/O) pads were varied at 1:1 with the copper pad, pad length + 5 mils (toe), pad length + 10 mils (toe), and pad length + 20 mils (toe). In all cases the perimeter pad widths were held the same. The stencil design is summarized in the table below (Table 1).

Table 1 – Stencil Design Summary

Component	Thermal Paste Area (%)	Thermal # Panes	Thermal Web Width (mils)	Thermal Brick Size (mils)	Perimeter Aperture Width (mils)	Perimeter Aperture Length 1:1 (mils)	Perimeter Aperture Length +5 (mils)	Perimeter Aperture Length +10 (mils)	Perimeter Aperture Length +20 (mils)
QFN 10	70	4	20	133.5	9.8	30.6	35.6	40.6	50.6
QFN 10	60	4	20	124	9.8	30.6	35.6	40.6	50.6
QFN 7	70	4	20	84	12.8	30.6	35.6	40.6	50.6
QFN 7	60	4	20	78	12.8	30.6	35.6	40.6	50.6
QFN 4	70	1	0	68.9	12.8	30.6	35.6	40.6	50.6
QFN 4	60	1	0	63.1	12.8	30.6	35.6	40.6	50.6

The QFN 9 mm components were not used in this experiment, and instead this work focused on the QFN 4 mm, QFN 7 mm and QFN 10 mm sizes. Variations in the length of the QFN perimeter pads paste print was done in combination with variations in the area of coverage on the thermal pad. These stencil modifications were used in an effort to follow up on the work of Tafoya, Ramirez, and O’Neill [9]. Tafoya, et. al. reported that increasing printed solder paste length resulted in decreased voiding. The intent of this work was to combine area of coverage on the thermal pad along with I/O pad solder joint modifications in order to minimize voiding to the lowest possible extent.

Reflow Profile

Reflow was conducted in a 10-zone convection reflow oven with an air atmosphere. A range of reflow profiles were tested which included: linear ramp to spike (RTS), short, short plus a soak, long, and long plus a soak. The measured reflow profile parameters for these are shown below (Table 2).

Table 2 – Measured Reflow Profile Parameters

Profile Name	Max Rise Slope (°C/sec)	Soak Time (150-200°C in sec)	Reflow Time (>220°C in sec)	Peak Temp (°C)	Time (25°C-peak in min)
Linear ramp to spike	1.7-2.1	89-91	73-74	244-247	4.5-4.6
Short	2.0-2.1	65-66	66-69	245-247	3.9
Short plus soak	2.0-2.1	92-94	52-55	242-245	4.3
Long	1.6-1.8	87-89	94-97	249-251	5.4-5.5
Long plus soak	1.5-1.8	114-116	75-80	246-248	5.8-5.9

Each of these profiles was tested with the thermal test board, the low voiding solder paste, and 3 sizes of QFN components and void area was measured. The linear ramp to spike (RTS) profile gave lower overall voiding than the other profiles. This RTS profile was chosen for the remainder of the work (Figure 4).

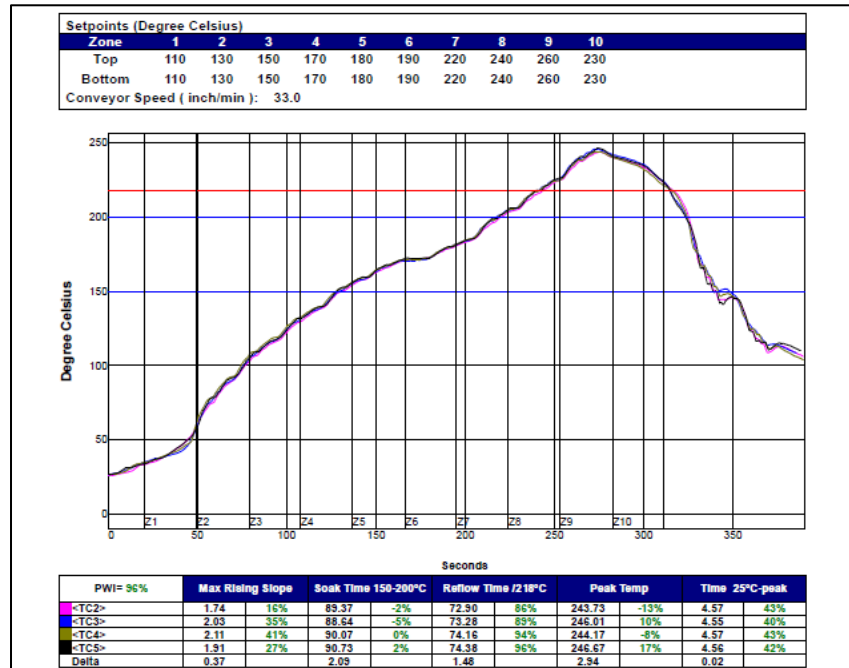


Figure 4 – Linear Ramp to Spike (RTS) Reflow Profile

Voiding

Three sizes of QFN’s were used for this work including 10 mm, 7 mm, and 4 mm body sizes (Figure 5).

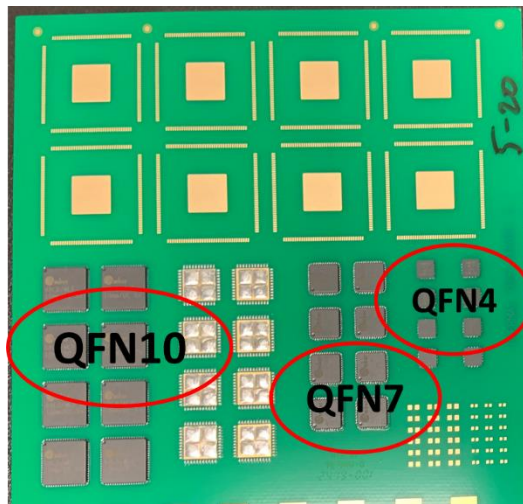


Figure 5 – Thermal Circuit Board with 3 Sizes of QFNs (10 mm, 7 mm, and 4 mm)

Void area and the size of the largest void was measured for each of the QFN thermal pads, using 2D X-ray. Statistical analysis was performed on the data and comparisons were made.

Statistical Analysis

Tukey Kramer honest significant difference (HSD) testing was done on the voiding data sets to compare and contrast the data. Tukey Kramer HSD analysis determines whether multiple data sets are significantly different, or statistically similar. This test is similar to Student's t-test used to compare means. The output of the Tukey Kramer HSD test is a chart that shows the data sets, several data calculations and reports (Figure 6).

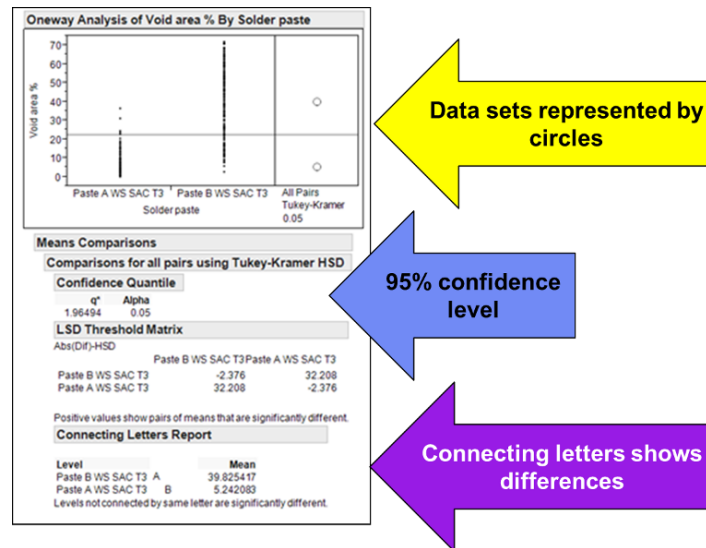


Figure 6 – Explanation of Tukey Kramer HSD Report

The Tukey Kramer HSD analysis shows whether the data sets under comparison are significantly different. This analysis is used to draw general conclusions and show trends in performance.

Process of Work

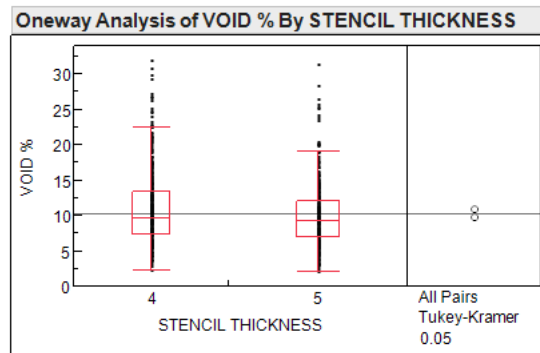
1. 20 thermal circuit boards were run for each of the two stencil thicknesses, for a total of 40 circuit boards.
2. 8 of each QFN component type were placed onto each circuit board, for a total of 24 components per board.
3. After reflow the void area % and the size of the largest void % was measured for the QFN thermal pads.
4. The void data was analyzed using statistical analysis software, and charts were generated.

RESULTS AND DISCUSSION

Voiding by Stencil Thickness

Overall voiding was lower for the 5 mil thick stencil than the 4 mil thick stencil (Figure 7).

Originally presented at IPC APEX 2020



Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

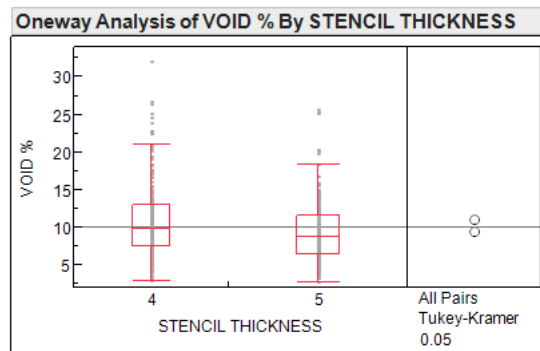
Level	Mean
4 A	10.9
5 B	9.8

Levels not connected by same letter are significantly different.

Figure 7 – Voiding by Stencil Thickness

Based on this result, voiding can be reduced by increasing overall solder paste height. In this case the solder paste height was increased by 25% from the 4 mil thick stencil to the 5 mil thick stencil, and thermal pad voiding was reduced by roughly 10%.

Voiding was lower for the 5 mil thick stencil than the 4 mil thick stencil with 60% area of coverage on the thermal pad (Figure 8).



Excluded Rows 447

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
4 A	11.0
5 B	9.4

Levels not connected by same letter are significantly different.

Figure 8 – Voiding by Stencil Thickness for 60% Area of Coverage

This was not true for the 70% area of coverage patterns (Figure 9). Voiding was statistically similar for the 4 and 5 mil thick stencils in the 70% area of coverage patterns.

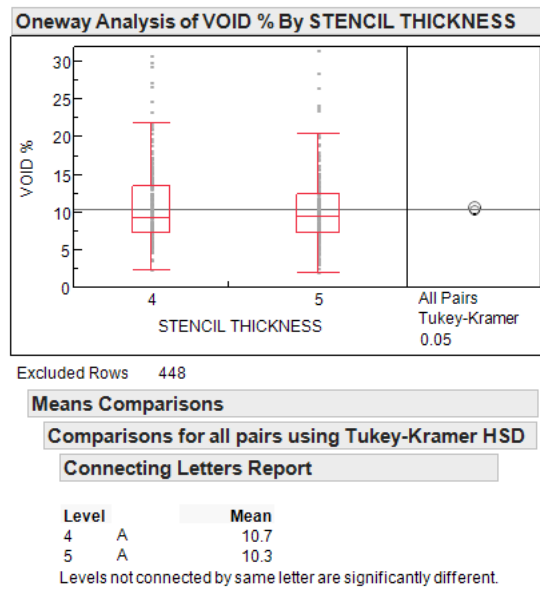


Figure 9 – Voiding by Stencil Thickness for 70% Area of Coverage

Based on this result, increasing the area of solder paste coverage from 60 to 70% makes voiding similar for the 4 and 5 mil thick stencils. The same principles apply for reduction of voiding. Voiding can be reduced by either increasing stencil thickness or increasing area of solder paste coverage, which both increase solder paste volume.

Voiding by Area of Coverage on the Thermal Pads

Voiding by area of coverage for the 4 mil thick stencil is shown below (Figure 10).

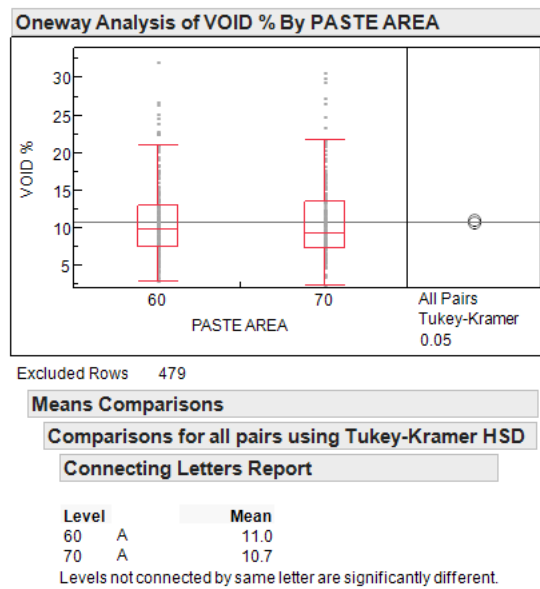


Figure 10 – Voiding by Area of Coverage for the 4 mil Stencil Thickness

Void levels are statistically similar for both 60 and 70% area of coverage with the 4 mil thick stencil. This was not true for the 5 mil thick stencil (Figure 11).

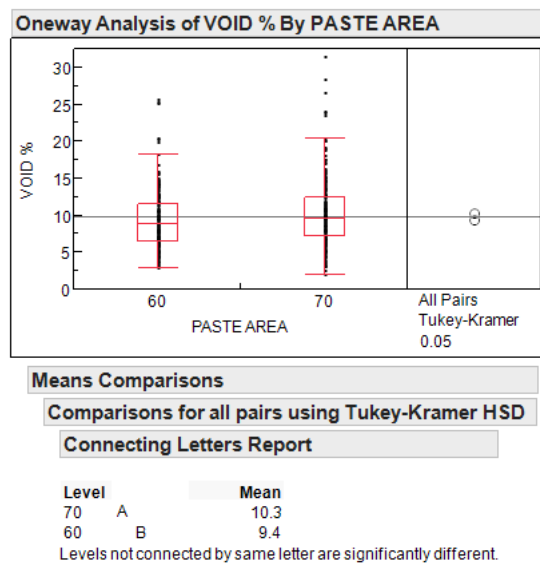


Figure 11 – Voiding by Area of Coverage for the 5 mil Stencil Thickness

Voiding was lower for the 60% area of coverage than the 70% area of coverage with the 5 mil thick stencil. This result is in contrast to the results for the stencil thickness comparisons.

Voiding by Component

The 3 different QFN components showed different voiding behavior (Figure 12).

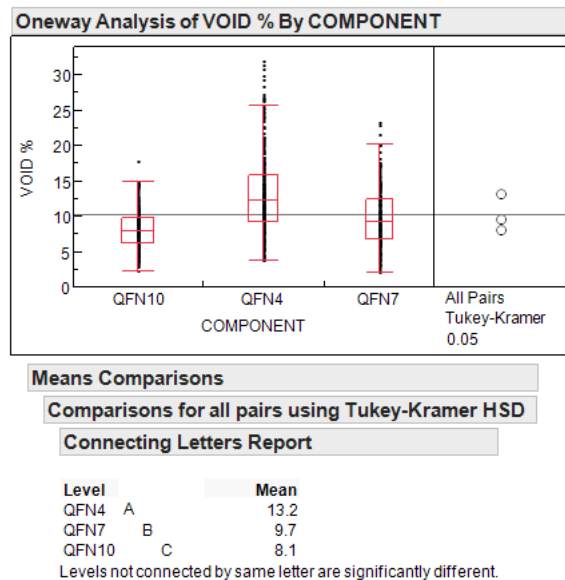


Figure 12 – Voiding by Component

The voiding levels were highest for the 4 mm QFN, followed by the 7 mm QFN, and finally the 10 mm QFN had the lowest overall voiding levels. This was true regardless of stencil thickness or area of coverage.

Voiding by Toe Adder

The most impactful differences in voiding were seen with variations in the length of the solder paste print to the toe side of the QFN perimeter (I/O) pads. This was true regardless of component type (Figure 13).

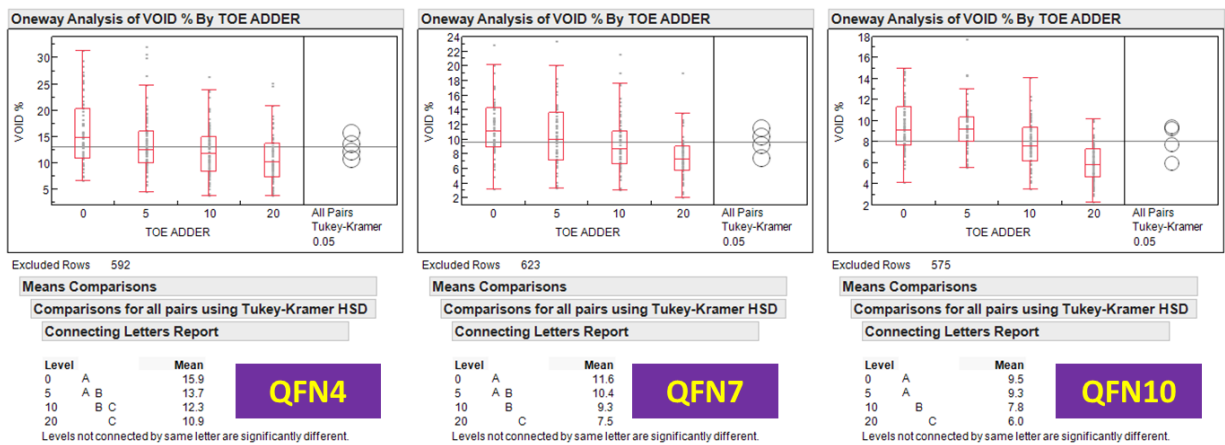


Figure 13 – Voiding by Toe Adder for the QFN4 (Left), QFN7 (Center), and QFN10 (Right)

This trend also holds for each area of coverage coupled with each stencil thickness (Figure 14).

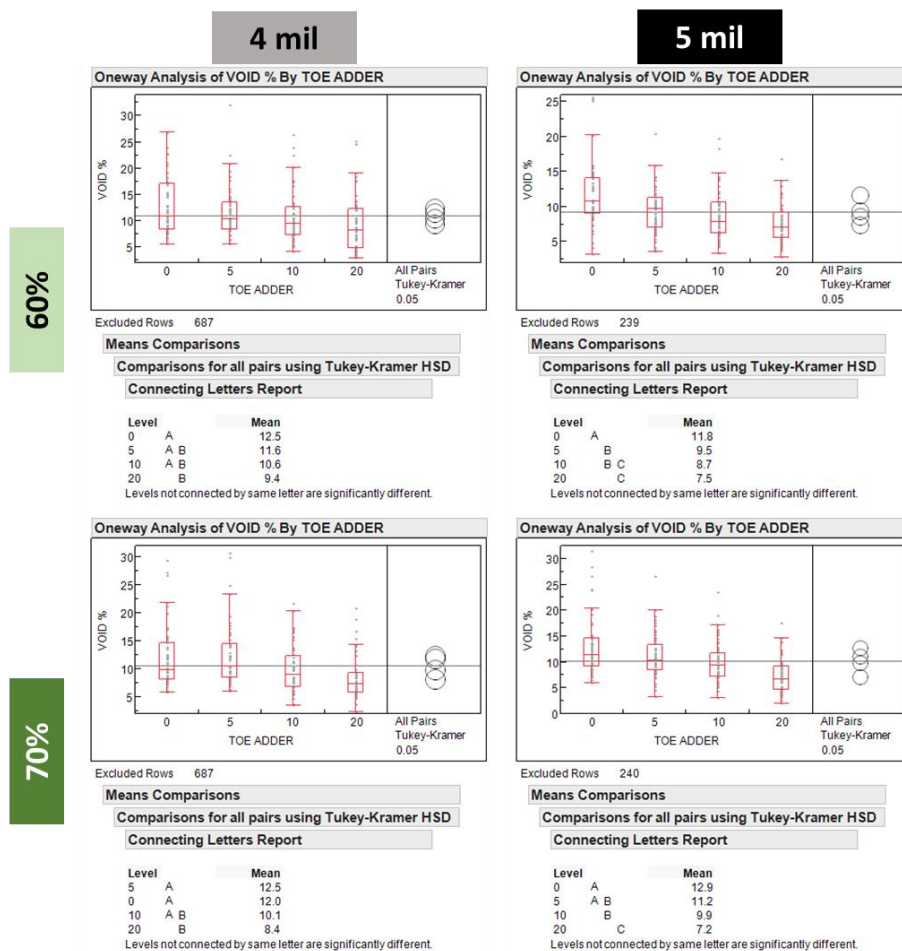


Figure 14 – Voiding by Toe Adder Separated by Area of Coverage and Stencil Thickness

Voiding is highest when the perimeter (I/O) pads were printed with solder paste at 1:1 coverage (0 overprint) on the pads. Most of these comparisons show that voiding is not significantly different between 0 and 5 mils of overprint, or between 5 and 10 mils of overprint. Voiding was reduced by adding length to the solder paste print with the lowest overall voiding given by the 20 mil overprint.

CONCLUSIONS AND RECOMMENDATIONS

Many of the variables that were tested influenced voiding. Several were found to reduce voiding and these are summarized below.

- The linear ramp to spike (RTS) profile produced the lowest voiding as compared to the other profiles that were tested. This is expected and a normal result for the solder paste used in this work.
- Increasing the stencil foil thickness from 4 mils to 5 mils reduced voiding significantly.
- With the 5 mil thick stencil, 60% area of coverage produced lower voiding than the 70% area of coverage.
- Overall voiding area decreases as QFN component body size is increased.
- Overprinting the toe on the QFN perimeter (I/O) leads by 20 mils produces the lowest void area. This is true regardless of stencil thickness and area of coverage.

This work shows that voiding on QFN thermal pad solder joints can be significantly reduced using a low voiding solder paste along with the appropriate reflow profile. Void area can be further reduced through modifications to the stencil design by increasing stencil thickness or adding overprint to the toe of the perimeter (I/O) pads. It is recommended to work with your solder paste and stencil suppliers to reduce voiding to the lowest possible levels.

REFERENCES

- [1] T. Lentz, G. Smith, "Fill the Void", Proceedings of SMTA International, 2016.
- [2] T. Lentz, P. Chonis, J.B. Byers, "Fill the Void II - An Investigation into Methods of Reducing Voiding", Proceedings of IPC APEX Expo, 2017.
- [3] T. Lentz, "Fill the Void III", Proceedings of SMTA International, 2017.
- [4] T. Lentz, G. Smith, "Fill the Void IV - Elimination of Inter-Via Voiding", Proceedings of IPC APEX Expo, 2018.
- [5] T. Lentz, "How Does Surface Finish Affect Solder Paste Performance", Proceedings of SMTA International, 2018.
- [6] T. Lentz, "Size Matters - The Effects of Solder Powder Size on Solder Paste Performance", Proceedings of IPC APEX Expo, 2019.
- [7] T. Lentz, "The Effects of Surface Finish on Solder Paste Performance - the Sequel", Proceedings of SMTA International, 2019.
- [8] G. Smith, T. Lentz, "Root Cause Stencil Design for SMT Component Thermal Lands", Proceedings of SMTA International, 2019.
- [9] C. Tafoya, G. Ramirez, T. O'Neill, "Assessing the Effectiveness of I/O Stencil Aperture Modification on BTC Void Reduction", Proceedings of IPC APEX Expo, 2017.